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Design of a 4-bit Arithmetic and Logic Unit using 9T Full Adder with Optimized Area and Speed

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Abstract*: *Arithmetic Logic Unit (ALU) is the most significant unit of any computing system be it microprocessors, embedded structures or any other computational device. This paper presents delay, power, area and energy optimization of a novel 4-bit Arithmetic logic unit created with the help of a newly designed 9T full adder unit and Gate Diffusion Input (GDI) technique. This novel ALU architecture is made by using a full adder which has only 9 transistors and various multiplexers. To analyze the simulations Cadence Virtuoso tool is used. As per simulation results, delay, power, area and total energy of the ALU design is improved. In this proposed design of 4-bit ALU, delay is reduced by 10.17%. power is reduced by 8.05%. PDP is reduced by 18.20% and transistor count is reduced by 17.82 %.

Index Terms*: *Arithmetic Logic Unit (ALU), Cadence Virtuoso tool, Gate Diffusion Input (GDI), Power Delay Product (PDP).

I. INTRODUCTION

Power consumption, total area, latency and energy consumption are the main criteria's considered while dealing with the requirements of today's electronics era. The power availability of portable electronic devices is very limited. We can say that the ALU plays an important role for the applications such as digital processing and microprocessors. Full adder, which is predominantly used for addition and other operations is the most crucial module while viewing the designing strategy. Clearly any considerable change in full adder design will lead to major improvement in the operation of ALU.Taking this in to account a novel full adder module is created using only 9 Transistors. With the help of this 9T full adder a new ALU unit is created and compared with the existing ALU design. For low area and low power designs, GDI technique is the most efficient method. Using only 2 transistors we can implement any logic function. This is the importance of GDI technique

II. EXISTING 4-BIT ALU DESIGN

A new ALU design was introduced to reduce the delay. The design

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A. *Full Adder*

Full adders are the basic building block for any digital circuit design in case of VLSI.If we want any significant improvement in performance parameters, we must upgrade the full adder specifications accordingly.GDI technique is used to create the full adder module which is used in the ALU design[3].This full adder is made by using total 18 transistors. According to them, the main specialty of this full adder is low power. In Fig.1diagramatic representation of design of full adder is shown.

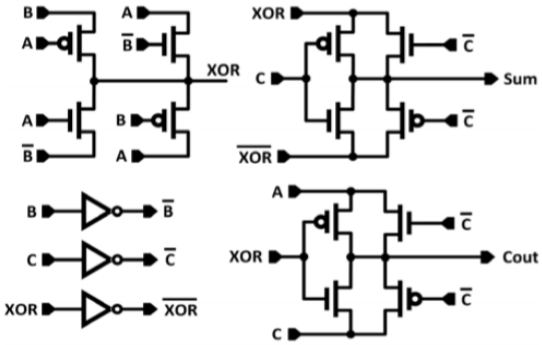

Fig. 1: 18T Full Adder [1]

B. *Logic Function Module*

Full adder cell is responsible for the creation *of* various logic functions. But if we are using this the overall delay will increase.so in order to reduce the delay of the circuitry we are using separate logic circuits. The designs of those logic are shown in Fig.2

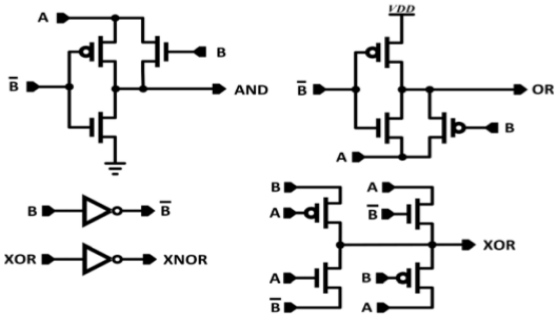

Fig. 2: Logic Block [1]

C. *Multiplexers*

Multiplexer selects the required data from any one of the many inputs and it sends the data to a unique output. Select lines are responsible for the selection of these inputs. Using full swing GDI technique here two multiplexers are designed.one is a 2x1 multiplexer and the other one is a 4x1 multiplexer [4],[5].

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The circuit diagram representation of 2x1 multiplexer is shown in Fig.3 and that of 4x1 multiplexer is shown Fig.4

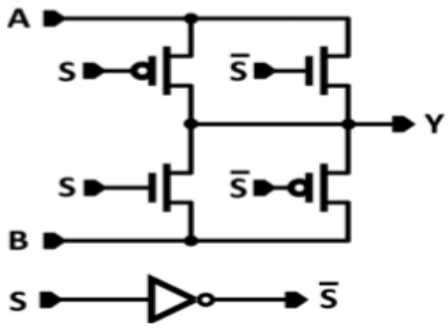

Fig. 3:2x1 Multiplexer using GDI [1]

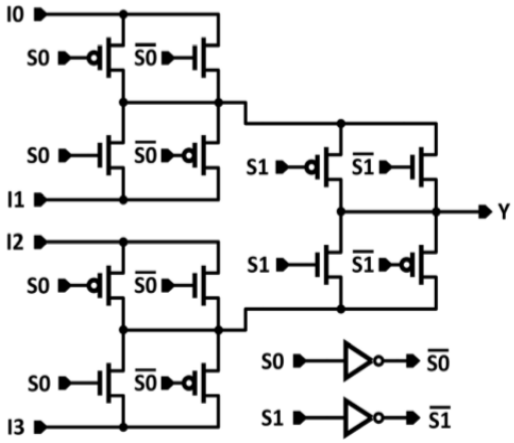

Fig. 4: 4x1 Multiplexer using GDI [1]

D. *Circuit implementation of 1-bit ALU*

A novel ALU is introduced. Full adder,2x1 multiplexer, logic block, an inverter and two 4x1 multiplexers are used to create this innovative ALU design. Diagrammatic representation is shown in Fig.5

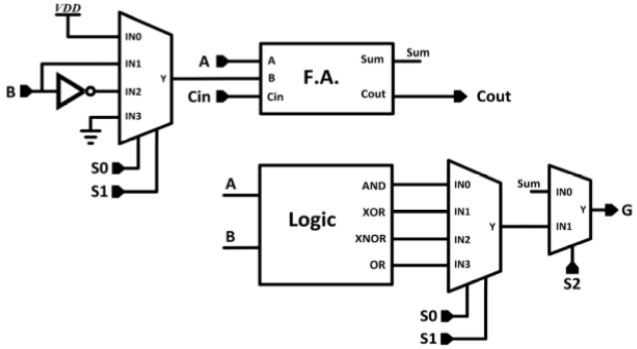

Fig. 5: 1- bit ALU [1]

Based on the data's from the select lines S0 and S1 the 4x1 multiplexer placed as first block operates the B operand such as logic 1 for decrement, B for addition, B´ for subtraction and logic 0 is selected for increment operation. It is done by inserting the out of first 4x1 multiplexer at B input of the full adder. The equation for calculation is given below

$$G=A+B+C_{in} \qquad (1)$$

In order to obtain the decrement operation, operand A is considered as G=A-1. Addition is obtained by simply adding the operands A and B and by keeping C_{in} as 0. Subtraction is done by adding A operand to 2's compliment of B operand. Increment was done by operand A is summed with C_{in}. according to S0 and S1 logic operations are selected by the remaining 4x1 multiplexer.to choose between arithmetic and logic operation 2x1 multiplexer is used. By analyzing the table which is shown below we can verify the operation of our ALU

TABLE I. Truth Table representation of operations of the 4-bit ALU

S0	S1	S2	Operation	ALU Functions
0	0	0	G=A-1	DECREMENT
0	0	1	G=A^B	AND
0	1	0	G=A+B´+1	SUBTRACTION
0	1	1	G=Ā	XNOR
1	0	0	G=A+B	ADDITION
1	0	1	G=A⊕B	XOR
1	1	0	G=A+1	INCREMENT
1	1	1	G=A∨B	OR

In order to obtain the 4-bit ALU design, one unit of 2x1 multiplexer and four modules od 1-bit ALU's are cascaded together.The circuit is shown below in Fig.6.

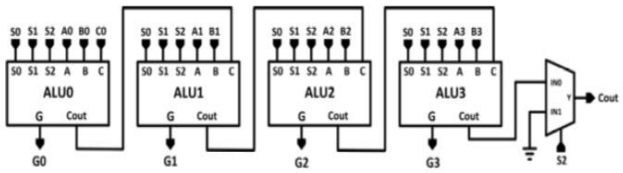

Fig. 6: 4-bit ALU design

II. PROPOSED 4-BIT ALU DESIGN

Full adder design has vital role in the design of an ALU. Due to this reason, in order to obtain a novel design for ALU the full adder module is replaced with a new 9T full adder and all the other modules are kept as the same.

A. *9T Full Adder*

To improve the performance of the ALU a newly introduced design of full adder is used. High speed, low power and lesser number of transistors are the main advantages of this full adder design. With the help of this novel architecture the ALU performance can be improved as per the requirements of today's industry [6],[7].

The full adder is divided into three modules. Module 1 and module 2 are XOR designs using Pass Transistor Logic. These two XOR modules will create the sum function. Module 3 is made up of GDI mux in order to provide the carry out of full adder [8],[9]. The main attraction of this full adder is less area since it has only 9 Transistors. This full adder design is used in the ALU block replacing the 18T full adder block. The diagrammatic representation is given in Fig. 7.

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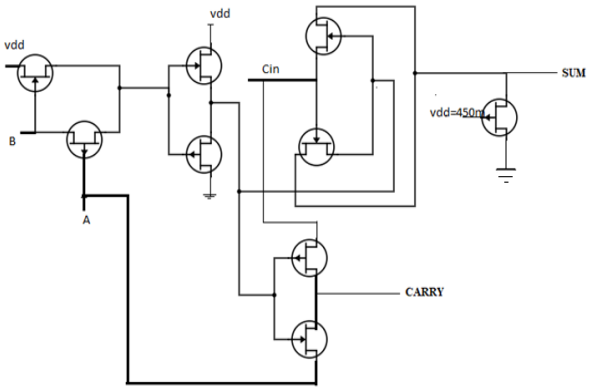

Fig. 7: New 9T full adder

Using this, the 1-bit ALU design is improved as shown in Fig. 8.

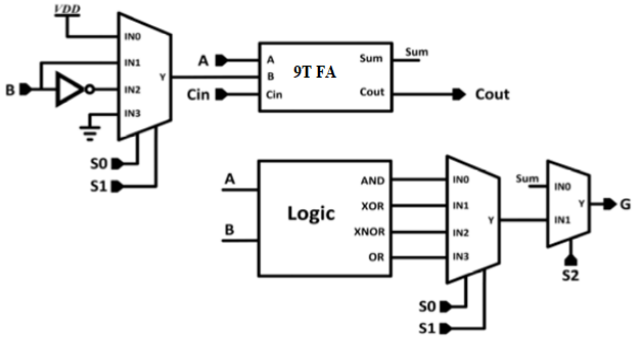

Fig. 8: Proposed 1-bit ALU

ALU design is improvised by using newly introduced full adder. Transistor count of the full adder is decreased from 18 to 9. This will result in less area and considerably low power.

4-bit ALU design is created by the use of 4 stages of 1-bit ALU design and it is compared and analyzed with the existing design for the measures of delay, power, transistor count &PDP.

III. SIMULATION RESULTS

The simulations were carried out using Cadence Virtuoso simulator with a power supply 1V. To analyze the design two test inputs are chose and they are A=1011 and B=1100.The newly introduced ALU design is analyzed and then it is compared with the existing ALU design proposed design. In Table II both the results are given.

Table II. Comparison of existing & proposed 4-bit ALU

DESIGN	DELAY (in ps)	POWER (in µW)	PDP (in fJ)	TOTAL NUMBER OF TRANSISTOR
Existing 4-bit ALU	77.517	22.19	1.72	220
Proposed 4-bit ALU	70.01	20.48	1.433	184

Newly introduced ALU's input wave form and output wave form are shown in below given Fig.

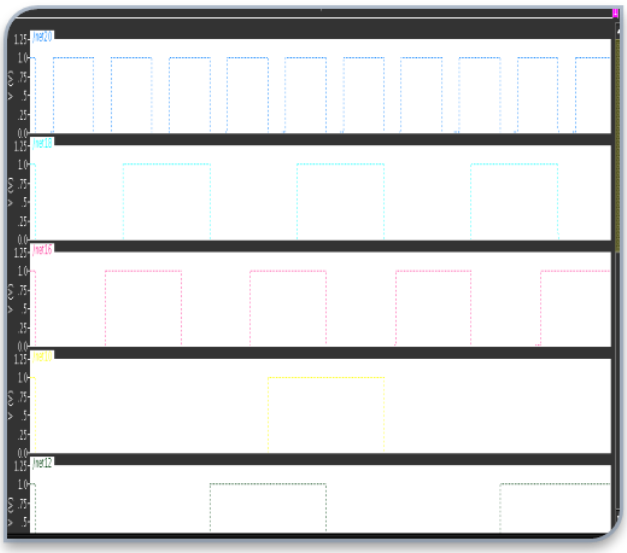

Fig. 9: Newly introduced 4-bit ALU's input transient response

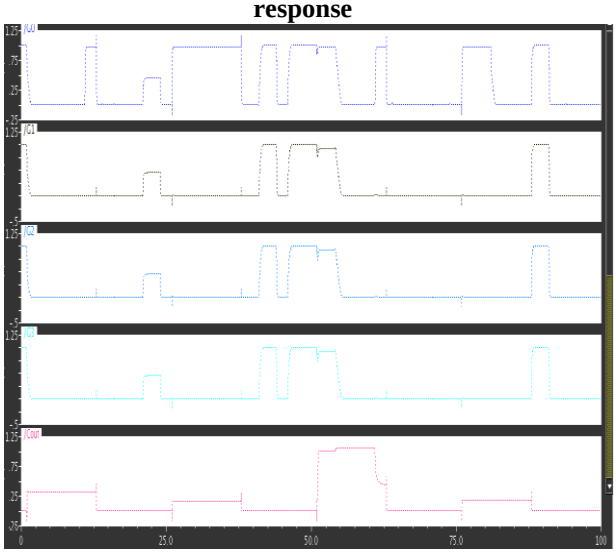

Fig. 10: Newly introduced 4-bit ALU's output transient response

IV. CONCLUSION

By verifying this design, we can say that delay, power, area and PDP are optimized. Delay is reduced by 10.17%. Power is reduced by 8.05%.PDP is reduced by 18.20% and transistor count is reduced by 17.82 %. Based on these results, we can conclude that this novel 4-bit ALU using newly introduced 9T full adder unit is highly recommended in case of less area, minimum power and fast VLSI designs.

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