Power-Efficient 32 Bit Adder-Subtractor with Integrated Logic Design and Leakage Mitigation Techniques

U.Palani1, G. Amuthavalli, R. Gunasundari

Abstract*: *The role of arithmetic circuits in all the signal processing units is of paramount importance and in which Adder-Subtractor circuit is indispensable. However, the increased transistor density in effect of technology miniaturization resulted in power dissipation or leakage. Since battery technology innovations cannot provide a better solution, circuit-level power-aware design is the ultimate choice of the design community. When high level processing units are involved with larger bit size circuits, adequate power is consumed and moreover, power dissipation completely squanders the static power. Hence, the key point to achieve low power solution at the design level is to reduce the design complexity and undesired consumption of power; for which a novel Integrated Logic Design (ILD) style and a novel Leakage Mitigation and Retention (LMR) technique are proposed. The proposed ILD and LMR design approaches are implemented in the design of 32 bit Adder-Subtractor circuit using Cadence 90nm technology node. The simulation result of the proposed circuit is compared with its conventional circuit and it is observed that the static power is reduced to nanowatt range from microwatts range. Thus, it is proved that the proposed 32 bit Adder-Subtractor is of power-efficient with its best low power design approaches.

Index Terms:*32 bit Adder-Subtractor, leakage,Power-efficient, Cadence. Gate Diffusion Input.*

I. INTRODUCTION

In the history of past decades, the number of transistors and switching speed were very low and necessity of low power design was not even in the design strategies. When miniaturization has become a trend more transistors are packed into a single chip and resulted in the issue of power dissipation or leakage. As the power consumption increases with increased power dissipation, the lifetime of the battery-powered applications become stringent. Since innovations in the battery technology cannot meet a better solution, power-aware design at the circuit-level become an ultimate choice of the designers.

Almost all the processing units of electronics and communication systems are indispensably depending on the arithmetic operations. Specifically, arithmetic circuits like adder and subtractor play a pivotal role in the arithmetic and logic unit [4] of optical domain [1], neural networks [11][16], digital signal processing [9], sensing applications [8][12], graphic applications [5], application specific integrated circuits (ASICs) [15][18], etc.,. The chip area is reduced nowadays by utilizing a single Adder-Subtractor circuit for both the addition and subtraction [6]. However, high level processing units with larger bit size circuits consume more power with lesser speed and larger area. Since there is a trade-off between power dissipation and speed, the conceptuality of power awareness in the design drive towards the low power circuits with better performance and speed [7]. The key point to achieve low power solution is to reduce the number of transistors and the design complexity with a desired logic design style. In addition, addressing of power dissipation or leakage with a leakage mitigation technique provides a complete power-efficient design.

In this communication, a structure of the work is organized as follows: Section 2 discussed the literature review of the Adder-Subtractor circuit implementation, logic design style and leakage mitigation, related works, problem statement and an introduction to proposed work. Section 3 discussed the proposed logic design style - leakage mitigation technique in detail. Section 4 presented the implementation of the proposed 32 bit Adder-Subtractor with the simulation results and its discussion. Section 5 concludes the work with future scope.

II. OVERVIEW

Basically, Adder-Subtractor is designed based on the designing of Boolean functions of the sum, carry, difference and borrow using Karnaugh map and implementing them using logic gates [6]. Different logic styles [14][17][19] have been investigated in the circuit to provide better performance, low power or high speed on different application and technology scenario. As leakage is the main cause of power scarcity, exhaustive study has been done from various literatures [3][10][20][21]; in which different leakage reduction techniques are presented with its own merits and demerits. Sharma et al [2] discussed about the design and analysis of 1 bit Full Subtractor using 120nm technology node for the area and power-efficient solution. Dhar et al [13] discussed the performance of Full Subtractor using Gate Diffusion Logic (GDI) in the context of energy-efficient, high speed and low power.

Manuscript published on 30 June 2019.
***** Correspondence Author (s)
U. Palani, Department of ECE, IFET College of Engineering, Tamil Nadu, India.
G. Amuthavalli, Department of ECE, Pondicherry Engineering College, Puducherry, India.
R. Gunasundari, Department of ECE, Pondicherry Engineering College, Puducherry, India.

Salimzadeh et al [14] discussed the reversible structure of Full Adder/Subtractor in the newer technology of quantum cellular automata.Rangarajanay et al [17]discussed the spin-based hybrid reconfigurable logic in the design of arithmetic circuits for power and area efficient applications. From the detailed review of the literatures and related works, it is understood that the limitations in the design of power-aware Adder-Subtractor are larger circuits with higher design complexity and the consequent high leakage power consumption.

III. PROPOSED INTEGRATED LOGIC DESIGN – LEAKAGE MITIGATION AND RETENTION (ILD-LMR) TECHNIQUE

According to this communication, the design of 32-bit Adder-Subtractor is solved with two design steps:

A. Logic Design

B. Leakage Mitigation.

The challenges in the logic design style is considered and proposed a novel logic style, called Integrated Logic Design (ILD). The leakage consumption is the greatest power squanderer at the active or sleep state of the circuits. The reduction of the leakage is accounted to include in the design and therefore novel Leakage Mitigation and Retention (LMR) technique is proposed. The 32 bit Adder-Subtractor is designed using Integrated Logic Design style with Leakage Mitigation and Retention technique and the better performance is achieved with low power consumption.

A. *Logic Design*

The logic design is basically identified by the transistor's orientation which mainly depend on the number of transistors involved, type of transistors used and the wiring complexity during the implementation of a particular logic function. Out of the two CMOS logic circuits (static and dynamic), the static CMOS circuit is considered in this paper. The literature review presented different logic design styles, such as static CMOS logic, pass transistor logic, performance and speed based logic, speed and power based logic, performance and low power based logic, transmission gate logic, gate diffusion input logic and hybrid logic styles. In spite of all the logic styles with its own merits and demerits, a novel logic style called Integrated Logic Design (ILD) style is proposed.

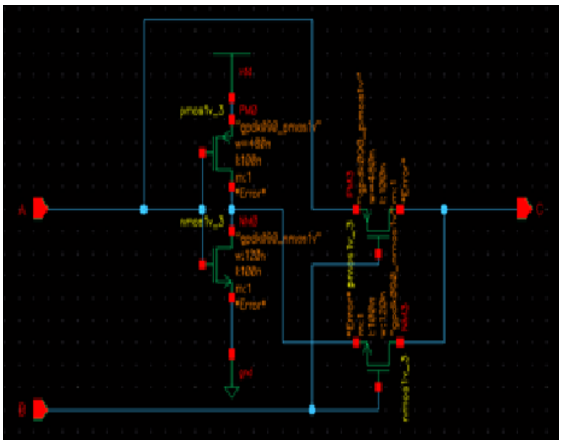
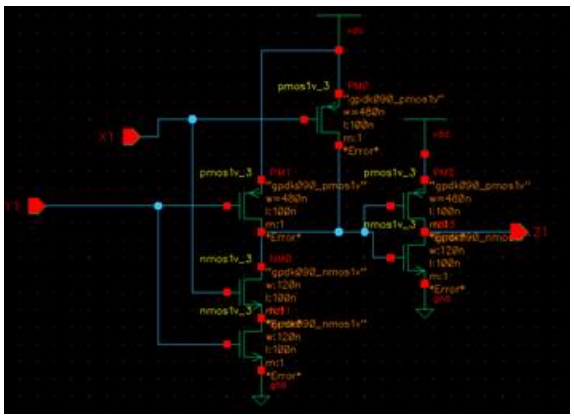
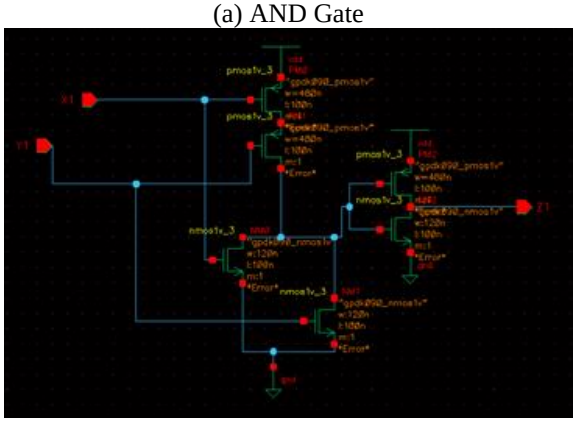


Fig. 1 EXOR gate using GDI logic

In this ILD style, the benefits of two logic styles are considered and integrated them without any compromise in the performance and speed of the circuit. Since the necessity of the design is the reduced size, Gate Diffusion Input (GDI) logic is used. But the reduced driving capability of the gates is tackled by exploiting GDI for the implementation of only complex logic function like EX-OR as in Figure 1. In order to provide full swing driving capability, simple logic functions are implemented using static CMOS logic style as in Figures 2 (a) and (b).Hence, GDI logic and static CMOS logic are integrated in the implementation of the logic function of 32-bit Adder-Subtractor to provide the desired performance.



(a) AND Gate



(b) OR Gate

Fig. 2 Logic gates using static CMOS logic

B. *Leakage Mitigation*

Low power consumption or increased lifetime is achieved by using hardware or software approaches. Hardware approaches focus on utilizing high power sources or renewable energy sources, which are solely an alternate solution, but not a proper solution to achieve low power. In the software approaches, the circuit is made to sleep whenever not needed. In these approaches, the concealed problem is the leakage consumption, which is the greatest power squanderer of static power. Practically, zero leakage is impossible and therefore leakage mitigation is the only and an exact solution to achieve utmost near-zero leakage consumption.

Hence, a novel, Leakage Mitigation and Retention (LMR) technique is proposed. The main function of this technique is to reduce the leakage consumption whenever the circuit is in sleep state and the previous data can be held and the circuit can even retrieve it after returning to the active state.

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Since the LMR technique is activated during sleep state and the logic of the circuit is to be undisturbed, the design of the technique is done with two levels of threshold voltage transistors: High Threshold Transistors (HTT) and Low Threshold Transistors (LTT). The LMR module as given in Figure 3 has three transistor units, which are Leakage MitigatorA (LM_A), Leakage Mitigator B (LM_B) and Data Retainer (DR).

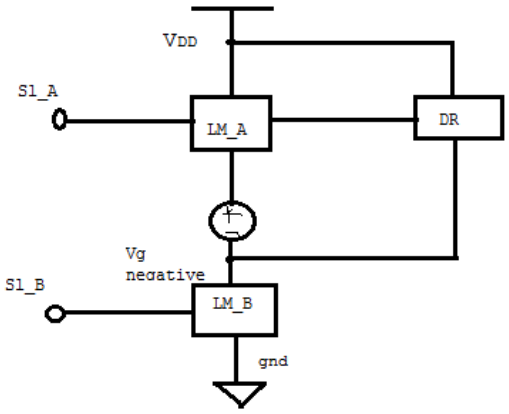

Fig. 3 Leakage mitigation and retention technique

The Leakage Mitigator and Data Retainer are designed using HTTs and are connected between power supply rails of the circuit. The sleep signals sl_A and sl_B are used to turn ON and OFF the LMs during the sleep or active state of the circuit.

With reference to the previous work [3], whenever the LM_A is activated, the drain-current through it is expressed as in Equation (1):

$$I_{ds(lm)} \cong \mu C_{ox} \left(\frac{W_{lm}}{L}\right)\left(V_{dd} - V_{th\_lm}\right)V_{ds(lm)} \quad (1)$$

Where, μ is the electron/hole mobility; Cox is the Oxide capacitance; L is the length of the LM transistor; Vth_lm is the threshold voltage of LM transistor; Vdd is the supply voltage; Wlm is the width of the LM transistor; Vds(lm) is the drain-to-source voltage of LM transistor, which is given in Equation (2) as:

$$V_{ds(lm)} = K\left[\frac{I_{ds(lm)}}{W_{lm}}\right] \quad (2)$$

Where, K is experimentally derived from the Equation (3) as:

$$K = \frac{L}{\mu} C_{ox}\left(V_{dd} - V_{th\_lm}\right) \quad (3)$$

Whenever the sleep signal activates the LMs, the logic circuit of 32-bit Adder-Subtractor is power gated and the changes in the supply voltage reduce the leakage of the OFF transistor. Then it is impacted on the second order effects of the transistors and influence the overall power consumption. Also, the gate voltage of the LM_B controls the voltage at the virtual ground terminal Vg and is expressed as an Equation (4):

$$V_g' = V_{G(lm\_B)} + S\log_{10}\left[\frac{W_{Adder-sub}}{W_{lm\_B}}\right] + \frac{\left(V_{th(lm\_B)} - V_{th(Adder-Sub)}\right) + \eta V_{dd}}{2\eta} \quad (4)$$

Since the gate of DR is connected to negative Vg', the DR is operated always in OFF state and the previous output voltage is appeared as drain-to-source voltage of DR, thus the data is retained during sleep state & retrieved by the circuit at this active state.

IV. RESULT AND DISCUSSION

The proposed ILD style and LMR technique are employed and designed 32-bit adder subtractor using Cadence Schematic Editor 90nm technology nodes as in Figure 4. The supply voltage of 1V and nominal temperature of 27°C are considered and simulated the circuit using Cadence Spectre. The static power consumption is observed for conventional and the proposed 32-bit Adder-Subtractor as in Table 1.

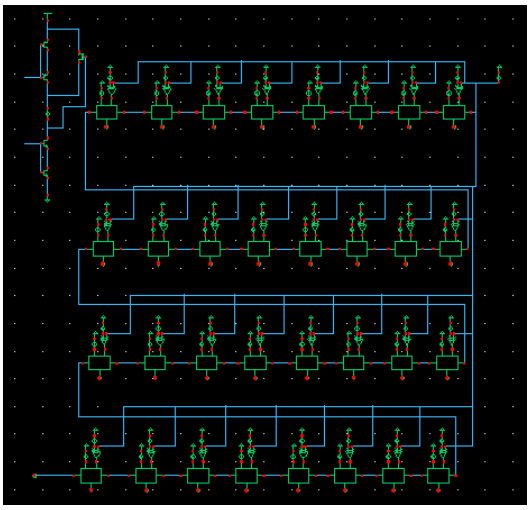

Fig. 4 Power-efficient 32 bit Adder-Subtractor

The conventional circuit of 32-bit Adder-Subtractor is designed and simulated using the same simulation environment. From the results, it is clearly understood that the large complex design of the circuit without leakage mitigation, consumes high static power (in microwatt range). The proposed 32-bit Adder-Subtractor with integrated logic design style and leakage mitigation and retention technique overcome the design constraints and challenges with a substantial reduction in static power consumption from microwatt to nanowatts range.

Table 1 Performance Analysis

32-bit Adder-Subtractor	Static Power
Conventional circuit (without any leakage reduction technique)	69.143 μW
Circuit with proposed ILD-LMR technique	50.51nW

V. CONCLUSION

The arithmetic circuits like Adder-Subtractor are in part of all the processing units of any targeted application. In the high-end processing units, the large size of the circuit and the high design complexity increases the power consumption of the circuit.

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Since power-aware design is of the ultimate goal of the design community, this paper proposed a technique called Integrated Logic Design - Leakage Mitigation and Retention (ILD-LMR) technique. In this technique, the ILD style reduced the size and complexity of the circuit and also the impact of secondary effects of the OFF transistor is mitigated and the leakage is reduced by the LMR technique. This ILD-LMR technique is proposed to design power-efficient 32-bit Adder-Subtractor. On comparing the performance of the proposed ILD-LMR design of 32-bit Adder-Subtractor with its conventional circuit (without any power reduction technique); it is clearly proved that the leakage is significantly reduced and low static power consumption is greatly achieved from microwatt range to nanowatts range. Thus, the proposed 32-bit Adder-Subtractor with integrated logic design and leakage mitigation technique is of power-efficient and is proven best low power design circuit and it will be implemented in other arithmetic and logic circuits to test its performance enhancement in the application-based processing units.

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AUTHORS PROFILE

U. Palani obtained his Diploma degree in Electrical and Electronics Engineering from DOTE-Tamil Nadu, Bachelor's degree in Electronics and Communication Engineering from University of Madras, Chennai and his Master's degree in Applied Electronics from Vinayaga Mission's University, Salem. He received his Ph.D., in Wireless Sensor Networks from Annamalai University, Chidambaram. He has 6 years of research experience out of 18 years of teaching experience. He is currently working as Professor in the Department of Electronics and Communication Engineering, IFET College of Engineering, Villupuram. His specializations include Digital Electronics, Sensor Networks, Internet Security and Computer Networks. His current research interest is Data Gathering in Wireless Sensor Networks. He is a Member of CSI. He is a Member of IEEE. He is a Life Member of ISTE, He is a Fellow, Institution of Engineers (India) and Member of International Association of Engineers.

G. Amuthavalli obtained her Bachelor's degree in Electronics and Communication Engineering from Madras University, Chennai and her Master's degree in Electronics and Communication Engineering from Pondicherry University, Puducherry. She received her Ph.D. in Low power VLSI design from Pondicherry Engineering College, Puducherry. She has 6 years of research experience and 9 years of teaching experience. Her specialization includes VLSI Design, Wireless Sensor Networks, Digital Electronics, Electronic Circuits and Embedded System. She is a Life Member of ISTE, She is a Fellow, Institution of Engineers (India) and Member of International Association of Engineers.

R. Gunasundari received her Ph.D degree in the faculty of Information and Communication Engineering, College of Engineering, Anna University, Chennai under the AICTE Quality Improvement Programme in 2009. She completed B.Tech degree and M.Tech degree in Electronics and communication engineering from Pondicherry Engineering College, Pondicherry. She has 20 years of teaching and research experience. Presently she is working as Professor in the Department of Electronics and Communication Engineering, Pondicherry Engineering College, Pondicherry. Prior to joining as faculty in Pondicherry Engineering College, she served as Scientist Engineer – C at ISRO satellite center, Bangalore. She has published more than 80 papers in reputed International/ National Journals and Conferences. Her areas of interest include mobile computing, wireless sensor networks and wireless communication networks.