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Thermal Effects and Stability of Cylindrical Surrounding Double-Gate (CSDG) MOSFET

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Abstract: This research work analyzes the thermal resistance in the CSDG MOSFET to realize the effect of thermal heat on the drain current, transconductance, and other parameters along a range of temperature of 0 – 300 K. This analysis has been verified through numerical simulation to determine the variation between the parameters and temperature. Thereafter, the thermal noise in CSDG MOSFET has been scrutinized with comparison to other MOSFETs. Finally, the temperature sensitivity of this device will be used to explore how the thermal stability can be ensured in the proposed CSDG MOSFET to affect its reliability and improved performance.

***Index Terms*: CSDG MOSFET, Nanotechnology, Thermal resistance, Thermal stability, Transconductance, VLSI.**

I. INTRODUCTION

The Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) is a basic semiconductor device in the production of Very Large Scale Integrated (VLSI) circuits. Its characteristics of simple structure, low power consumption and economical fabrication have facilitated its application in the design of portable electronic devices [1, 2]. However, despite the peculiarity and reliability of this device, temperature change affects its features and tends to reduce its functionality. When the temperature is increased or reduced beyond the tolerance, the total energy from the molecular motion of the carrier in MOSFET is affected and the required speed and functionality becomes unattained. Inability to adequately manage the effect of temperature change often leads to thermal runaway, caused by recycling of increased temperature with leakage current, which have unstable consequences on the MOSFET [3-5].

When the temperature of the MOSFET is increased at high voltage supply, the drain saturation current as well as switching speed is reduced [6]. Likewise, exposure to cryogenic temperature results in the increase in device transconductance and reduction of series resistance, this explicate a better dynamic performance. More so, the reduced temperature produces a reduced sub-threshold current and slope that translate to reduced power consumption [7, 8]. These advantages at lower temperature come at the cost of reduced reliability and performance of the device. Nevertheless, shortcoming nullifies the advantages and makes thermal effect a concern to manage [9].

Bresson et. al. [10] have investigated the thermal conductivity in *65 nm* channel length of a SiO_2 buried oxide (BOX) MOSFET. In that research work, high-*k* dielectric materials such as Al_2O_3 and diamond were compared with the default SiO_2. Also, low-*k* dielectric materials, like air was compared with the SiO_2.

The thermal conductance was analyzed after generating an equivalent thermal resistance circuit, where it was discovered that replacing the conventional BOX with diamond (which is of thermal conductivity $800\ Wm^{-1}k^{-1}$) or manageable with Al_2O_3 and AlN (of $20\ Wm^{-1}k^{-1}$ and $5\ Wm^{-1}k^{-1}$ thermal conductivities respectively). However, this thermal sensitivity comes with an increased short channel effect. *Devrani and Srivastava* [11] have analyzed the advancement of MOSFET with the application of Hafnium [11]. *Ball* [12] proposed a way of overcoming the thermal challenges in MOSFET by introducing a monolithic approach of integrating a controller with MOSFET to detect when the device is heated and needed to be protected. This approach is appreciable except that it will substitute for the reliability of the MOSFET. In order to manage the thermal effect and improve the performance of the MOSFET in application, multiple gates transistors was introduced [13-15]. The multiple gates created have more controls over the channels which produces good current per unit width with low leakage current [16]. The effect of heat with this improvement have however been a challenge that has been discussed with different models and proposal being introduced to adequately manage the problem at hand.

However, this improvement was not enough to curtail the effect of heat on the functionality of the MOSFET device, this brought about the introduction of a new structure in Cylindrical Surrounding Double-Gate (CSDG) MOSFET [17, 18] This structure shown in Fig. 1 is with the understanding of the thermal effect on MOSFET and how to fabricate a structure that best overcome this effect.

The cylindrical structure is used to overcome the corner effect from the carrier mobility [19]. Also, with the cylindrical structure, the device has little body contact with the IC board. The external gate of the device has little contact with the board, and it generate little heat that could be overcome with the help of a heat sink. Likewise, the parameters of the device is carefully considered with specifications of channel lengths = *20 nm*, internal radius = *5 nm*, external radius = *10 nm*, oxide thickness = *2 nm* and work function = *4.5 eV*.

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This paper is organized as follows. The thermal resistances available in CSDG MOSFET have been described in the section II. Thermal effects on the parameters of CSDG MOSFET have been analyzed in section III. The thermal noise generated in the CSDG MOSFET has been discussed in the Section IV. The Section V explain how thermal stability can be achieved using the CSDG MOSFET. Finally, Section VI concludes the work and recommends the future aspects.

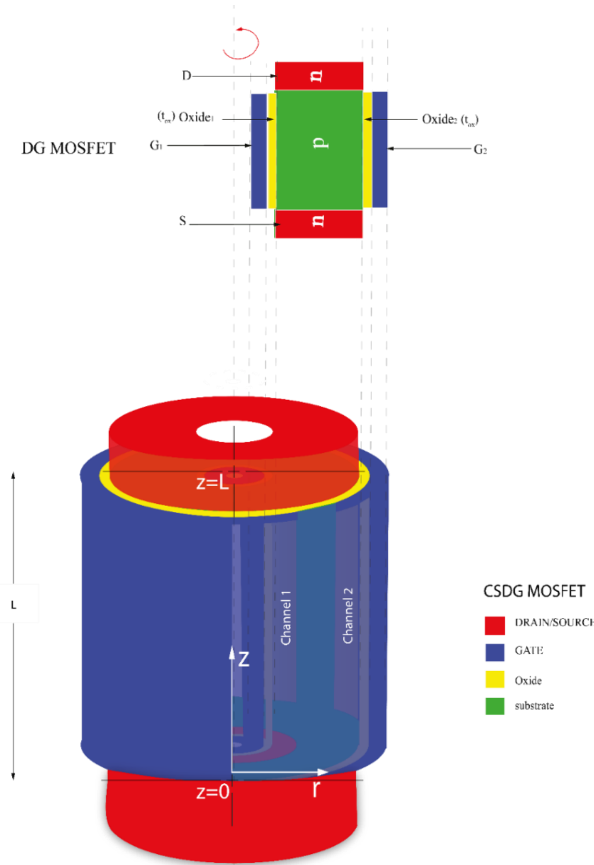

Fig. 1: A 2-D diagram of the n-channel CSDG MOSFET [20].

II. THERMAL RESISTANCES IN CSDG MOSFET

These reviewed models for managing heat effect and their drawback are used to analyze the equivalent thermal resistance for the CSDG MOSFET [21]. The internal and external cylindrical parts of the CSDG MOSFET have been considered with negligible gate thermal resistance ($R_{\Theta G}$) along the power of both frames. The equivalent resistance circuit has been modelled with the consideration of a shared resistance of the source and drain along the two channels with no or little consideration of body of the CSDG MOSFET as shown in Fig. 2.

$$R_{\theta_{internal}} = R_{\theta_{(S1)}} + R_{\theta_{(CH1)}} + R_{\theta_{(D1)}} \quad (1)$$

$$R_{\theta_{external}} = R_{\theta_{(S2)}} + R_{\theta_{(CH2)}} + R_{\theta_{(D2)}} \quad (2)$$

Since the internal and external cylindrical parts are in parallel, the total thermal resistance in this CSDG MOSFET is expressed as:

$$R_{\theta_{CSDG}} = \frac{\left[\left(R_{\theta_{s1}} + R_{\theta_{CH1}} + R_{\theta_{D1}}\right)\left(R_{\theta_{s2}} + R_{\theta_{CH2}} + R_{\theta_{D2}}\right)\right]}{\left[\left(R_{\theta_{s1}} + R_{\theta_{CH1}} + R_{\theta_{D1}}\right) + \left(R_{\theta_{s2}} + R_{\theta_{CH2}} + R_{\theta_{D2}}\right)\right]} \quad (3)$$

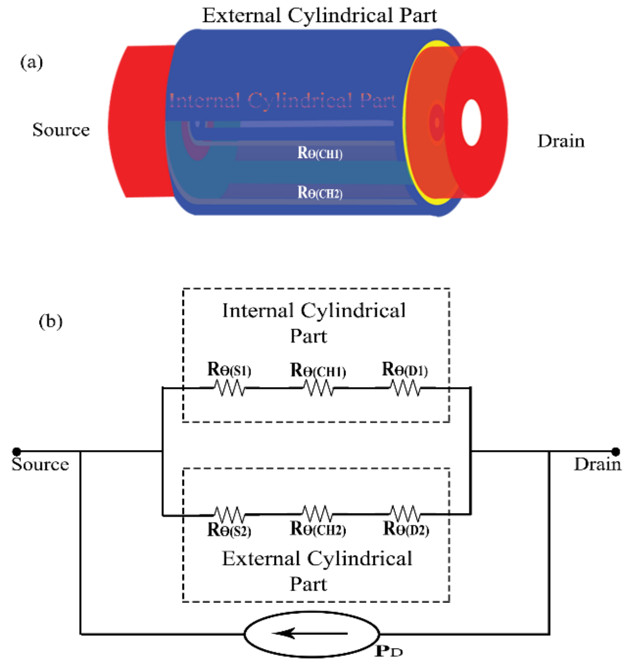

Fig. 2: (a) Simplified diagram of n-channel CSDG MOSFET and (b) its Equivalent resistive model.

From this analysis, the parallel connections of the CSDG MOSFET help reduce thermal resistance. The thermal resistance is reduced in the CSDG compared to other reviewed MOSFET. This will be helpful in the application of the CSDG MOSFET in nanotechnology.

III. THERMAL NOISE IN CSDG MOSFET

Due to the shrinking of the MOSFET to achieve better performance in application, the thermal noise in the device becomes more pronounced [22, 23]. Although, it is always predicted that thermal noise in short-channel MOSFET is higher than the high-channel MOSFET, this can be true but not with excess factor [24, 25]. With the factor of channel length and rise in temperature in the CSDG MOSFET, the agitation along the channels become noticeable even at zero applied gate-voltages ($V_{GS1} = V_{GS2} = 0$).

Thermal noise in the CSDG MOSFET is expected to be conspicuous due to its nanoscale region of operation and the double channel it possesses. However, a proposed model to reduce the thermal noise in the CSDG MOSFET is being introduced. Observing the charged-based proposal for Power Spectrum Density (PSD) at gradual channel approximation of the thermal noise in MOSFET given as [26-30]:

$$\delta_{id} = \frac{4kT\mu q}{L^2} \quad (4)$$

where T and μ are the temperature and charge carrier mobility along the channel respectively, while Q_{ch} and L are the total charges along the channel and length of the channel. Although Eq. (4) was modelled for long channel MOSFET, but it was discovered that its effect can be used to reduce the short channel effect through increased transconductance value which CSDG MOSFET possesses. Eq. (4) is valid if the drift current has little or no effect on the charge transport along the channels of the CSDG MOSFET. However, the diffusive random current has large effect on the transport of the charges causing a significant effect on the thermal noise generated in the CSDG MOSFET. Since the thermal noise is dominant at the linear (ohmic) region of the CSDG MOSGET, this region will be used to analyze the thermal noise of the device.

Likewise, short channel separations in CSDG MOSFET cannot be possibly seen as a resistance, due to degradation of carrier mobility by lateral generation of the electric field [31], because of this condition, the thermal noise will be considered at the gradual channel region. Considering of the channels in the CSDG MOSFET with respect to the dominance of the diffusive random current, the thermal noise can be given as:

$$\delta i_n^{\,2} = 4nq^2 D\Delta f \frac{W}{L} \quad (5)$$

where n and D are the carrier density and diffusion constant, respectively and Δf and W are the band width measurement and width of the channel, respectively. Due to the degraded carrier mobility effect, the drain current can be calculated as:

$$I_d = \mu n W q(V)\frac{\partial V}{\partial L} \Bigg/ \left(1 + \frac{\partial V / \partial L}{E_C}\right) \quad (6)$$

The E_C is the critical electric field at the point where the carrier velocity will become saturated. The Eq. (6) can be integrated with respect to applied voltage along the channels from the source to the drain and the noise of the noise can be expressed as:

$$\Delta I_d = \delta i_n \frac{\mu n W q(V)\Delta V}{L + \frac{V_{DS}}{E_C}} \quad (7)$$

where $\mu nWq(V)$ represent the product of mobility, number of charges, charges along the channel and width of the channel with respect to the applied voltages at the gates of the CSDG MOSFET. Therefore, the two channels of the CSDG MOSFET can be expressed as:

$$i_{dn}^{\,2} = \sum\left[\Delta I_d\right]^2 \quad (8)$$

Substituting Eq. (5) and Eq. (7) into Eq. (8) gives:

$$i_{dn} = \sum 4nq^2 D\Delta f \frac{W}{L} \cdot \frac{g_{th}\Delta V^2}{\left(L + \frac{V_{DS}}{E_C}\right)^2} \quad (9)$$

It has been observed that thermal noise current in CSDG MOSFET is higher due to the carrier heating effect examined with the gradual channel approximation. This fact helps to appreciate the application of the device in Nanotechnology. The resulting model shows the importance of the carrier heat effect at gradual channel region with voltage biasing almost at V_{DS}. This shows a greater and more influential thermal noise drain current at higher applied voltage.

IV. THERMAL EFFECT ON THE PARAMETERS OF CSDG MOSFET

Generally, MOSFETs are temperature dependent devices. This implies that temperature is a main contender in the efficiency and performance analysis of the device [30, 31]. Self-heating in the device affect its proposed environment and affect the performance and reliability of the device. Our improved CSDG MOSFET is modelled with this factor in view. The structure is cylindrical in order to have little contact with the board and generate less heat.

In this section, the CSDG MOSFET is analyzed using its parameters such as drain current, transconductance, and carrier mobility to determine its temperature dependence. This analysis has been performed using mathematical modelling of its parameters at various temperature range. The impact on these parameters and how it influences the overall performance of the CSDG MOSFET will also be discussed.

A. Thermal effect on Drain current

Increase in the temperature has a consequential effect on the carrier mobility which in turn affects the drain current. To examine the movement of electron along the channels of the CSDG MOSFET, the drift-diffusion approach comes with the limitation of scattering for previous MOSFETs. But for the CSDG MOSFET, it is established that the channels are undoped and most scattering mechanism are insignificant except for electron-electron collision which is not considered in detail in this work.

When the temperature in MOSFET is increased, the drift current is increased such that with the application of voltage at both gates of the CSDG MOSFET, electric field is generated along the formed channels which excite the electrons. However, with this increase in temperature, the charge carrier accelerates at increased speed but with further increase in the temperature, the carrier mobility is reduced. This is due to the increasing collision of the electrons along the cylindrical channels which affect the express movement of the electron from the source to the drain. Recall that drift velocity (v_d) is proportional to the carrier mobility (μ) expressed as [28-30]:

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$$v_d = \mu E \quad (10)$$

When the mobility is increased, the drift velocity increases but, with further increased in temperature, the mobility of the carrier charges is constrain due to collision which result to reduced drift velocity. With the cylindrical structure of the CSDG MOSFE, the drift current, which is a function of the drift velocity is also affected such that:

$$I_{drift} = \frac{nq\mu 2\pi(a+b)V}{L} \quad (11)$$

With the increased temperature, the number of charges (n), the voltage applied (V) and the channel length (L) are kept constant, the mobility (μ) becomes a factor that affect the drift current. When the mobility is appreciable, the drift current is increased and vice versa. Also, the diffusion current is proportional to the cross-sectional area of the CSDG MOSFET due to the movement of the electrons from higher concentration to lower concentration along the channel. Therefore, diffusion current is:

$$I = Dq\pi(a+b)^2 \left[-\frac{dn}{dL} \right] \quad (12)$$

where D is the diffusion constant which is the product of the carrier mobility and thermal voltage (Φ_t), that is:

$$D = \mu \Phi_t \quad (13)$$

$$\Phi_t = \frac{kT}{q} \quad (14)$$

where k is the Boltzmann constant and T is the temperature.

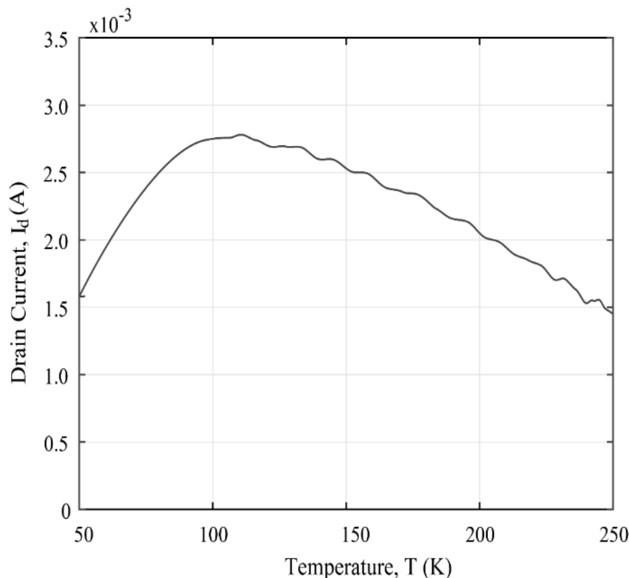

Fig. 3: The variation of the drain current (I_d) of the CSDG MOSFET with range of temperature (K).

The increase in temperature is supposed to bring a logical increase in the diffusion current, but for the electron-electron collision, which tends to obstruct the express movement of electrons when the temperature is increased above tolerance.

The drift-diffusion model is further verified in simulation with V_{GS} =*0.3 V* at different temperature to find the drain current in Fig. 3. In Fig. 3, it is observed that as the temperature increases, the drain current also increases. This shows the reliability of the CSDG MOSFET at cryogenic temperature.

B. Thermal effect on Transconductance

From the analysis of the drain current with temperature, the transconductance of the CSDG MOSFET can also be analyzed. This is possible because the transconductance is the ratio of the drain current to the gate-source voltage. From the Eq. (5) and Eq. (6), differentiating the drain current (I_D) w.r.t. the gate-source voltage (V_{GS}) at constant drain-source voltage (V_{DS}) explains the transconductance.

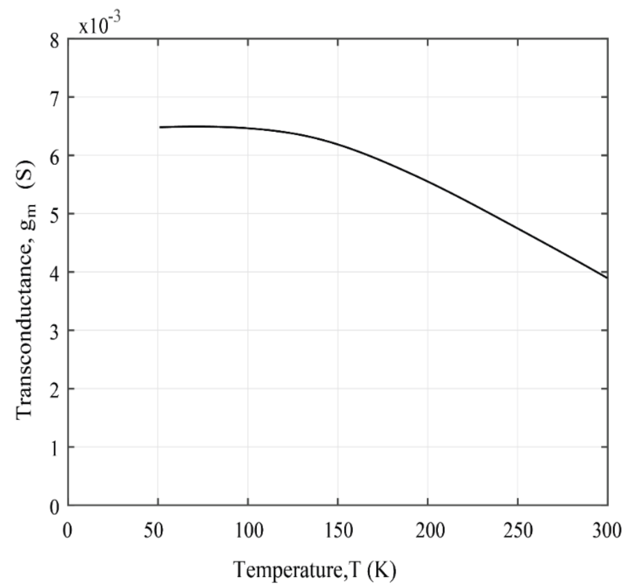

Fig. 4: Variation of transconductance of the CSDG MOSFET with temperature range to measure effectiveness.

The transconductance is verified by simulation with the parameters used. It is discovered that since the saturation current increases with decreased temperature, so it is expected from transconductance. From Fig. 4, it has been observed that transconductance is steady with temperature change until little above *100 K*, where it begins to fall gradually. Between *100 K* and *150 K*, the decline isn't too obvious but beyond *150 K*, the decline in the transconductance becomes noticeable. This shows that the effectiveness of the CSDG MOSFET can be measured at temperature less than *100 K*, but above *150 K*, the device becomes not too reliable. However, to avoid this, some precautionary measure will be considered in further sections.

C. Thermal effect on Carrier mobility

The motion of the electrons along the conducting channels and how it is affected by temperature explains the mobility.

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As higher the electron motion in the conducting channels of CSDG MOSFET, efficiency of the device will be better. Factors that affect the carrier mobility in the CSDG MOSFET are the electric field, scattering mechanism, temperature among others. Electric field is generated from the gate-source voltages (V_{GS}) applied at the two gates of the CSDG MOSFET.

Since the CSDG MOSFET is characterized by lower threshold voltage, the applied V_{GS} help the electron mobility to increase until a saturation point is reached where the drain current becomes steady.

In the design of this improved structure, carrier mobility has been considered and it reflects in the undoped property of the conducting channels, and the channel lengths not extensive like previous structure.

With the undoped channel length, various scattering mechanism become negligible due to lack of impurity doping. However, the electron-electron collision is a scattering mechanism to consider. Also, another factor that affect electron mobility to be considered is the temperature. In the CSDG MOSFET, it has been discovered that at a cryogenic situation, the drift current increase with increase in temperature. This also increases the carrier mobility from the relationship established in [20, 29, 30].

$$E = \frac{\lambda(a+b)}{2\pi ab\varepsilon_0} \quad (15)$$

$$\mu = \frac{2\pi\varepsilon_o}{\lambda}\left[\frac{ab}{a+b}\right]v_{d_{CSDG}} \quad (16)$$

$$\mu = \frac{2\pi\varepsilon_o}{\lambda T}\left[\frac{ab}{a+b}\right]v_{d_{CSDG}} \quad (17)$$

where E and λ are the electric field and electron per unit, a and b are the internal and external radii and ε_0 and v_d are the permittivity and drift velocity, respectively.

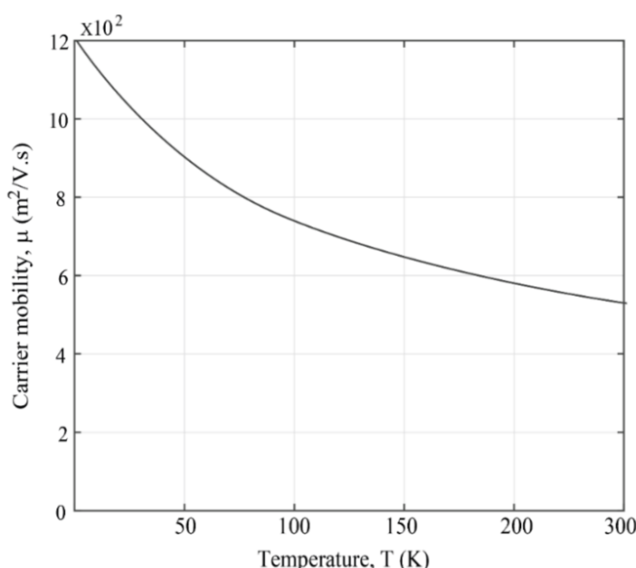

Fig. 5: Variation of Carrier mobility of CSDG MOSFET with temperature.

However, the drift velocity increases until the temperature attains the point where electron to electron collision becomes very significant, making electron mobility to reduce as the temperature increases. This has been verified in Fig. 5.

It has been observed from Fig. 5 that the carrier mobility in the CSDG MOSFET is inversely proportional to temperature and as such the carrier mobility increases as the temperature decreases. This can be attributed to the modality in the radius of the device, because as the radius decreases, the electron mobility when temperature rise is increased. This increase in mobility cause collision among the electrons, making mobility to decline and by extension affects other parameters. The CSDG MOSFET possessive an adaptive temperature ability, however the temperature should not be increased beyond *100* ^0C as it affects the reliability of the device and damage the device in the process.

V. THERMAL STABILITY IN CSDG MOSFET

Thermal instability is a phenomenon experienced from the application of MOSFET in electronic circuitry. It was discovered that beyond its Safe Operating Area (SOA), the device becomes unstable and unreliable due to the internal and external heat influences on it [34]. Internal heat influences due to the stuffing of many passive devices into a chip and external heat influence due to MOSFET contact with its surrounding and impact of temperature changes experienced. The CSDG MOSFET has been analyzed with respect to temperature, however it is a necessity to get thermal stability of the device. This MOSFET is made of millions of passive devices stuffed in it. This could also cause internal thermal instability in the device. Also, another cause of instability is the external heat generated from the surrounding of the device.

Another proposed a way of overcoming the thermal challenges in MOSFET by introducing a monolithic approach by integrating a controller with MOSFET to detect when the device is heated and needed to be protected [12]. This approach is appreciable except that it will substitute for the reliability of the MOSFET. In the novel CSDG MOSFET, this approach is not applied but an appropriate approach from the architectural fabrication of the device. The thermal challenge has been combated a bit in the proposed improved CSDG MOSFET structure. To limit the internal heating in the device, a hollow which is determined by the radius of the internal structure analyzed as seen in Fig. 1. This is fabricated to allow air, a substance of very low thermal conductivity to flow through the device, in turn reducing the effect of the internal heating generated by the device. This is one of the improvements that the previous propose structure did not include.

The external heating is also limited by the cylindrical structure of the CSDG MOSFET, which has little contact with the board it is mounted upon. The part of the device in contact with the board is the external gate and the heat effect of this contact can be eliminated with the involvement of a heat sink on the board it is mounted. Also, to analyze if the circuitry in which the CSDG MOSFET is employed can be functional without the heat sink, the power dissipated can be calculated as:

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$$P_{max} = R_{\theta_{CSDG}} * I^2 \quad (18)$$

The maximum power the CSDG MOSFET can dissipate can also be calculated as:

$$P_D = \frac{(T_{max} - T_{amb})}{R_{\theta_{CSDG}}} \quad (19)$$

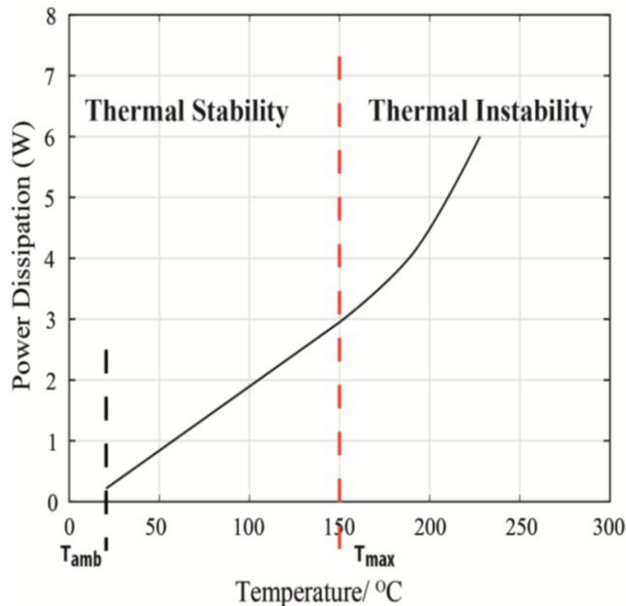

Fig. 6: Power dissipated in the CSDG MOSFET with respect to temperature changes.

where T_{max} is the maximum temperature the CSDG MOSFET can adapt to (range of *100 K – 150 K*), $T_{amb.}$ is the ambient temperature (about *25 K*) and $R_{\Theta(CSDG)}$ is the thermal resistance of the CSDG MOSFET. The heat sink can be ignored for the CSDG MOSFET when the dissipated Power (P_D) is less than the maximum power dissipated (P_{max}) as illustrated in the equations. However, almost at the Tmax, the stability of the CSDG MOSFET is compromise and cause great havoc to the board it is mounted on, however, this is still temperature accommodative compared to the other MOSFET types.

VI. CONCLUSION AND FUTURE ASPECTS

In this research work, the effect of heat on the CSDG MOSFET is presented. The CSDG MOSFET was analyzed under the influence of temperature change during its utilization. To achieve this, the thermal resistance was first modelled, and a reduced thermal resistance was derived. This model yield a reduced thermal resistance in the CSDG MOSFET. The thermal effect on the parameters of the CSDG MOSFET was then analyzed with a verification of the suitable temperature that the CSDG MOSFET is best used. The noise generated due to the heat has been a bit complex to analyzed, but this research work has been able to develop a physics-based model for drain thermal noise current with carrier heat effect consideration and some suggested possible ways to stabilize the thermal effect on the CSDG MOSFET explained.

The CSDG MOSFET has been an improved device in the nanotechnology and VLSI application and it has the capability to withstand the internal and external heat generated in the process.

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