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Implementation of High Performance 2D Transform using Area Efficient Even Odd Decomposition Methodology for Future Video Coding

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***Abstract*: *Future Video Coding(F.V.C),High Efficiency Video Coding(H.E.V.C) are international image compression standards developed by ITU,ISO,JPEG organizations to produce better compression factor at an expense of high computational complexity.FVC has higher computational complexity and resource utilization compared to HEVC, H.264 standards.FVC utilizes various DCT algorithms for image compression and various IDCT algorithms for image reconstruction. This paper presents an approach for Hardware implementation of 8X8 DCT, IDCT modules in Design1 through HDL (Verilog).Design 1 can generate 64 Transformed Coefficients per cycle. This implementation utilizes hardware resources (multipliers, adders) at higher expense.Inorder to overcome this problem a methodologyhasbeenimplementedinDesign2throughevenodd decomposition algorithm. Design 2 can generate 64 transform coefficients per clock cycle with less utilization of multipliers compared to Design 1.Multipliers occupy more area in hardware implementations. This paper mainly focusses to reduce hardware resources as much as possible. To eliminate utilization of multipliers completely a methodology has been proposed in this paper .The proposed methodology has been implemented in Design 3 generates 8 transform coefficients per cycle with complete elimination of multipliers (With Zero (0)multipliers).Design 3 also reduces Four(4) stages of DCT, IDC Toperationsto Two(2) stageswhichreducesthenumber of transform coefficients to be utilized. This modification reduces the adders and shifters count to minimal number. However this implementation produces 64 transform coefficients after 8 clock cycles. Allthe Designsaresimulatedandsynthesized using Xilinx Vivado(2018.1).Theresultsobtainedarecomparedin terms of both simulation and synthesis shows that the Proposed Methodology(Design 3)produces same simulation results as Design1andDesign2withlessutilizationofhardwareresources. This Proposed Hardware Design can be utilized in low power, area efficient FVC modules as it has less number of adders, shifters with complete elimination of multipliers.*

Index Terms*: *Future Video Coding (F.V.C), High Efficiency Video Coding(H.E.V.C), Discrete Cosine Transform (D.C.T), Inverse Discrete Cosine Transform(I.D.C.T),Even Odd DCT,IDCT Algorithms.

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I. INTRODUCTION

Image compression is a technique utilized in image processing applications to reduce size of image .This technique helps to store more amount of data in the available disc space and also reduces time required for images to be sent over the internet or downloaded from web pages.There are several different ways in which an image can be compressed. Image compression is mainly categorized into two types

1. Lossless, 2.Lossy

Lossy image compression is preferred by JPEG for image compression. Lossy compression reduces the quality of reconstructed image up to an extent. This loss is hard to identify as in real time processing. After reconstruction smoothening algorithms and filtering mechanisms are implemented on the image [1].

H.264, H.E.V.C, are the image compression standards utilized for lossy compression processing. F.V.C is the new image compression standard developed by I.T.U and I.S.O standardization organizations. H.E.V.C produces twice the image compression factor compared to H.264[2],[3].H.E.VC utilizestransformunitsofsize4x4,8x8,16x16,32x32.Inorder to improve compression efficiency and to increase processing speed F.V.C utilizes Transform units from 4x4 to 64x64[4]. DC Tisa lossy image compression algorithm utilized in FVC, HEVC Encoders. IDCT is used for image reconstruction After application of DCT the obtained values are quantized and at receivers end they are de-quantized before applying IDCT. Quantization is the area where actual compression occurs. Inthispapera8x8DCT,IDCTareimplementedona8x8 chunk of data. This implementation utilizes multipliers, adders in large number. In hardware implementation it is a specification to reduce multipliers count as much as possible as they occupy more area, consume more power.Inorder to implement an area efficient Architecture a methodology has been implemented in Design 2.This methodology has been implemented using evenodd decomposition algorithm. This implementation has less number of multipliers compared to Design 1 as it deals with 4x4 matrix multiplications on 8 input values at a time. This implementation can also generate 64 transform coefficients per clock cycle.

However to eliminate utilization of multipliers completely and to reduce adders count a methodology has been proposed in Design3. The Proposed method ologyisimplementedusing Even Odd Decomposition Algorithm [5][6][7] along with utilization of registers, multiplexers, adders/subtractors and shifters. The proposed methodologycangenerate8transformcoefficientspercycle.

II. METHODOLOGY

Design 1:

2- Dimension DCT Equation :-

For a N X N Image u(m,n), Forward DCT is defined as

$$\vartheta(k,l) = \alpha(k)\alpha(l)\sum_{m=0}^{N-1}\sum_{n=0}^{N-1} u(n)\cos\frac{\pi(2n+1)k}{2N}\cos\frac{\pi(2n+1)l}{2N}$$

$0 \le k \le N-1$

$1 \le k \le N-1$

Where $\alpha(0) = \frac{1}{\sqrt{N}}$ & $\alpha(k) = \frac{2}{\sqrt{N}}$

Inverse DCT (IDCT) is given by

$$u(m,n) = u(k) = \sum_{k=0}^{N-1}\sum_{l=0}^{N-1} \alpha(k)\alpha(l)\vartheta(k,l)\cos\frac{\pi(2n+1)k}{2N}\cos\frac{\pi(2n+1)}{2N}$$

$0 \le m,n \le N-1$

Coefficient matrix

N*N cosine transform matrix is given by C = {c(k,n)}

$$C(k,n) = \begin{cases} \frac{1}{\sqrt{N}}, & k = 0, 0 \le n \le N- \\ \sqrt{\frac{2}{N}}\cos\frac{\pi(2n+1)k}{2N}, & 1 \le k \le N-1 \\ & 0 \le n \le N-1 \end{cases}$$

DCT module in this design has been implemented through row column decomposition method.

8X8DCTcoefficientsgeneratedfromalgorithmareshownin form of variables for simplicity in equation 1.DCT,IDCT operations are performed using this coefficient matrix.

$$C = \begin{bmatrix} a & a & a & a & a & a & a & a \\ b & c & f & g & -g & -f & -c & -b \\ d & e & -e & -d & -d & -e & e & d \\ c & -g & -b & -f & f & b & g & -c \\ a & -a & -a & a & a & -a & -a & a \\ f & -b & g & c & -c & -g & b & -f \\ e & -d & d & -c & -e & d & -d & e \\ g & -f & c & -b & b & -c & f & -g \end{bmatrix}$$

Implemented architecture of the DCT, IDCT modules are shown in Figures 1,2

TheImplementedmethodologyinDesign1involves4stages of multiplication operations. Each stage involves 8x8 Matrix multiplication operation which generates 64 transformed coefficients percycle. IDCT implementation is also similar to DCT but the application of transform coefficients is in reverse manner. The design implemented is simulated and synthesized in Xilinx Vivado 2018.1.

DCT Module

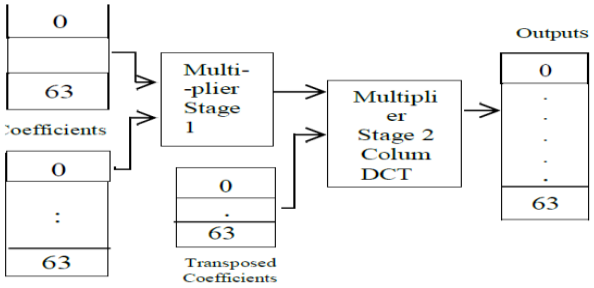

Figure 1:- Block diagram of DCT

IDCT Module

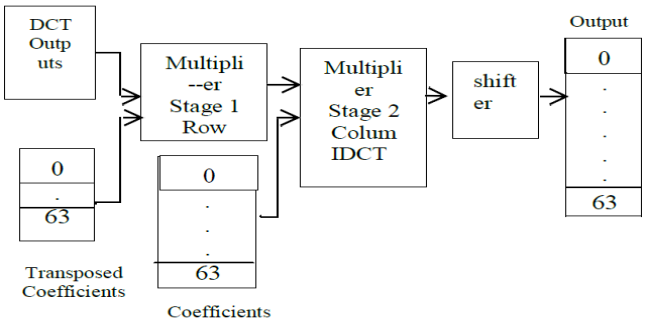

Figure 2:- Block diagram of IDCT

Design 2:

Even Odd Decomposition Algorithm:

Design 1 implementation involves 4 stages of 8x8 multiplication operations. It is a specification in hardware implementation to minimize multipliers count as much as possible as they occupy more area. To reduce multipliers count 8x8 DCT,IDCT are implemented using Even Odd Decompositionalgorithm. Even Odd Decompositionhelpsto Decompose an 8x8 module (DCT/IDCT) to two (2) 4x4 modules. This Decomposition technique implemented in Design 2 helps to reduce Hardware(multipliers especially) and produces samesimulation results as of Design 1.The Even Odd Decomposition algorithm operates column wise on input matrix using symmetrical properties of DCT,IDCT.

Even Odd Decomposition algorithm can be implemented in formofmatrixoperationsshowninequation2,3(DCT,IDCT)

Hardware representation of implemented Design is shown in Figures 3,4 for DCT and IDCT modules The design implemented is simulated and synthesized in Xilinx Vivado 2018.1.

Even Odd DCT Algorithm in form of matrix operations

$$\begin{bmatrix} Y(0) \\ Y(2) \\ Y(4) \\ Y(6) \end{bmatrix} = \begin{bmatrix} a & a & a & a \\ c & f & -f & -c \\ a & -a & -a & a \\ f & -c & c & -f \end{bmatrix} \begin{bmatrix} X(0)+X(7) \\ X(1)+X(6) \\ X(2)+X(5) \\ X(3)+X(4) \end{bmatrix}$$

$$\begin{bmatrix} Y(1) \\ Y(3) \\ Y(5) \\ Y(7) \end{bmatrix} = \begin{bmatrix} b & d & e & g \\ d & g & -b & -e \\ e & -b & g & d \\ g & -e & d & -b \end{bmatrix} \begin{bmatrix} X(0)-X(7) \\ X(1)-X(6) \\ X(2)-X(5) \\ X(3)-X(4) \end{bmatrix}$$

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Even Odd IDCT Algorithm in form of matrixoperations

$$\begin{bmatrix} Y(0) \\ Y(1) \\ Y(2) \\ Y(3) \end{bmatrix} = \begin{bmatrix} a & c & a & f \\ a & f & -a & -c \\ a & -f & -a & c \\ a & -c & a & -f \end{bmatrix} \begin{bmatrix} X(0) \\ X(2) \\ X(4) \\ X(6) \end{bmatrix} + \begin{bmatrix} b & d & e & g \\ d & g & -b & -e \\ e & -b & g & d \\ g & -e & d & -b \end{bmatrix} \begin{bmatrix} X(1) \\ X(3) \\ X(5) \\ X(7) \end{bmatrix}$$

$$\begin{bmatrix} Y(7) \\ Y(6) \\ Y(5) \\ Y(4) \end{bmatrix} = \begin{bmatrix} a & c & a & f \\ a & f & -a & -c \\ a & -f & -a & c \\ a & -c & a & -f \end{bmatrix} \begin{bmatrix} X(0) \\ X(2) \\ X(4) \\ X(6) \end{bmatrix} - \begin{bmatrix} b & d & e & g \\ d & g & -b & -e \\ e & -b & g & d \\ g & -e & d & -b \end{bmatrix} \begin{bmatrix} X(1) \\ X(3) \\ X(5) \\ X(7) \end{bmatrix}$$

EVEN ODD DCT MODULE

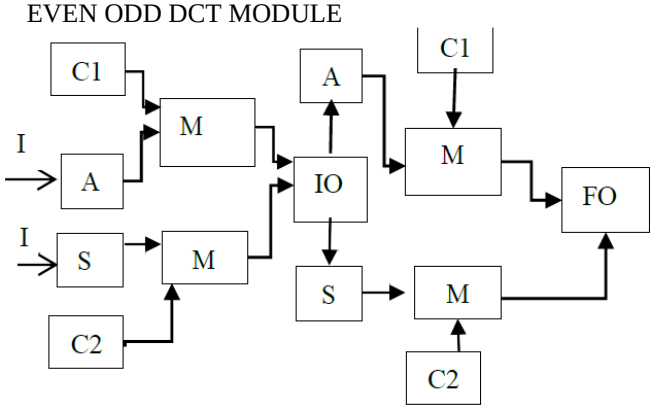

Fig: 3. Even odd DCTmodule
I→Inputs,M→Multiplier,C1,C2→Odd, EvenDCTCoefficients,A→Adder,S→Subtractor, IO→IntermediateOutputs,FO→FinalDCTOutputs

EVEN ODD IDCT MODULE

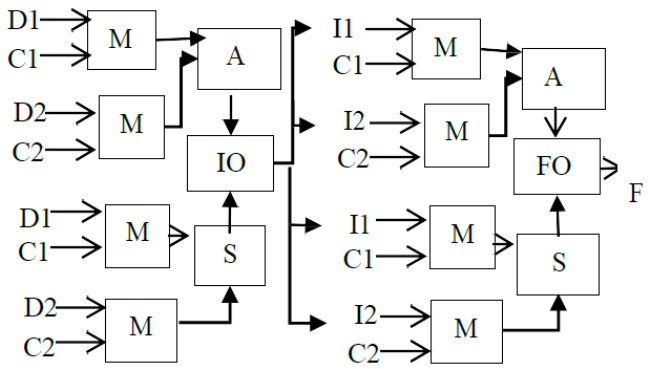

Fig 4: Even odd IDCT module
D1,D→DCTOutputs,IM→Multiplier,C1,C2→EvenOdd IDCTCoefficients,A→Adder,S→Subtractor, IO→IntermediateOutputs,I,I2→IntermediateOutputs,FinalI DCTOutputs→IDCToutputs

I. PROPOSEDMETHODOLOGY Design3

From the implementations of Design 1 and Design 2 it is evident that DCT,IDCT implementation involves utilization of resources in larger number especially multipliers,adders.DCT,IDCT implementations involves 4 stages of operations (Two(2) for DCT,Two(2) for IDCT).This results in increase of computational complexity alongwiththehardwareresources.Inordertoovercomethese issues a methodology has been proposed and implementedin Design 3.The proposed methodology eliminates the utilization of multipliers that is entire DCT ,IDCT modules areimplementedwithZero(0)Multipliersthroughaddingand shifting operations. This methodology also reduces four(4) stages of operation to two(2) stages(One(1) for DCT,One(1) for IDCT).This can be achieved through utilization of two multiplexers, multiple registers. Entire mechanism is applied to Even Odd Decomposition Algorithm only. In Design2 128 transform coefficients are utilized. The Proposed methodology (Design 3) utilizes only 64 transform coefficients to complete the entire operation (DCT, IDCT).Proposed Methodology requires half the number of transform coefficients utilized in Design 2. As number of coefficients to be utilized reduces shifters and adders count also reduces as each coefficient utilized requires at least an adder, shifter for implementation. In Design 3 usingcounters same hardware is utilized for all 8x8 chunk of inputs for performingDCT,IDCToperations.TheimplementedDesign is simulated and synthesized same as Design 1, Design 2.Design3withZeroMultipliersandLessnumberofAdders, shifters can be utilized in low power, Area Efficient FVC, HEVCModules.

ProposedArchitectureforEvenOddDCT,IDCTmodulesar e shown in figures5,6.

Proposed Architecture of Even Odd DCT Module

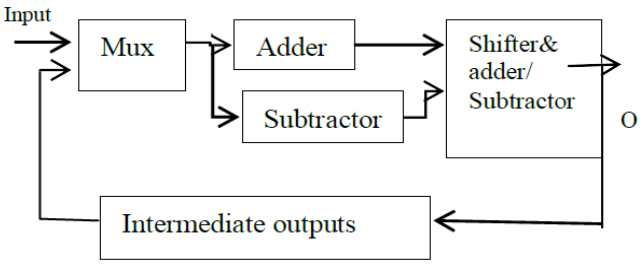

Fig: 5.Proposed Even Odd DCTModule

Proposed Architecture of Even Odd IDCTModule

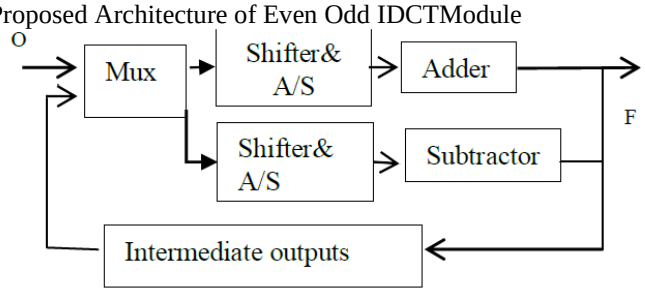

Fig:6.ProposedEvenOddIDCTModule
O□DCToutputs,Mux□Multiplexer(2:1),A/S□Adder/Subtra ctor,F□FinalIDCTOutputs

III. RESULTS ANDDISCUSSION

All the 3 Designs are simulated and synthesized in Xilinx Vivado 2018.1 using Verilog HDLZed Board is utilized for simulation and synthesis of all the 3 Designs.8x8 Chunk of data(64 values) is Fed as input to all the 3 Designs(same inputs for all the 3 Designs) and the output results are observed.In Design1 at a time 8x8 Chunk(64 outputs) are obtained.InDesign2atatimethe64outputsareretrieved.In Design 3 which is the proposed method 64 outputs are obtained after 8 Clocks.

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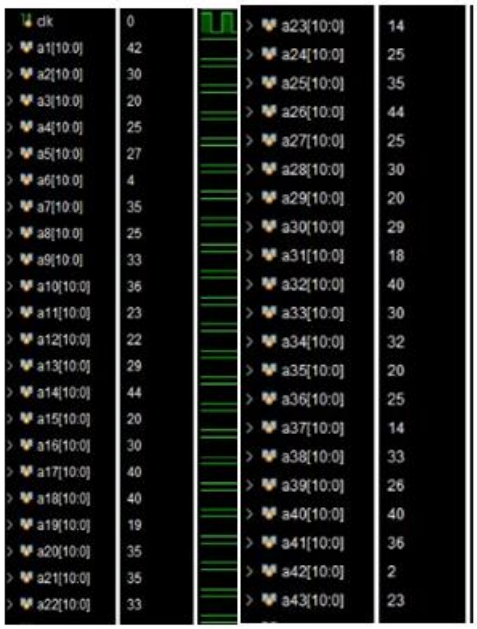
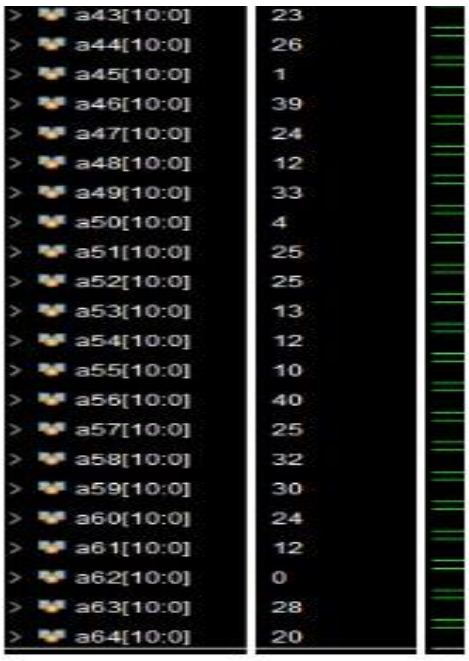
The results obtained in simulation of allthe3Designsaresameandallarealmostequaltotheinput values with little variation as it is DCT,IDCT Compression(lossyCompression,there is liitle decrement in output value with respect to inputvalues).

Simulation Results are snipped from Vivado tool and shown in Figure A,B Inputs: For Simple Representation purpose inputs and Outputs obtained in Design3(Proposed Methodology)are shown FigureA InputsatDCT





FigureA InputsatDCTFig:A.Inputs

FigureB→OutputsatIDCT

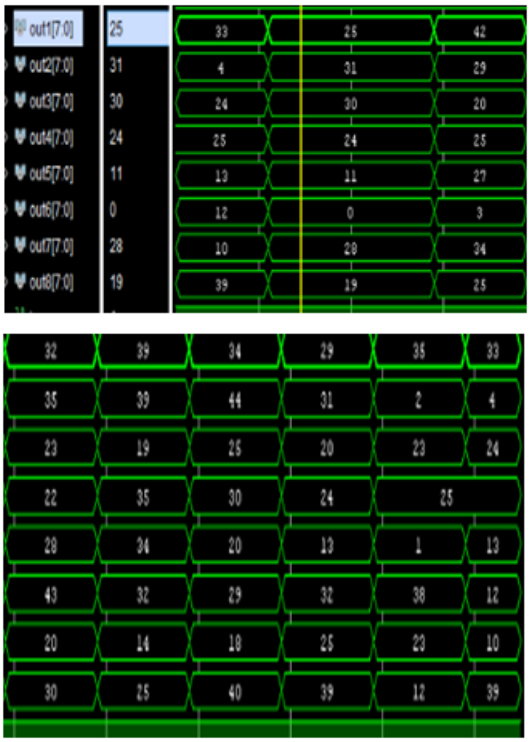


Fig: B Outputs

A sample of obtained outputs for applied inputs are compared in Table I Below

Table I

INPUTS	OUTPUTS
25	25
32	31
30	30
24	24
12	11
0	0
28	28
20	19

Little variation in outputs is due to application of LossyDCTalgorithmWhichresultsinreductionofoutputvalu esto an extent compared toinputs

Synthesis Report (Resources):

The implemented Designs are synthesized and obtained parameters are tabulated.Parameters obtained for Design 1,Design 2 are shown in Table II,Table III

Design 1

Table II

Parameter	DCT	IDCT
Multipliers	588	656
Transform Coefficients	128(64x2)	128(64x2)
Registers	64	64
Adders	64	128

DESIGN2

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TableIII

Parameter	DCT	IDCT
Multipliers	448	384
Transform Coefficients	64(32x2)	64(32x2)
Registers	429	797
Adders	288	304

Synthesis report generated for Design 3 in Xilinx Vivado is snipped and shown in Figure C, Figure D.

```
Hierarchical RTL Component report
Module eo
Detailed RTL Component Info :
+---Adders :
       4 Input     41 Bit       Adders := 1
      13 Input     41 Bit       Adders := 3
       5 Input     41 Bit       Adders := 1
      14 Input     41 Bit       Adders := 3
       2 Input     41 Bit       Adders := 4
       3 Input     41 Bit       Adders := 4
       2 Input     12 Bit       Adders := 4
       3 Input     12 Bit       Adders := 4
       2 Input      6 Bit       Adders := 1
       2 Input      5 Bit       Adders := 1
+---Registers :
                   41 Bit    Registers := 136
                   11 Bit    Registers := 8
                    6 Bit    Registers := 1
                    5 Bit    Registers := 1
                    1 Bit    Registers := 3
```

FIG:C.PROPOSEDDCT SYNTHESIS REPORT

```
synth_1_synth_synthesis_report_0 - synth_1
C:/Users/viswanadh yellumraju/evenoddfinal.runs/synth_1/idct.vds
 98  Start RTL Hierarchical Component Statistics
 99  ---------------------------------------------------------
100  Hierarchical RTL Component report
101  Module idct
102  Detailed RTL Component Info :
103  +---Adders :
104        2 Input     42 Bit       Adders := 4
105        3 Input     42 Bit       Adders := 4
106       13 Input     41 Bit       Adders := 1
107        4 Input     41 Bit       Adders := 3
108        2 Input     41 Bit       Adders := 2
109       14 Input     41 Bit       Adders := 3
110        5 Input     41 Bit       Adders := 3
111        2 Input      6 Bit       Adders := 2
112  +---Registers :
113                    42 Bit    Registers := 8
114                    41 Bit    Registers := 136
115                     8 Bit    Registers := 8
116                     6 Bit    Registers := 2
117                     1 Bit    Registers := 3
```

FIG:D.PROPOSEDIDCT SYNTHESIS REPORT

From the Synthesis Report Shown in Figures C, D the parameters obtained are shown in Table IV

DESIGN 3

TableIV

Parameter	DCT	IDCT
Multipliers	0	0
Adders	26	22
Shifters	72	80
Transform Coefficients	32	32
Registers	149	157
LUT	3579	3847

AcomparisonhasbeenmadeforalltheimplementedDesigns and the parameters obtained are shown in TableV

Table V

	Multipliers	Adders	Transform coefficients	Registers
Design 1 (DCT + IDCT)	1244	192	256	128
Design 2 (DCT + IDCT)	832	592	128	1266
Proposed Method(DCT + IDCT)	0	48	64	306

Design 1 utilizes 1244 multipliers,192 adders ,256 coefficients. Design 2 reduces multipliers count to 832 , and coefficients count to 128 but utilizes more number of adders, registers compared to Design 1.Proposed Methodology which has been implemented in Design 3 utilizes 64 transform coefficients,48 adders and optimal number of registers with zero multiplies to perform entire operation

IV. CONCLUSION:

In this paper 3 Designs are simulated and synthesized in Xilinx Vivado using Verilog HDL.Design 1 is implemented using2DDCT,IDCTRowColumnMethod.Design1utilizes multipliers, adders at higher expense. Design 2 reduces multiplier count to certain extent using even odd decomposition Method. Proposed Methodology which has been implemented in Design 3 implements the entire DCT, IDCT operation with Zero (0) Multipliers. It utilizes 25 percentage of transform coefficients, adders utilized in Design1, and 50 percent of transform coefficients utilized in Design 2. However proposed methodology takes 8 clock cycles to process a chunk (8x8) ofdata.

DCT, IDCT modules are used in FVC, HEVC Encoders and Decoders for better compression factor. The work performed in this paper can be extended by applying DCT, IDCT algorithms to a real time image and also to observe Compression factor quantization mechanism can be implemented

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AUTHORS PROFILE

Mr. P Srikanth Reddy has more than 5 years of industrial experience working on FPGA & Hardware Implementation of video processing codecs in TYNETEE and PATHPARTNER TECHNOLOGIES. He obtained his masters degree in microelectronics and system automationat NORTHUUMBRIA university, newcastle upon tyneU.K .He is currently working as assistant proffessor in klef deemedtobeuniversity.Hisresearchactivitiesarerelatedto vlsi design, Verification , implementation and signal processing applications, machine learningalgorithms.

Mr Y Viswanadhis currently pursuing his masters degree in vlsi design at klef deemed to be university He obtained his bachelors degree in electronics and communication engineering at v.k.r,v.n.b&a.g.k college of engineering. His research activities includes hardware design & implementation of dct,idct modules forfvc&hevccodecs,digitalvlsi modules design and verification through hdls His other works includes hardware implementation of various protocols likespi,uart.

Mr.M Sridhar is currently pursuing his masters degree invlsidesignatklefdeemedtobeuniversity.Heobtained his bachelors degree in electronics & communication engineering at vishnu institute of technology. His working area of interest includes digital vlsi design& hardware implementation, software to hdl code conversions, hls methodologies.