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Efficient Cell Sizing Of Single Precision Floating Point ALU for DSP Applications

D.V.Sivasai , N.Srinivasulu, D.Kondamacharyulu

Abstract: ***Technological advancement in satellite communication and signal processing technology, high frequency of operation with low noise margin is required. So the technological advancement has resulted in the introduction of digital technology where digital processing units had created more impact. The ALU plays a crucial role in digital technology by encrypting the data and providing more secrecy and security. Numerous ALU blocks are required in DSP units for the proper transfer of the signals. As a result various methodologies are introduced for the design of ALU unit. The most recent history of digital technology suggests that there is a rapid growth in various technological aspects leading to compression of technologies from micro level to Nano level at a very faster rate. So various lateral thinking methodologies had come into existence for the designing process. This led to a thought of designing a most significantly used digital block of the circuitry with the help of advantageous and advanced methods. In this paper where the basic problem in the blocks like sizing can be reduced and power consumption can be explained. A righteous and well executed tools are used in the design methodology to properly regulate and monitor the basic parameters. Most preferable XILINX VIVADO is used in the process of design.***

Keywords: Digital signal processing ,Single Precision ,IEEE 754 PROTOCOL , SOC

I. INTRODUCTION

The ALU are the major working blocks in the digital technology and can be used in various real time applications like communication and data secrecy. Floating point ALUs are badly advantageous in filter designing and other various digital processing applications. The standardized IEEE 754 protocol techniques are used in the analysis of single precession and double precession operation containing a sign bit, an exponent and a binary mantissa.[1] The floating point ALU have a high scope in various signal processing and data path systems with a low noise margin operating at a high frequency Helpful in communication systems. The latest research technology in 3 dimensional computational analysis and highly used graphical processing units which are used in various architectural models, motion picture and animations.[5] Floating-point multiplication is one of the most frequent operations in FP applications. In addition to the three basic steps in fixed-point multiplication, which are partial product generation, partial product accumulation, and final stage addition, the FP multiplication also needs to perform product normalization and rounding, as well as the sign and exponent processing[4]. He proposed a booth encoding algorithm to deuce the area. The main draw back of the conventional way of designing a ALU resulting high usage
of performance parameters. It is more sensitive to high level bit manipulation. A special technique named latency fusion between binary bits the exponential bits to ease the arithmetic way of implementing digital logic that helped to analyze the computation in an easier way implement but the accuracy of the acquired signal is not adequate with respect to mathematical calculation[3]. The floating point architecture was with single precession was proposed which is an easy way of implementing the multiplication operation with less area resulting in reduction area consumption in the ALU design. The floating point architecture shows a greater variation in the results with accuracy. It helps us in operating in the less latency and faster speed and the capacity to reconfigure the chip area in the hard core implementation. The DSP operations work under a very high frequency and travel through long distance which can be done by the proper design of the DSP processor where the floating point ALU plays a crucial role. The floating point ALU's are the important components in the central processing units (CPU) and various processors like MIPS processors.

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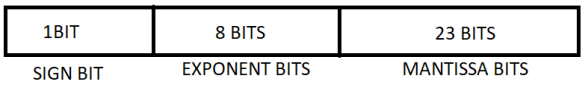
II. IEEE 754 PROTOCOL

The floating point operations work in the standardized protocol where each decimal is subjected into 3 parts.

- 1 sign bit
- 8 exponent bits
- 23 mantissa bits

The single precision contains 32 bits



The standardized representation of the any floating point number is given by

FP=(-1)^N * 1.M * 2^(E-bias)

where N= sign bit
M=mantissa bits
E=exponent bits
Bias=normalized correction

In the single precision operation the normalised correction is 127. Therefore the representation is referred as[3]

FP= (-1)^N * 1.M * 2^(E-127)

Apart from the representation of the decimal value this protocol contains some special numbers which obstruct the operations such as

- **Signed zero:** It tends to extreme negative value or the extreme positive value when divided by any number but the mathematical value of the number remains the same. The sign represents the tending of the value on the number scale.
- **Sub normal numbers:** Significantly known as the underflow gap between the adjacent values of the numbers.
- **NAN's:** Special case numbers where the result is invalid operations like the complex numbers (square root of the negative numbers). The result of any NAN multiplied by 0 is 1.

2.1 ROUNDING NUMBERS:

Used to reduce the complexity of the operation.This is mainly done in normalization process. These rounding models are of various types

- Nearest integer rounding
- Up rounding (to infinity)
- Down rounding (to negative infinity)
- Towards zero (tend to slide towards zero)

2.2 EXCEPTIONAL CASES:

In the floating point operations there exist some exceptional cases or the invalid kind of operations that tend to cause fault result. Various kinds of exceptional cases are

- Divide by zero
- Complex numbers
- Non-terminating decimals

To remove these kind of exceptional cases exceptional handling is used in different ways to set the results which do not effect the floating point operations.

- **Inexact:** if there is a difference between the exact result and the rounding result.
- **Underflow:** if rounded value limit tends to zero.
- **Overflow:** if rounded value limit tends to infinity or large number
- **Divide by zero:** set for finite operands and infinite results.
- **Invalid:** set for not a real valued function

III. DESIGN ARCHITECTURE

The floating point ALU architecture should perform the arithmetic operations and some of the universal logic operations that are shown in figure 1. The analysis of the design in the ALU architecture should contain all the sub element blocks with each block having to restore the properties of the IEEE 754 protocol . The ALU architecture contains an adder/subtractor architecture together, a multiplier architecture and a divider architecture and a shift register to perform the left or right shift operations during the normalization of the result.

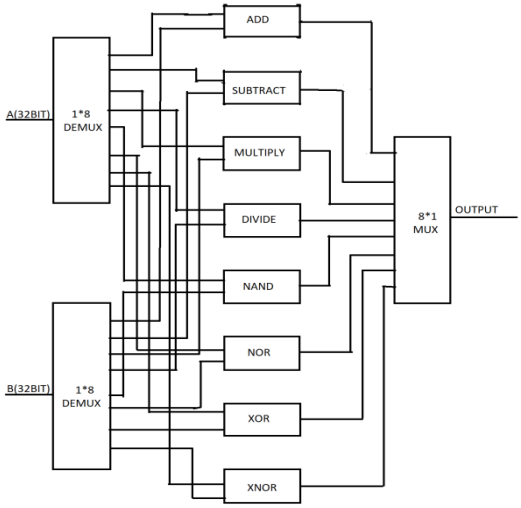


Figure 1: Architecture Of The Alu

The ALU architecture contains an adder/subtractor architecture together, a multiplier architecture and a divider architecture and a shift register to perform the left or right shift operations during the normalization of the result.

TABLE 1: ALU OPERATION THROUGH SELECTION

S.NO	SELECTION BITS [2:0]	ALU OPERATION
1.	000	ADDITION
2.	001	SUBTRACTION
3.	010	MULTIPLICATION
4.	011	DIVISION
5.	100	NAND
6.	101	NOR
7.	110	EX-OR
8.	111	EX-NOR

Each sub element block has a separate kind of algorithm which allows to design those modules in the effective manner.

3.1 SHIFT REGISTER:

The basic element in the shift register is the flip flop who share the data from one another through the same clock pulse at a time . In the architecture the universal shift register is required to perform the left or the right shifting operations. Figure 3 shows the resemblance of a shift register.

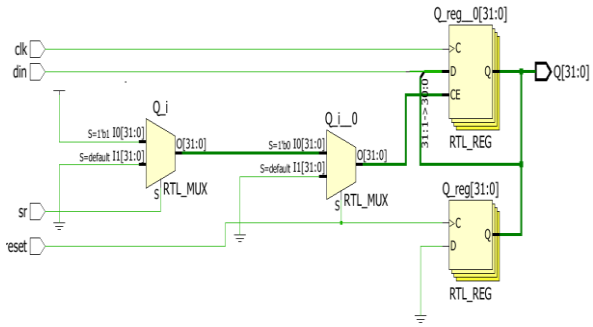


Figure 2: Shift Register

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Shift register plays a key role in the normalization process. The main use the element is to implement feedback operations or to perform the stack operations on the hardware or as a memory element.

3.2 ADDER/SUBTRACTOR ALGORITHM:

Consider the algorithm of an adder/subtractor shown in figure 4. These addition or subtraction operations are the basic arithmetic operations in the ALU. The floating point addition and subtraction operation take the help of a shift register .

3.2.1 INITIALIZING MODULE: It initializes the floating point numbers and convert them into a standard IEEE 754 protocol by subjecting it into the sign, exponent and mantissa bits.

3.2.2 EXPONENT CHECKER: At this point the value of the numbers of the exponent are checked by the equivalent operations. If the values of the exponents are same then the exponent and mantissa values are passed directly. If they are not equal then the mantissa is shifted to the left by the difference if the exponents.

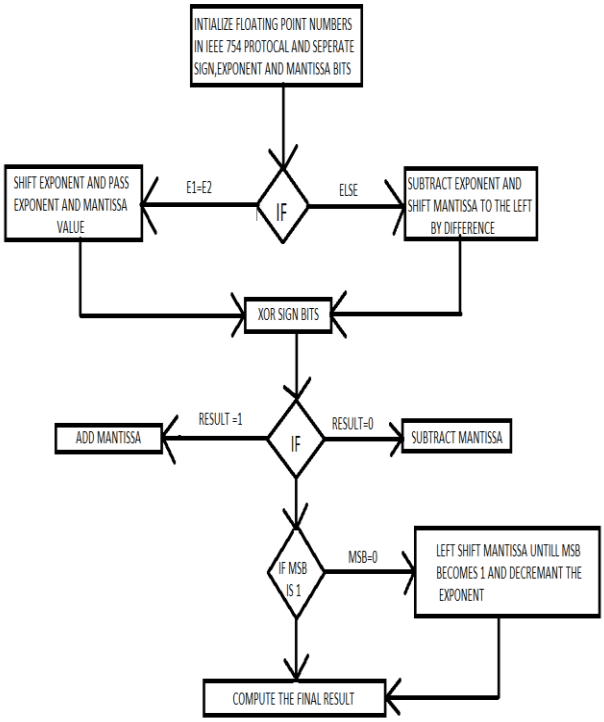

FIGURE 3: ADD/SUB ALGORITHM

3.2.3 SIGN CHECKER: The sign bits of the two operands are checked using the ex-or operation and if the result of the sign is 1 then addition operation is performed if 0 then the subtraction operation is performed.

3.2.4 MSB CHECKER: After the addition or the subtraction operation is performed if the MSB of the resultant mantissa is 1 the result is computed directly else the mantissa is shifted left until the MSB bit becomes 1 and the exponent is reduced by 1.

3.3 MULTIPLIER ALGORITHM:

The adder plays a crucial role in the floating point multiplication along with the shift register. It has the same operation to that of an adder in the MSB checker and the initialize module.

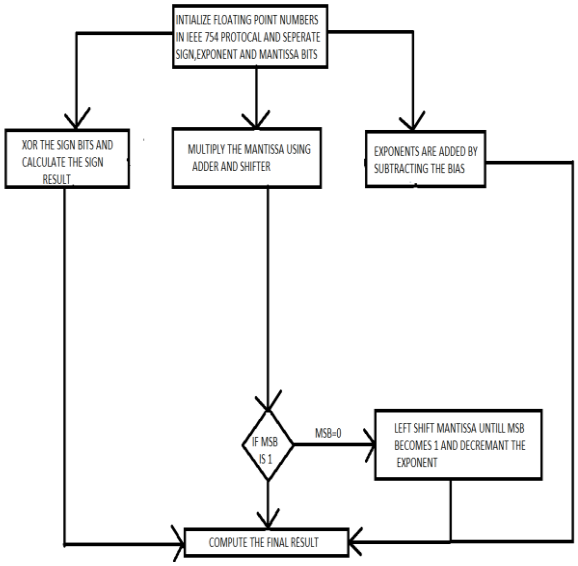

FIGURE 4: MULTIPLIER ALGORITHM

3.4 DIVIDER ALGORITHM:

The divider can be the multiplication operations to multiplicand and the reciprocal of the multiplier. It has the similar kind of operation to that of multiplication in the sign result and the MSB checker. It can also be considered as the cumulative operation of the subtrator and the right shifter algorithm. It plays a crucial role in division multiplexing of the communication signal like the time division and the frequency division multiplexing operations.

3.4.1 PADDING MODULE: Adding 0's to the LSB bit of the mantissa until the number of bits become doubled.

3.4.2 EXPONENT CHECKER: The exponent of the operands are subtracted by adding the bias.

3.4.3 DIVISION CHECKER: If the mantissa of the first operand is less than the second operand then perform the division operation else shift the mantissa towards right by 1 bit and decrement the exponent and perform division operation and later compute the result to the MSB checker

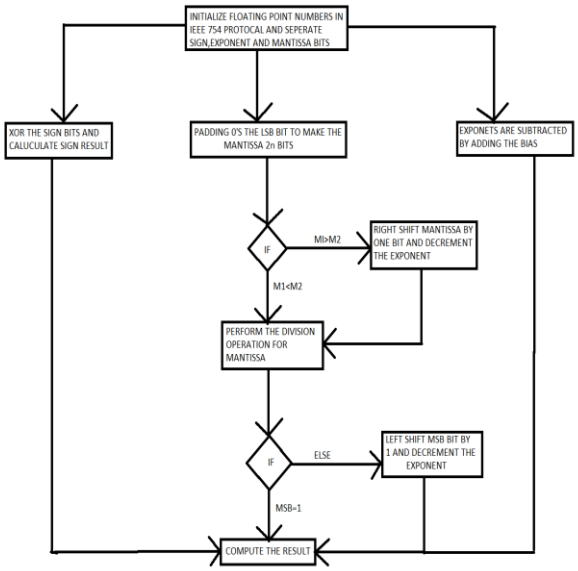

FIGURE 5: DIVISION ALGORITHM

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IV. RESULTS AND DISCUSSIONS

Each module in the floating point ALU architecture is designed with an aim of reducing the consumption of the hardware area from the utilization process. The proposed architectures have a reduction in the number of LUT's used and the number of DSP blocks used the number of flip-flop's used. Considering the reduction in number of utilizations the floating point ALU is more area efficient. The elaborated designs of the ALU components and its performance characteristics with respect to area are shown[8].Simulation of floating point adder is required in the operation of the ALU design. The area constraint are shown in the figure 8 corresponding to the major aim of the proposed design.

FIGURE 6: ADDER SIMULATION RESULT

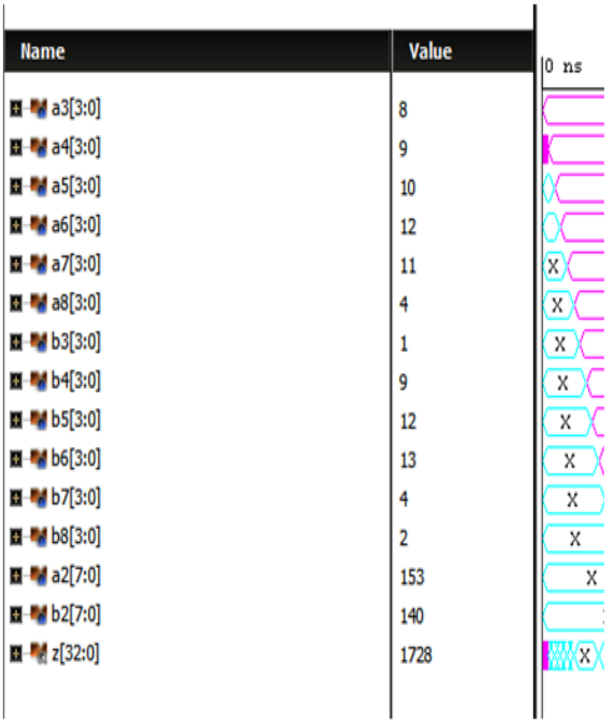

FIGURE 7 SIMULATION RESULT OF SUBTRACTOR

In recent years, Floating-point numbers are widely adopted in many applications due to its high dynamic range and good robustness against quantization errors, capabilities. Floating-point representation is able to retain its resolution and accuracy. IEEE specified standard for floating-point representation is known as IEEE 754 standard. This standard specifies interchange and arithmetic formats and methods for binary and decimal floating-point arithmetic in computer programming environments.[IEEE 754-2008].

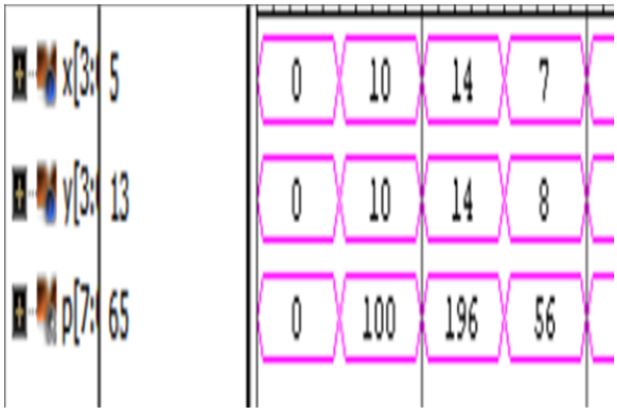

FIGURE 8: SIMULATION OF MULTUPLIER

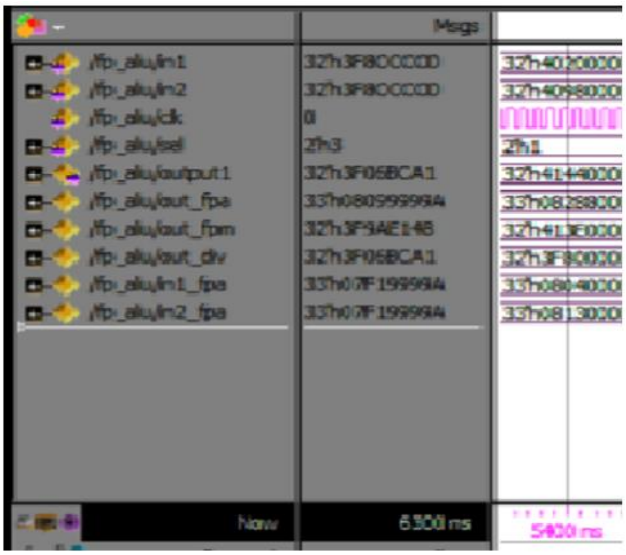

FIGURE 9: SIMULATION RESULT OF DIVIDER

An observation of reduction in major area constraints of the like the LUT's, IO blocks and the flip flop are reduced compared to the existing design in the adder architecture. Reduction in the area constraint of the architectural block helps in a theoretical assumption of reduction in the consumed power of the architecture with respect to the area. The fact that floating-point numbers cannot exactly represent all real numbers , which floating point operations cannot exactly represent true arithmetic operations results in several shocking things. This is often associated with the finite preciseness with that computers usually represent numbers.composition Ni_xMn_{1-x}. Be aware of the

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different

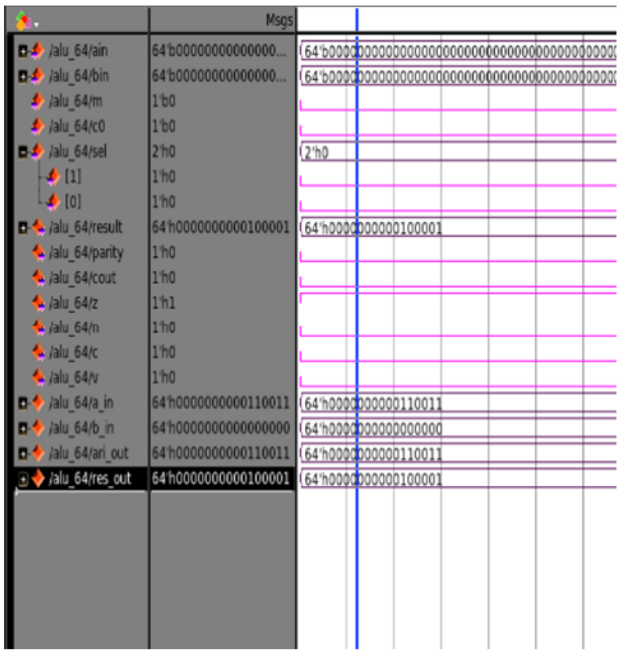

FIGURE 10 SIMULATION RESULT OF ALU

meanings of the homophones

An ALU encompasses a kind of input and output nets, that area bunit the electrical conductors accustomed convey digital signals between the ALU and external electronic equipment. once associate degree ALU is working, external circuits apply signals to the ALU inputs and, in response, the ALU produces and conveys signals to external electronic equipment via its outputs .

Assumption of the power analysis can be done by analyzing the reduction in the parameters of the area constraints.[2] Figure 11 depicts the area comparison of adder. The simulation result of the floating point multiplier design is done by the Kasturba algorithm shown in figure 8. Where the simulated result is shown in the radix unsigned decimal form. Elaborated design of the multiplier is simulate in the VIVADO 2018.2.[1]

Obtained area report of the proposed multiplier is verified with the results of VERTEX-5 and VERTEX-7 and concluded as shown in figure 13. Arithmetic complex design performed by various design methodologies resulted in efficient design. Figure 9 plots the simulation result of the divider architecture to be noticed in the and its area constraints are analysed in figure 14.

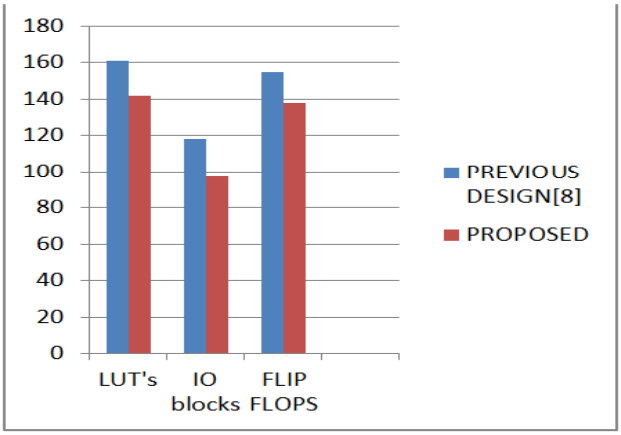

FIGURE 11: AREA COMPARISION OF ADDER

. Analysis of these results are done in various micro boards in the XILINX VIVADO like the zed board, zync 7000 and the zed board evolution kit.[6] All modules within the ALU style area.

Unit complete mistreatment Verilog HDL take a look at vectors area unit given to the inputs of the Figures and Tables.

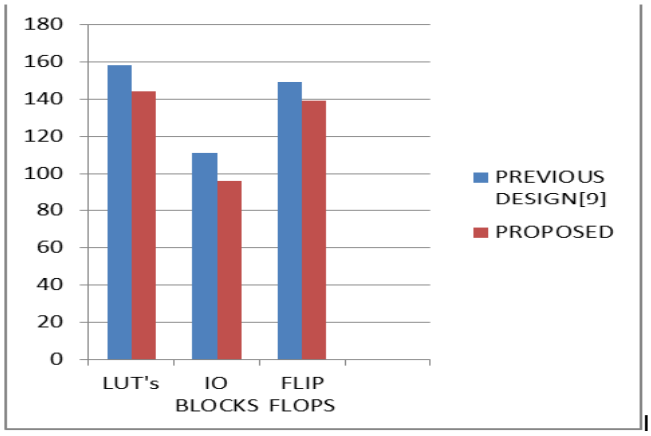

FIGURE 12 : AREA COMPARISION OF SUBTRACTOR

The opcode input may be a parallel bus that ALU associate operation choice code, that is associa te enumerated price that specifies specified arithmetic or logical operation to be performed by the ALU. The opcode size (its bus width) determines the utmost variety of various operations the ALU will perform; as an example, a four-bit opcode will specify up to sixteen completely different ALU operations. Generally, associate ALU opcode isn't a similar as a machine language opcode. floating purpose ALU to testify its practicality

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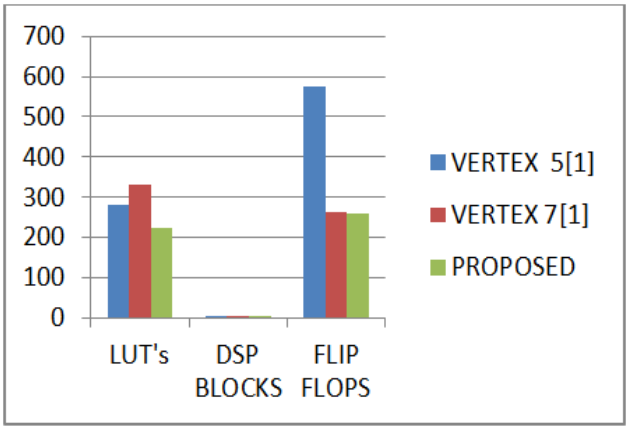

FIGURE 13: AREA COMPARISION OF MULTIPLIER

The simulation is meted out with 6.5b machine and RTL synthesis is finished with RTL Compiler tool in Cadence. Physical style of this design is finished with SoC Encounter cadence tool in 180nm technology. Analysis of these results are done in various micro boards in the XILINX VIVADO like the zed board, zync 7000 and the zed board evolution kit.[6]

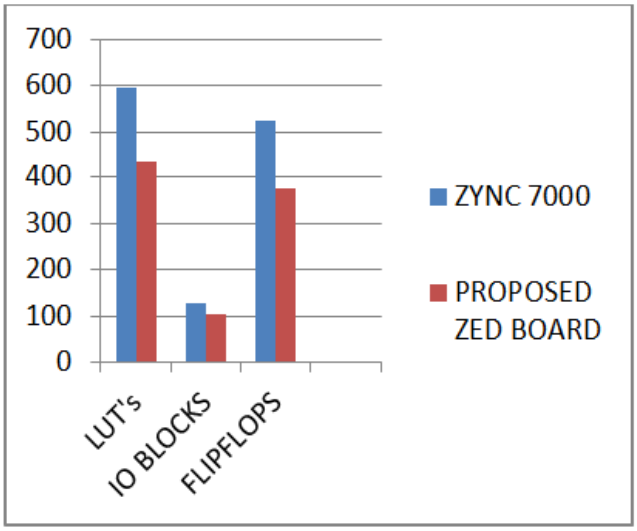

FIGURE 14: AREA COMPARISION OF DIVIDER

Cell usage reduction of the ALU blocks where the number of usage elements are reduced compared to the previous work where the area can be reduced [9]. Theinputs to AN ALU area unit the information to be operated on, known as operands, and a code indicating the operation to be performed; the ALU's output is that the results of the performed operation. In several styles the ALU additionally has standing inputs or outputs or both that convey info a couple of previous operation or the present operation severally between the ALU and external standing registers .Arithmetic operations are combined with some logical operations as shown in table 1 and the more efficient ALU helpful in DSP applications and filter designs. Figure 10 shown the simulation result of the ALU operations. it would seem that an outsized range of additional digits would want to be provided by the adder to confirm correct rounding; but, for addition or subtraction victimization careful implementation techniques solely 2 additional guard bits and one additional sticky bit have to be compelled to be carried on the far side the preciseness of the operands.

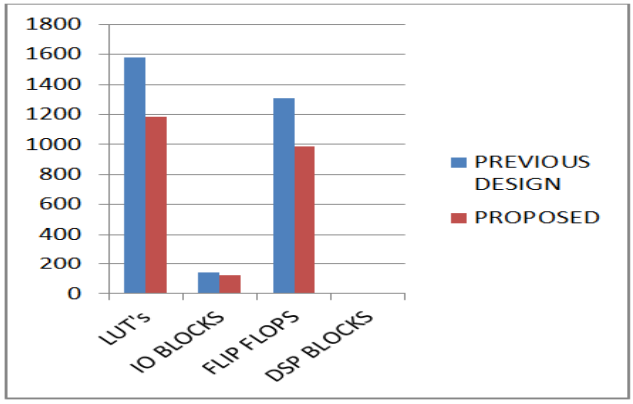

FIGURE 15: AREA COMPARISION OF ALU

In the digital design process the area and power of any design are interlinked towards each other. The power of any combinational or sequential circuit is dependent on its consumed area resources. So the number of LUT's or any other area constraint in the designed circuitry is reduced therefore an assumption that the power consumption of the design also reduced. Figure 16 shows the power and area relation of each block in the ALU design.

	LUT's	IO BLOCKS	FLIP FLOPS	DSP's
ADDER	142	97	138	-
SUBTRACT	149	96	136	-
MULTIPLIER	224	-	260	2
DIVIDER	433	104	375	-
ALU	1184	122	986	3

TABLE 2: AREA OF EACH BLOCK IN ALU

POWER ANALYSIS:

General design technology follows more than single parameter its design constraint. Due to the reduction in one of the design constraints i.e. cell usage a parallel parameter proportional to the obtained and analysed. By considering the decrease in the area parameter a theoretical assumption was concluded that the power consumption of the architectural analysis was studied through the graphical representation shown figure 16-20.

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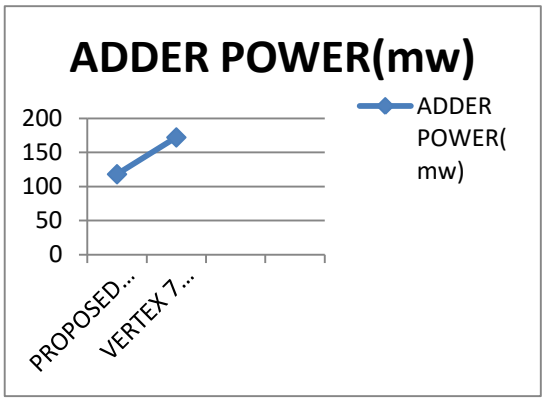

FIGURE 16: POWER COMPARISON FOR ADDER

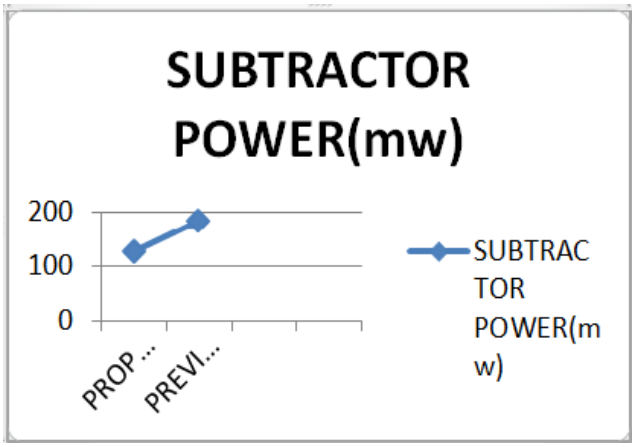

FIGURE 17: POWER COMPARISON OF SUB

From the power analysis graph we can come to a conclusion the power and area are interdependent on each other. The power of any architectural design block can be analysed using the implementation of the cell usage in the circuitrary.

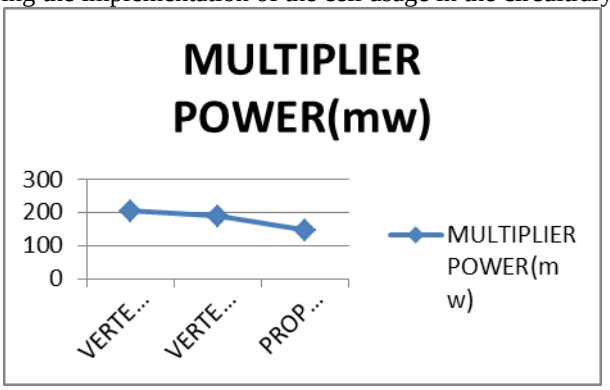

FIGURE 18:MULTIPLIER POWER CONSUMPTION

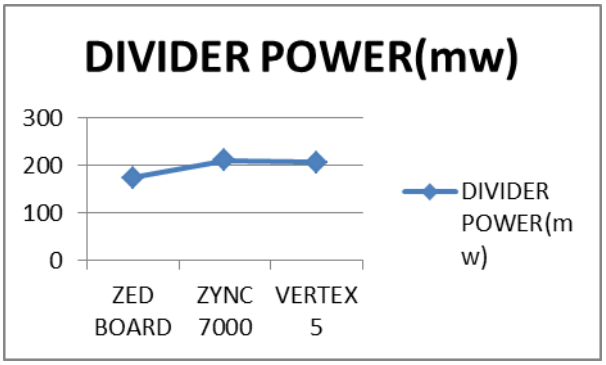

FIGURE 19 : DIVIDER POWER CONSUMPTION

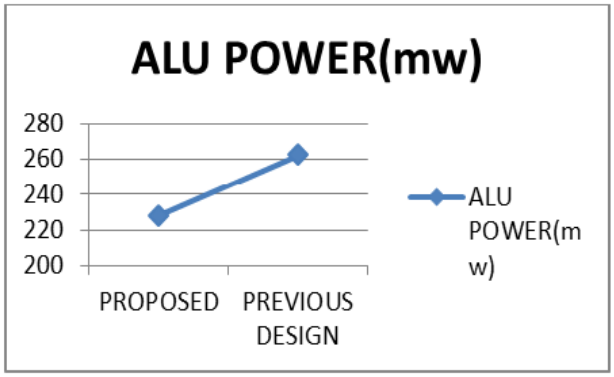

FIGURE 20: ALU POWER CONSUMPTION

CONCLUSION

From this paper it is evident that the ALU module in various computer architectural components like the CPU'S and the MIPS processors can be designed in a more efficient way by reducing the utilization and increasing the area effiency. This ALU block plays a crucial role in signal transmission and receiving in the DSP applications which will help in maintaining the secrecy of the data by encryption and decryption. Taking on further a more efficient DSP processor can be designed with a program controller which helps in the digitalization of the analog data and storing it at a high frequency.

REFERENCES

1. IET Digit.Tech. 2017, Vol. 11 Iss. 4, pp. 149-158.
2. IEEE standard for floating-point arithmetic', IEEE Std. 754-2008, 2008, pp. 1–70.
3. Kuang S.-R., Wang, J.-P., Hong, H.-Y.: Variable-latency floating-point ALUs for
4. low-power applications', IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2010.
5. 4. Booth, A.D.: 'A signed binary multiplication technique', Q. J. Mech. Appl. Math.,1951, 4, (2), pp. 236–240.
6. de Dinechin, F., Pasca, B.: 'Large ALUs with fewer DSP blocks'. Int. Conf. on Field
7. Programmable Logic and Applications, 2009. FPL 2009, August 2009, pp. 250–255.
8. Oberman, S., Flynn, M.: 'Design issues in division and other floating-point operations', IEEE Trans. Comput., 1997, 46, (2), pp. 154–161.
9. Ho, C.H., Leong, P.H.W., Luk, W., et al.: 'Virtual embedded blocks: a methodology for evaluating embedded elements in FPGAs'. 2006 14th Annual IEEE. Symp. on Field-Programmable Custom Computing Machines, April 2006, pp. 35–44.
10. Andreas Ehliar "Area Efficient Floating-Point Adder and Multiplier with IEEE-754 Compatible Semantics", 2014 IEEE.
11. Dave Omkar.M, Aarthy.M "ASIC Implementation of 32 bit Floating Point ALU using pipelining" International Journal of Computer Applications(0975-8887) volume 94-No.17,May 2014.

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