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Consummation and Contrastive Analysis of Digital Modulation Schemes Using Cell Based Design

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Abstract*: *The rapid growth and fast approaching advancement in the communication technology has led to rapid increase in usage of digital communication technology over analog communication technology resulted in the process of passing information more securely from one to another. Advancement of technology resulted in cost effective SOC's utilized in designing a well implemented QPSK modulator with booth multiplier as an integral part of the design. This project deals with the critical parametric problems involved in technologies like cell sizing, timing constraints. The main criterion involved here is the usage of the IP cell based design as a subset of the communication system design. The progression of the design is evaluated in the Verilog compiler with the help of an IP integrator present in XILINX VIVADO 14.2. Basic HDL is used for its prior simulation in Xilinx RTL simulator. The main advantage of the design is the re usage of the modulator without writing and simulating the HDL code. The obtained design can be compared with other methods of modulations such as BASK, BPSK, BFSK in terms of critical parametric issues and then it is simulated that can obtain better results with high accuracy.

***Index Terms: Digital communication, modulation techniques, booth algorithm, QPSK, IP cores, SOC*.**

I. INTRODUCTION

The digital communication has more precedence than analog communication in many aspects. The usage of digital systems has been increased and will be increased further. The passage of information/data from source to destination would need some special digitally modulated techniques such as shift keying techniques [2]. In this paper a QPSK modulator with booth multiplier as the main module of the design. The whole design is a package of modules such as SIPO (serial in parallel out shift register), booth multiplier, and an adder [1]. The design of each module can be carried out through a technology named IP core technology in which the whole design will be packaged into a single cell. Since the modulation of a signal digitally has many advantages, for a better quality and efficient communication, digital modulation technique is employed. The main advantages of the digital modulation over analog modulation include available bandwidth, high noise immunity and permissible power. In digital modulation, a message signal is converted from analog to digital message, and then modulated by using a carrier wave [3]. There are different types of modulation techniques mainly such as ASK (amplitude shift keying), FSK (frequency shift keying), PSK (phase shift keying). The Amplitude modulation was developed in the beginning of the 20th century. Being the earlier, this modulation technique used to transmit voice by radio. It is used in electronic communication. In this modulation, the amplitude of the carrier signal varies in accordance with the message signal, in which the other factors like phase and frequency remain constant. This technique requires more power and greater bandwidth; filtering is very difficult. Amplitude modulation is employed in pc modems, VHF craft radio, and in moveable two-way radio. Unlike ASK, the frequency of the carrier signal varies in accordance with the message signal. This type of technique named as FSK i.e. frequency shift keying in which other parameters like amplitude and phase remain constant. Frequency modulation is employed in Is modified, then it affects the frequency. So, for this reason, this modulation is also comes under the frequency modulation and it was named as phase shift keying and can be known shortly as PSK. In this paper PSK for baud rate n = 1 and n=2 is simulated and they were named as BPSK and QPSK (binary and quadrature phase shift keying).techniques.

Generally, phase modulation is used for transmitting waves. It is an essential part of many digital transmission coding schemes that underlie a wide range of technologies like GSM, Wi-Fi, and satellite television. This type of modulation is employed for signal generation in al synthesizers, like the Yamaha DX7 to implement FM synthesis.

The main module used in the process of the design of the QPSK modulator is booth multiplier.

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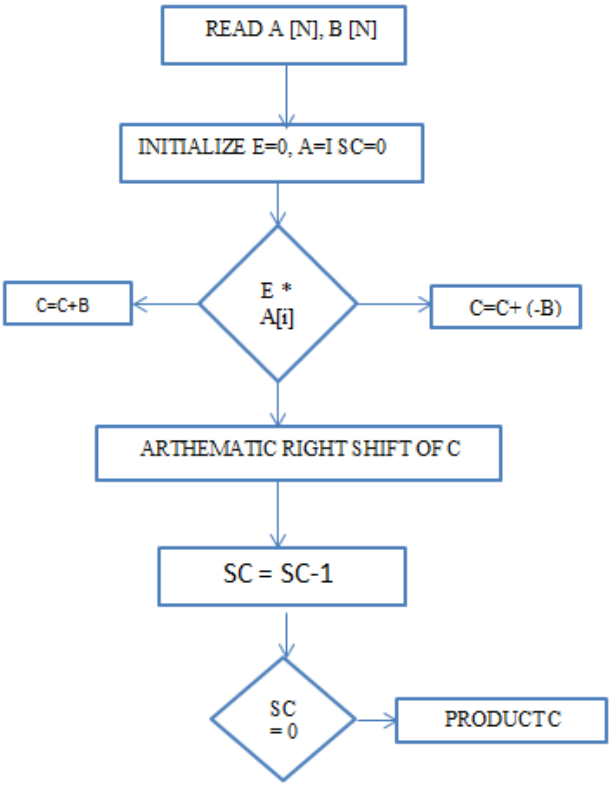

Fig 1: booth's algorithm [1]

The steps to perform method that is portrayed algorithamatically as shown below

- Read input eight bit information (multiplier A (n)) and carrier information (multiplicand B (n))
- Initialize one bit transition detector register E=0, and index bit I = zero and A=I Initialize sequence counter SC i.e. SC=0.
- Concatenate E and A
  If is 10 calculate B from the output C If is 01 add B to the output C
- Else if it is 00 or 11 perform arithmetic right shift on C and duplicate the worth of A[i] to E.
- Decrement the sequence counter by one i.e. SC= SC-1.
- If the operation is over, the ultimate products are going to be keep within the register C

The whole design has implemented or simulated in semi-custom pattern which is also can be known as standard cell based design. This can be done by packaging the whole design / project into single intellectual property cell/ standard cell of the core and hence named as IP core design. Below are the steps for converting an HDL module into an IP core standard cell [5].

- Behaviour modelling (HDL) of the module.
- Creating an IP.
- Modifying IP definition.
- Adding product guide to the IP cell/package which describes about the functionality of the cell.
- Reviewing and packaging of an IP
- Validating the new IP location.
- Addition of the repository path to add the IP in the catalogue of the IP.
- Using the new IP cell present in the catalogue of the IP in further complex design that can also be packaged into a single cell.

- From the definition the IP cell could be a reusable core block of knowledge which will be utilized in creating field programmable gate array(FPGA) or application specific integrated circuit(ASIC) for a product[4]. IP cores area unit a part of the growing electronic style automation (EDA) business trend towards continual use of antecedently designed elements. Ideally, an IP core ought to be entirely moveable - that's, able to simply be inserted into any merchandiser technology or style methodology. Universal Asynchronous Receiver/Transmitter (UARTs), central process units (C.P.U.s), local area network controllers, and PCI interfaces area unit all samples of IP cores. IP cores can be partitioned into three type's namely soft, firm and hard IP cores.

II. ARCHITECTURAL OVERVIEW

The architecture of the QPSK modulator for the proposed design shown in fig 2 consists of an adder, multiplier which was discussed above and a shift register in type SIPO mode, .i.e. serial in parallel out

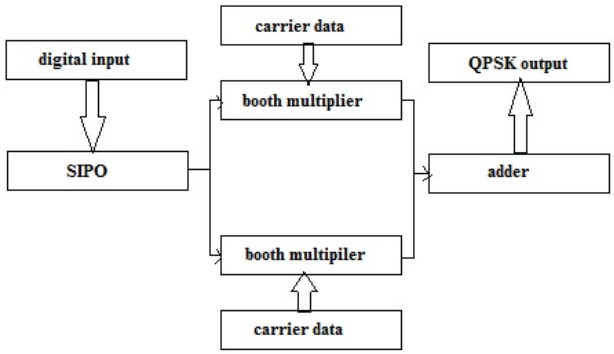

Fig 2: block diagram of Quadrature Phase Shift Keying [1].

Here the modulator has two multipliers to receive the even and odd bit data coming from the SIPO shift register. If we have a look at the structure the input data which is digital in nature is given to the SIPO register, the parallel output goes to the booth multiplier as a message signal and as a one of the input to the booth multiplier. The second input to the booth multiplier is the carrier signal which we give separately. Therefore the output of both multipliers will be combined by an adder whose output is the modulated output .i.e. QPSK modulator output [1]. The obtained QPSK modulation is compared with the other modulation techniques which were designed in previous to QPSK. .i.e. BASK, BFSK, BPSK etc. the modulation process in the BASK (binary amplitude shift keying) can be done by changing the amplitude of the carrier signal with the modulation signal such as message signal.

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The main modules in the BASK modulator shown in fig 2 are sine wave generator, MOD 5 counter and PISO shift register. A global clock is given to run every module present in the design. The main module in the design is the sine wave generator that can be simulated by changing the value in the register in a continuous manner.

At first the given input parallel data is converted to serial data by using a PISO shift register which is of 32 bits. The clock can be varied according to our requirement by using a MOD 5 counter. A 2_1

Multiplexer is used to produce the output based on the selection of high/low serial data coming from the PISO.

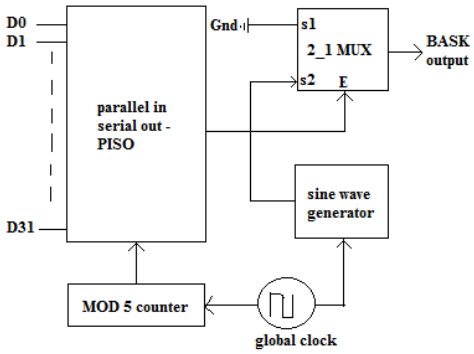

Fig 3: block diagram of Binary Amplitude Shift keying [2].

Unlike BASK, the modulation process in BFSK(binary frequency shift keying) can be carried out by the following process such that the carrier signal can be modulated in terms of frequency with respect to the input discrete signal.

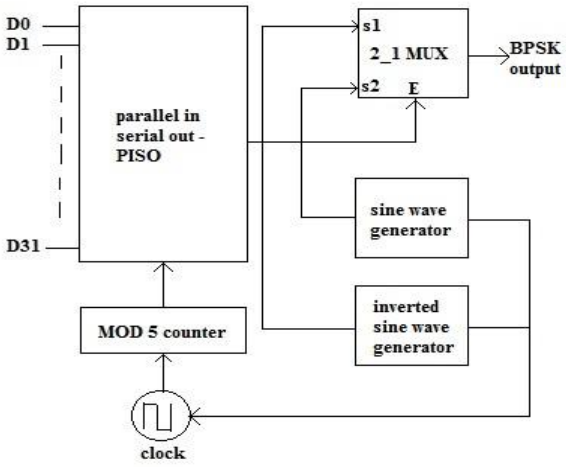

Fig 4: block diagram of Binary Frequency Shift keying [2].

The architecture of BFSK shown in fig 3 is same as the above with a slight change that can be made by taking two sine wave generators with two different clock frequencies. So, based on the serial data coming out from the PISO the output can be produced at the multiplexer.

The phenomenon in which the phase of the carrier can be varied with respect to the discrete input signal is known as binary phase shift keying. The architectural block shown in fig 4 is same as BFSK with an inverted sine wave generator replacing sine wave generator.

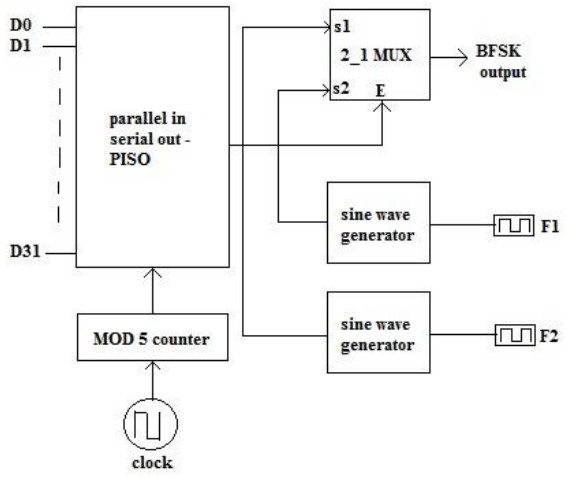

Fig 5: block diagram of Binary Phase Shift Keying [2].

III. RESULTS AND DISCUSSIONS

The multiplication result of booth multiplier represented in the form of simulated output as plotted below.

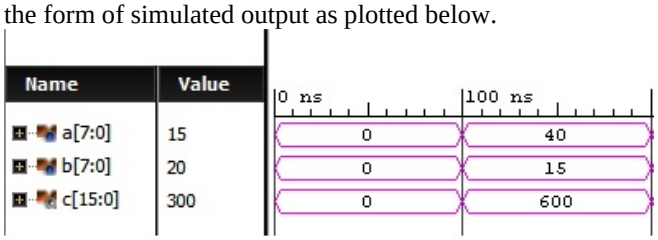

Fig 6: simulation result of booth multiplier.

Table I: areal analysis of booth multiplier.

Resource	Used	Available
I/O	35	200
Global buffers	1	32
Look up tables	38	53200
D flip flops	29	106400

The IP cell based block designs and their internal elaborated designs of the four modulation techniques are shown in figures 07-13.

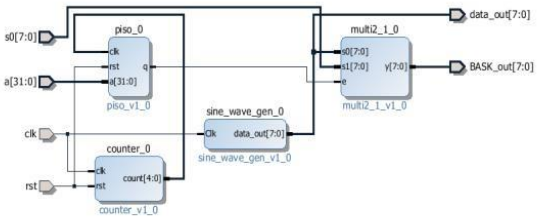

Fig 7: cell based block design of BASK.

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The above figure consists of a block diagram that was designed by using cells of PISO, MOD 5 counter, sine wave generator, 2_1 multiplexer. The clock that was globalized will be given to sine wave generator and to the counter.

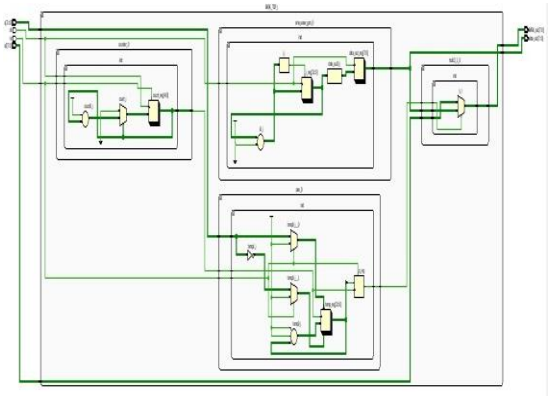

Fig 8: internal logic circuit of BASK.

The output of the counter is given as a clock to the parallel in serial out shift register. The output of the PISO is given as a selection line to the MUX so, depending on that output from PISO the MUX produces the output.

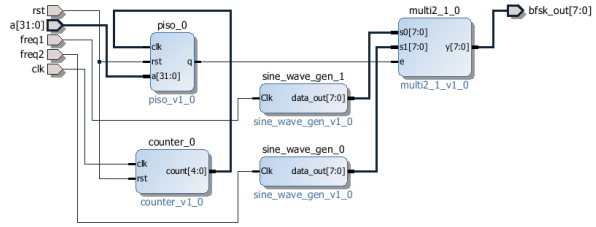

Fig 9: cell based block design of BFSK.

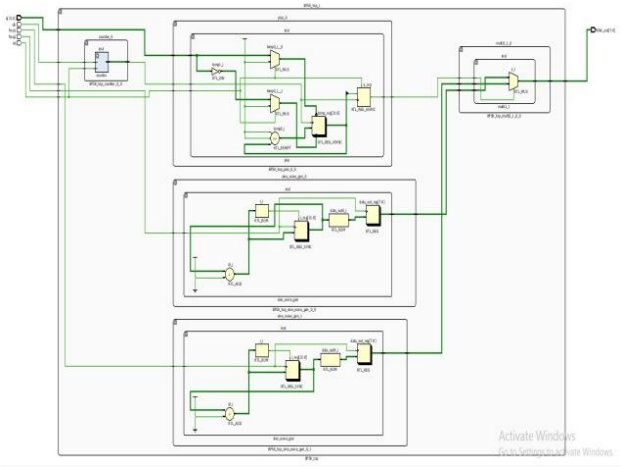

Fig 10: internal logic circuit of BFSK.

The above figure consists of a block diagram that was designed by using cells of PISO, MOD 5 counter, sine wave generator, 2_1 multiplexer. The clock will be given to the counter; the output of the counter is given as a clock pulse to the PISO which is of 32 bit. Here two sine wave generators were used with two different frequencies F1 and F2 the output of the two generators were given to the input of the 2_1 MUX. So, based on the output from the PISO the MUX produces the output either with respect to the frequency F1 or F2.

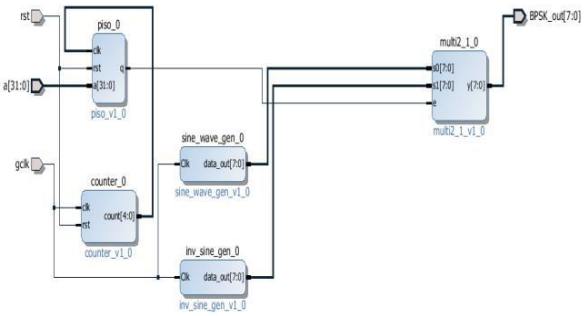

Fig 11: cell based block design of BPSK.

The above figure consists of a block diagram that was designed by using cells of PISO, MOD 5 counter, sine wave generator, 2_1 multiplexer. Like the previous one the clock was given to the MOD 5 counter to alter the clock frequency and the output is given as a clock pulse to the PISO.

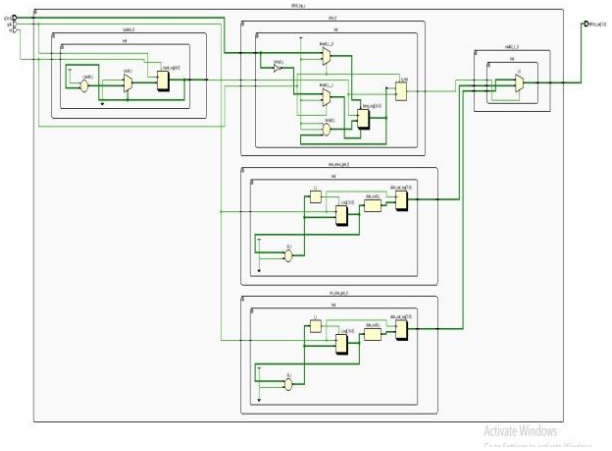

Fig 12: internal logic circuit of BPSK

Here the second generator of sine wave is replaced by the inverted generator of sine wave. The process is the same as in BFSK.

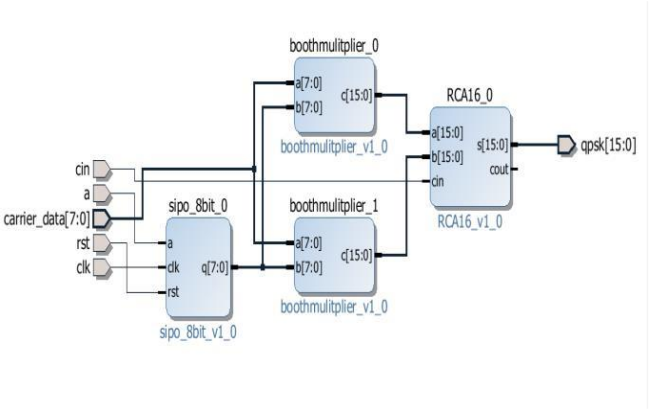

Fig 13: cell based block design of QPSK.

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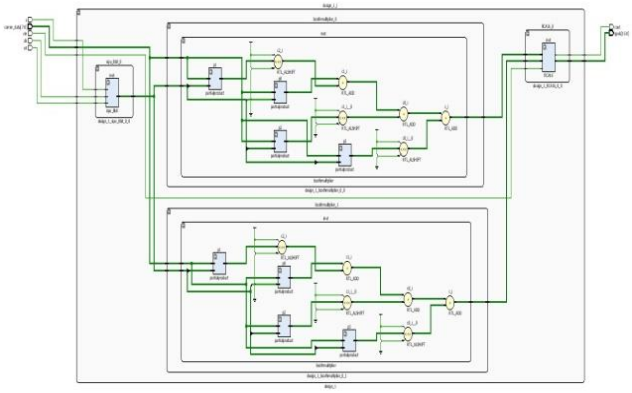

Fig 14: internal logic circuit of QPSK.

The figure above is a block diagram designed using SIPO cells, booth multiplier and an adder. Here the input to the SIPO is 8 bit the output of the SIPO is in parallel form and that data is given as inputs to the booth multipliers and referred to as the modulation signal, the other input to the booth multiplier is the carrier data of 8 bit discrete signal that the output of booth multipliers is given as inputs to the adder. Consequently, adder produces the output. Have a note about the use of two multipliers so that the parallel data is even and odd bits so one is odd and one is odd.

The simulated waveforms and area report of the four modulation techniques are shown in figures 12-15 and parametric issues in terms of size are compared with the help of a comparison table. The packaged IP cells of each modulation techniques are shown in figures 8-11.

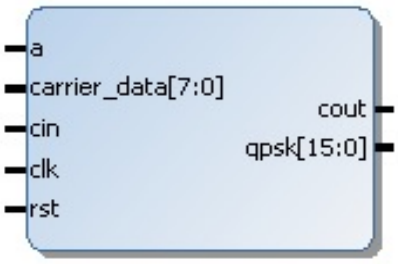

Fig 15: packaged IP cell of QPSK.

The above figure represents the packaged IP core block cell of quadrature phase shift keying modulator. That will be utilized in the complex designs further reducing the re-enacting of hardware description language code.

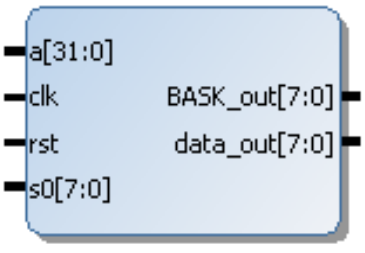

Fig 16: packaged IP cell of BASK

Fig 17: packaged IP cell of BFSK

Fig 18: packaged IP cell of BPSK

Table II: comparison table of area report between four digital modulation techniques

Parameter	BASK	BFSK	BPSK	QPSK
FF	137	181	181	58
LUT	111	191	191	97
I/O	58	44	42	22
BUFG	1	3	1	1

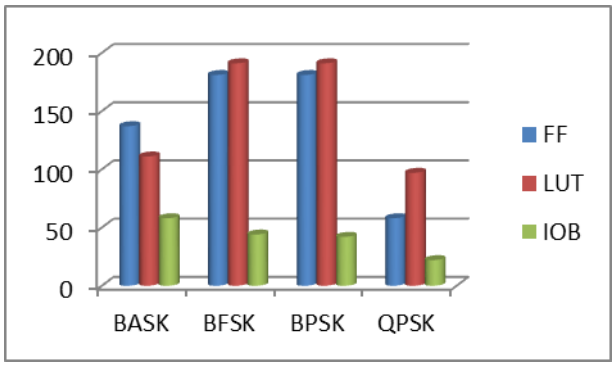

Fig 19: bar graph of comparison between different modulation techniques.

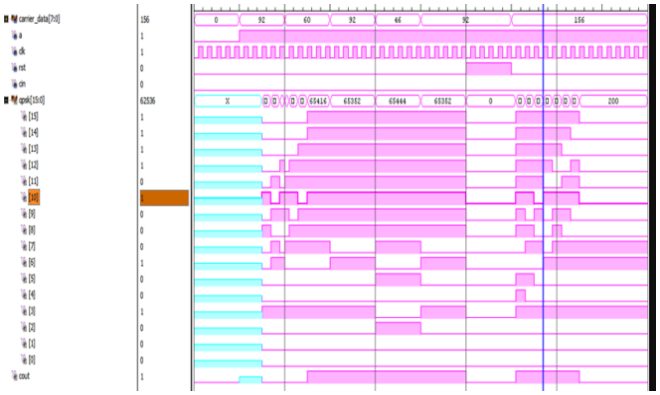

Fig 20: QPSK resultant wave forms.

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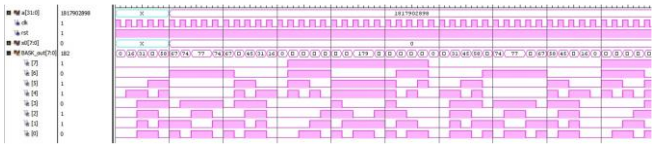
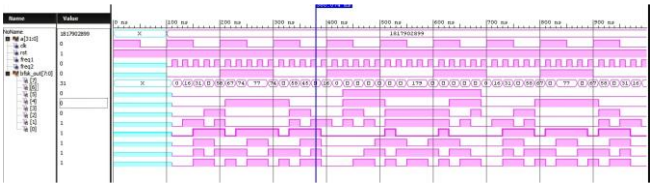


(A)



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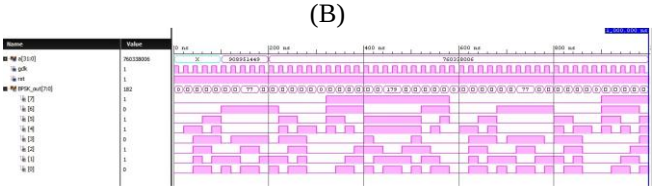

(C)

Fig 21: (A) BASK wave forms, (B) BFSK wave forms, (C) BPSK wave forms.

Here a new parameter has got to be thought of i.e. power. Here it absolutely was assumed because the space occupation had reduced by the comparative analysis between the previous and new designs of QPSK modulator.

IV. CONCLUSION

From this modulator design, a reusable IP core standard cell of a QPSK modulator can be obtained which will be designed by using different required packaged IP cells in an IP Integrator later on, the performance parameters will be compared with the previous versions to obtain a better result than the previous one. The communication system is designed for many wireless applications by using this design of QPSK modulator and the obtained design can be compared with other designs such as BASK,BFSK,BPSK. The time can be decreased by reusing these cells than composing and re-enacting the code without fail.

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