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Design of Low Power Comparator and Binary Code Encoder for 5 Bit Parallel Adc

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Abstract: ***ADC is one of the important building element many communication systems. Among all the ADC's flash ADC is preferred for low resolution and high speed applications. Flash ADC consists of comparator and encoder. There are many ways out in the world to implement an encoder and comparator which are the basic parts of ADC. The paper comprises of a comparator and a high speed, low power encoder with a sampling rate of 5Gs/s using different MOS technologies. Full adder based encoder and mux based encoder are designed using CPTL and transmission gate logic. The simulation results shows that power dissipation of the encoder using transmission gate logic is observed to be almost double that of the complementary pass transistor logic. The design and implementation are done by mentor graphics tool using 130nm technology with a supply voltage of 1.2V.***

Index Terms: ADC, Complementary Pass transistor logic (CPTL), Transmission Gate Logic, Flash ADC, Comparator, Encoder.

I. INTRODUCTION

Almost all the real time signals are analog in nature. It is hard to analyze and store the data as the computers, micro-processors are in the digital form. Therefore, the Analog signal should be converted to the digital signal in-order to store and analyze the data. Among the group of ADC's Flash ADC is chosen for high speed applications. Its resolution ranges from 6 to 8 bits. If the resolution increases the number of comparators used and the encoder size will increase which will result in the system complexity. This makes the system to be expensive.

Flash ADC is widely used efficiently in terms of its speed [1]. It is also named as Parallel ADC. It comprises of series of comparators and a priority encoder. Each comparator compares the input signal with reference signal [2]. When Vin is greater than the Vref the output of the comparator goes high else output goes low. This obtained output of the comparator is given as input to the priority encoder. Priority encoder generates the binary code based on the higher order input [3].

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II. DESIGN OF COMPARATOR

The primary block of parallel ADC is comparator. The main objective of the comparator is to compare the input signal with the ref signal and generates the thermometer code output [2]. Comparator is comprised of three blocks:

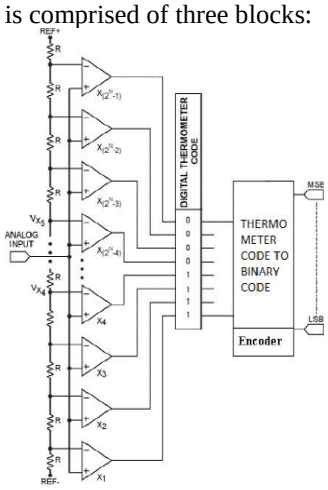

Figure 1: Flash ADC Architecture.

A. Pre-Amplifier:

Little variations between the inputs amplified to a large value is the main function of this block which uses a dynamic logic. When the clock=1, the preamplifier amplifies the given Inputs and the output is available at output node. When the clock=0, the output nodes are equalized and there by overdrive recovery time is reduced [2].

B. Latch:

Latch works in regenerate mode when the clock is low. When clock is disabled, current flows from supply to ground that gives rise to static power consumption [5]. When clock is enabled, memory element is operating in clear mode and the regenerating output nodes are at a voltage $V_{dd/2}$.

C. Buffer:

The goal of the output buffer is to convert the memory element output to 0 or 1. There are two parts in the circuit. It comprises of a self-biased differential amplifier and two inverters [6].

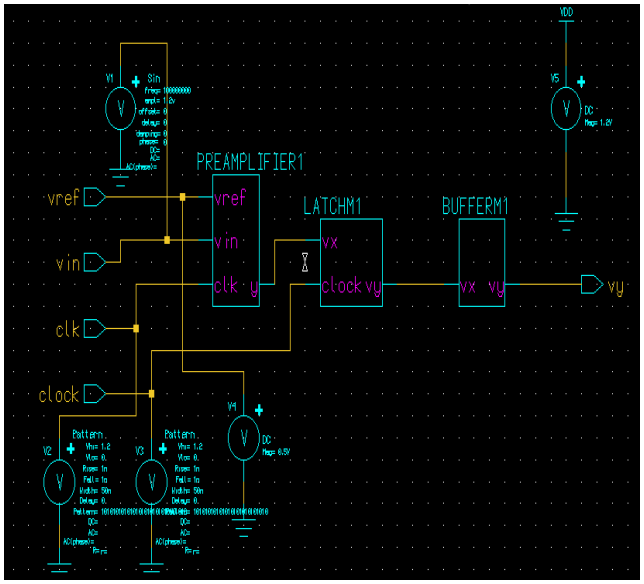

Figure 2: Block diagram of comparator.

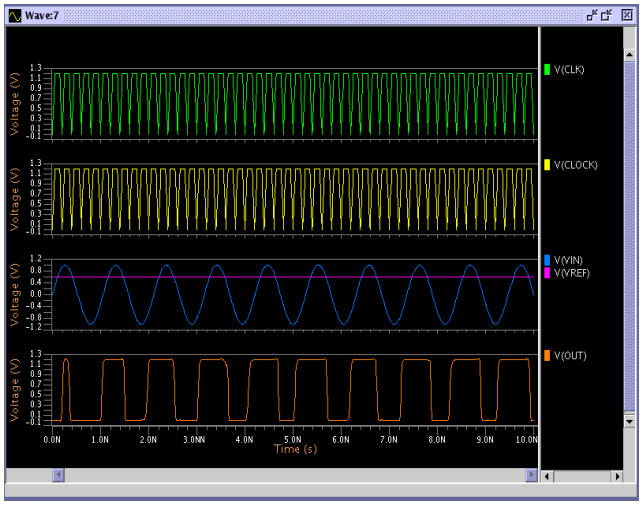

Figure 3: Output of comparator.

III. DESIGN OF ENCODER

A.Full Adder Based Encoder:

The main building block of Full adder Based encoder [7] is Full adder. An n-bit encoder requires $2^n - n - 1$ Full adders. The number of full adders required for implementing 5 bit encoder is 26. There are 32 input bits ($T^0 to\ T^{31}$) and 5 output bits ($B^0\ to\ B^4$) [3]. These 5 output bits are obtained from previously encoded input bits. The entire conversion process is carried out in two different levels. In the primary level the logical 1's at the input of the full adders will add up to give 2-bit binary outputs.

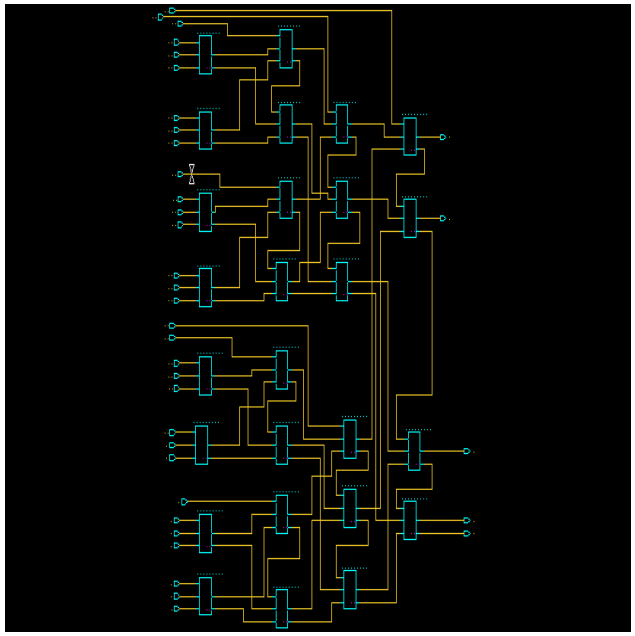

Figure 4: The block diagram of Wallace tree encoder.

a. 5-bit full adder based encoder:

In the secondary level the output of the previous stage acts like input and these inputs of the adjacent full adder cells are being added to result in a 3-bit binary outputs. This process is continued till we obtain the required output of n-bits. The efficiency of this encoder depends on the full adder implementation.

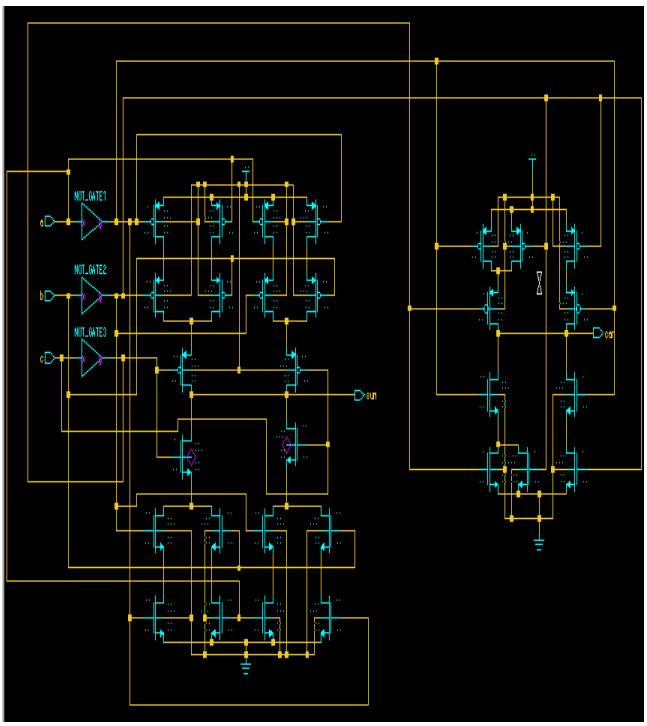

Figure 5: Full adder using Complementary pass transistor logic.

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b. full adder using complementary pass transistor logic:

Drawback of NMOS pass transistor technology is, it will not give strong one at the output. In order to obtain a strong zero and strong one we use inverter at the output. This method is called complementary pass transistor logic. The number of transistors used in complementary pass transistor logic is more and thus increases the complexity of the circuit.

c. full adder using transmission gate logic:

The parallel combination of P-MOS and N-MOS will represent a transmission gate logic. The P-MOS passes strong one and poor zero whereas the N-MOS passes strong zero and poor one. Both of them work simultaneously.

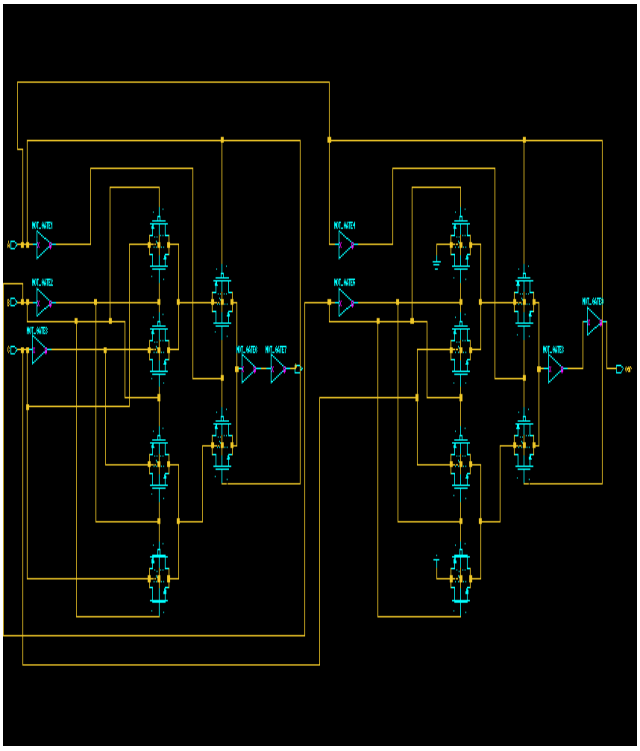

Figure 6: Full adder using transmission gate.

The main advantage of transmission gate is simplicity. The number of transistors can be reduced which decreases the complexity of the circuit.

B. Multiplexer Based Encoder:

The main building block of Multiplexer based encoder is 2:1 Multiplexer. It decreases the amount of hardware used than the Full adder based encoder. For n-bit encoder we use $2^n - 1$ Multiplexers with two inputs. The encoded output bits are considered as input signals for the multiplexers. If the number of input bits rises then the number of input selectors required will also increases.

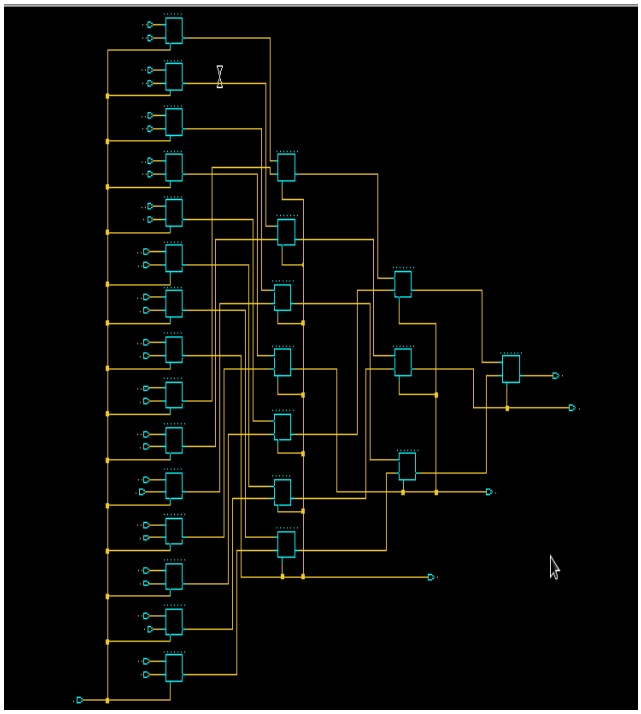

Figure 7: Multiplexer based encoder.

a. 2:1 multiplexer block:

Based on the selection bit one of the input is selected at the output. Performance of mux based encoder depending on 2:1 multiplexer implementation.

b. 2:1 multiplexer using complementary pass transistor logic:

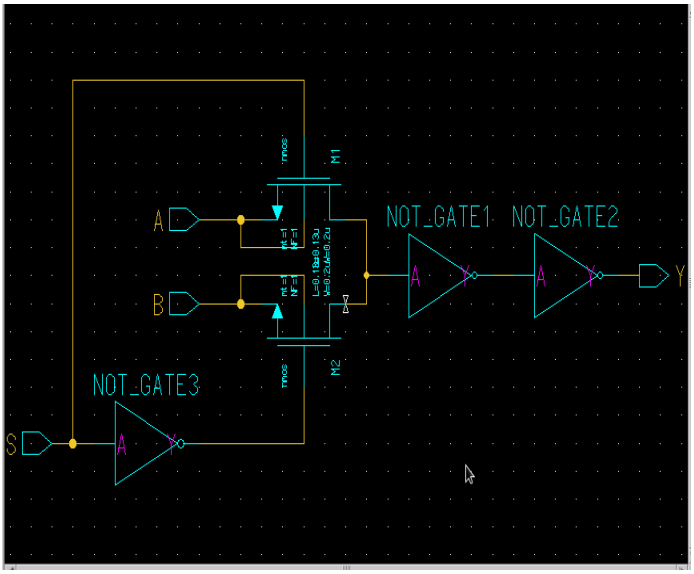

Figure 8: 2:1 Multiplexer using Complementary pass transistor logic.

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In order to obtain strong '0' and strong '1' we have placed two inverters at the output. When the selection line is '0' then the input 'B' is obtained at the output. When the selection line is '1'the input 'A' is obtained at the output. As the inverters are placed at the output of this logic the number of transistors required will increase which increases the circuit complexity. This is the major drawback that can be avoided in transmission gate.

c. 2:1 multiplexer using transmission gate logic:

In transmission gate the N-MOS and P-MOS are connected parallel to each other. There will be 3 input lines and 1 output line. Based on the selection line stage the output is obtained. This logic decreases the circuit complexity.

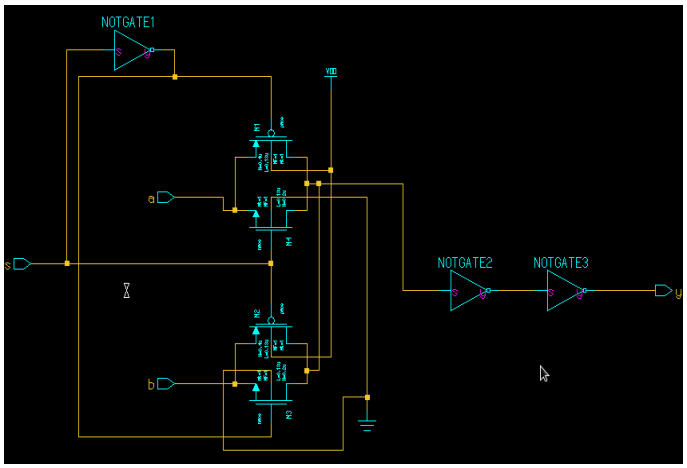

Figure 9: 2:1 Multiplexer using transmission gate logic.

IV. RESULTS

I. Power and Delay for Comparator.

	Power	Delay
Latch	10.259µW	1.0423ns
Output Buffer	10.274µW	1.0423ns
Pre-Amplifier	43.193µW	1.0423ns

II.Full Adder based encoder

	Full adder using CPTL	Full adder using TG	Full adder encoder using CPTL	Full adder encoder using TG
Resolution	-	-	5-bit	5-bit
Technology used	130nm	130nm	130nm	130nm
Reference voltage	1.2V	1.2V	1.2V	1.2V
Power Dissipation	356.96µW	1.2129 W	7.417µW	8.7269 W
Delay	307.19ps	300.10 ps	850.30 ps	41.553 ns

III.MUX BASED ENCODER

	MUX using CPTL	MUX using TG	MUX based encoder using CPTL	MUX based encoder using TG
Resolution	-	-	5-bit	5-bit
Technology used	130nm	130nm	130nm	130nm
Reference voltage	1.2V	1.2V	1.2V	1.2V
Power dissipation	60.520nW	75.37nW	595.45µW	972.51nW
Delay	39.96ns	79.916ns	132.34ps	217.82ps

V. CONCLUSION

With the help of mentor graphics tool, the encoder and comparator is implemented using 130nm technology with a supply voltage of 1.2V. The delay and power dissipation are the main parameters measured for the comparator and encoder. The power dissipation of the encoder using transmission gate logic is 972.51nW which is almost double that of the complementary pass transistor logic. The comparison of parameters is done.

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