International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-8 Issue-4, April 2019

An Odd Parity Genertor Design Using Nano-Electronics

S.Rooban, S.Rooban, K. Lakshmi Swathi, Ch.Monica, B.Shivaramakrishna

Abstract:*In the growing trends of digitalized world, devices with low-power consumption has marked their importance. When we go for CMOS technology, we find many Nano-scale computing problems. In order to avoid them we go for an emerging Nano computing technology which is a Quantum -dot Cellular-automata. QCA has potential advantages like high speeds, low power dissipation and higher device densities. In this paper, a 4-bit, 8-bit, 16-bit and a 32-bit odd parity generator are proposed which are highly dense and consume low power.*

Index Terms: *Quantum dot cellular automata, Odd parity generator, QCA designer, QCA pro.*

I. INTRODUCTION

Digital communication systems have been rapidly increasing with increase in data communication [1]. When we go for analog communication, we don't have flexibility options and the data processing options which are present in digital communication. We will then have less distortions and interventions compared to that of analog communication. Digital communication uses binary format where we have a fully on condition or a fully off condition. Digital circuits can be produced easily with a lower price and they can be more flexible [1-3]. Digital communication systems often use error detection and correction mechanisms, they use the concepts of parity generator and parity checker. These mechanisms can be realized in CMOS technology.

Presently, the entire electronic world is running through the CMOS technology but the disadvantage of it is that it has restrictions in the Nano-level. In order to reduce this restriction many researchers tried to find a substitute for the CMOS technology. Quantum Dot Cellular automata [QCA] is a very good substitute for CMOS technology.

QCA was introduced by C.S. Lent in 1993, after which they proposed many logical circuits, memory cells and some reversible logic circuits which are based on QCA. The first ever parity generator in QCA was proposed by Hashemi et al[4]. A 4-bit parity generator requires about 168 cells, and a 32-bit parity generator required about 1968 cells.

Manuscript published on 30 April 2019.
***** Correspondence Author (s)
S. Rooban*, ECE, KoneruLakshmiah Educational Foundation, Guntur, India.
K.LakshmiSwathi, ECE, Koneru LakshmiahEducational Foundation, Guntur, India.
Ch.Monica, ECE, KoneruLakshmiah Educational Foundation, Guntur, India.
B.Shiva Rama Krishna, ECE, KoneruLakshmiah Educational Foundation, Guntur, India.

Later a design y Angizi et al [5] in required about 188 cells and 1862 cells for 4- bit and 32-bit parity generator. In the next design Sheikhfaal et al [6]. used about 98 cells. Among all the most efficient and optimized design was proposed by Singh et al [7]. which requires about 87 and 1044 cells for implementing the 4-bit and 32-bit parity generators.

In this paper we proposed an innovative parity generator of 4,8,16 and 32-bits. The design introduced here occupies minimum area, minimum number of the cells and low time delays. The paper is organized as: background to QCA in the section 2 and in section 3 the QCA implementation of the proposed circuit, the simulation results of proposed design is discussed in section 4 and in section 5 the paper is concluded.

A. *BACKGROUND TO QCA TECHNOLOGY*

Quantum dot cellular automata it forms a new way for the digital communication. In order to represent binary 0 and binary 1 in QCA we have polarity -1 and polarity 1 as shown in fig. 1, Where p= -1 represents logic 1 and p=-1 represents logic 0.

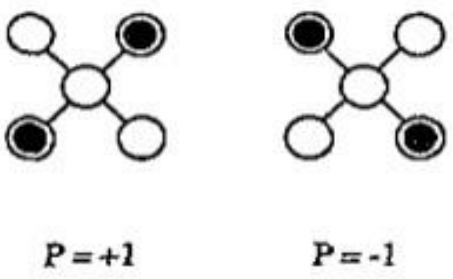


Fig. 1 Polarization

When we go for the QCA technology, we have a QCA cell which acts as the building block. It has four quantum dots with two of them with movable electrons. These electrons are always located diagonally opposite to each other and they have the capability of swapping these electrons to between the adjacent cells but not the neighboring cells. Basing on the position of the electrons the quantum cell attains a polarization. We generally have two types of polarizations as discussed p=+1 and p=-1. We also have two types of cells in QCA, regular and the rotated cells as shown in fig. 2. Rotated cells are generally used for wire crossings.

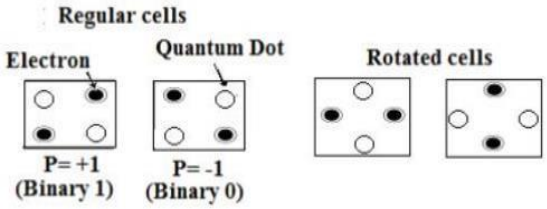


Fig. 2 QCA regular and rotated cells

In QCA the signal is transmitted through the QCA wire which is formed by placing the QCA cells with same polarization consecutively If the wire is made by a 90-degree phase shift then the output will be same as output as shown in fig. 3. If the wire is made by a 45-degree phase shift, then output gets inverted as shown in fig. 4. In QCA the electric current doesn't flow between the neighboring cells which leads to low power consumption.

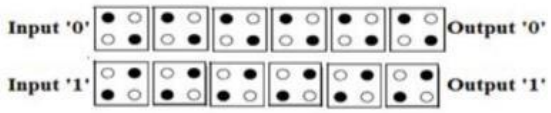


Fig. 3 QCA wire using regular cells

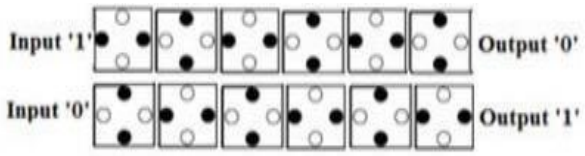


Fig. 4 QCA wire using rotated cells

In QCA we have clocking signaling mechanism, which involves four time zones as shown in fig. 5. The four time zones are Switch, Hold, Release and relax.

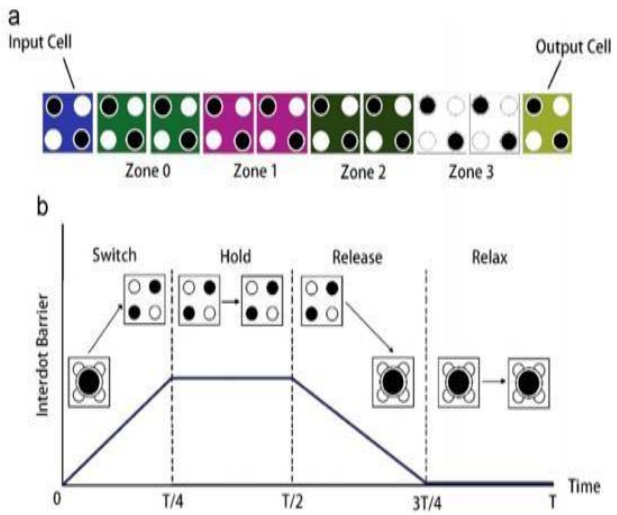


Fig. 5 clock zones

II. METHODOLOGY

In digital communication we usually encounter some errors as information in presented in binary format. For this reason, we add parity bits to the data we are sending to detect errors. When we go for 4-bit parity generator we have 4 inputs and one output, and the truth table is shown in table1.To implement this circuit in QCA we used a 3-input XNOR gates [7]. The proposed 4-bit layout uses only 26 cells, occupies 0.03μm^2 area and requires two clock cycles to generate the output which is accurate. The layout for 4-bit parity generator is shown in fig. 6.

The 8-bit odd parity generator proposed uses about 51cells and occupies 0.08μm^2 area and requires about three clock cycles to generate the expected output. The layout for the proposed 8-bit odd parity generator is shown in fig. 7.

In order to implement a 16-bit odd parity generator we will need 3-input seven exclusive- NOR and one 2-input exclusive NOR gates are needed. A 16-bit odd parity generator uses about 100 cells and occupies about 0.15μm^2 area and its layout in QCA designer is shown in fig. 8.

A 32-bit odd parity generator uses about 220 cells and occupies an area of 0.2980μm^2 and its layout is shown in fig. 9.

INPUTS				**OUTPUT**
X1	X2	X3	X4	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TABLE 1 Truth table for 4-bit odd parity generator

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication (BEIESP)

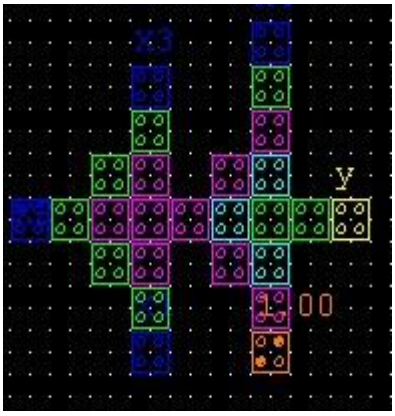


Fig. 6 4-bit odd parity generator

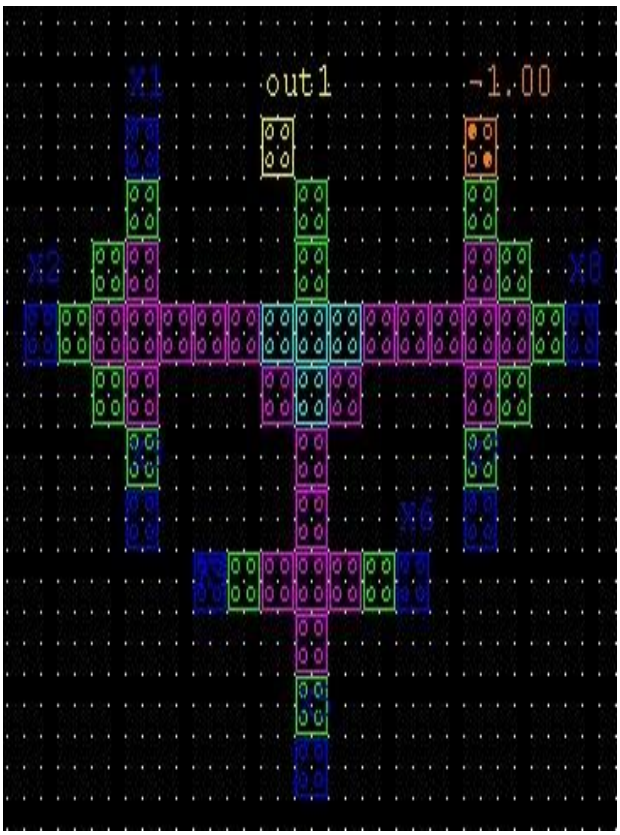


Fig .8 16-bit odd parity generator

III. SIMULATIONRESULTS

The proposed design is being implemented using the QCA designer version 2.0.3[8]. The output achieved in simulation tool is identical to that of the correct ones which ensures that the design is efficient in producing the required outcomes. The proposed 4-bit odd parity generator simulation results are being shown in fig. 10

IV. DISCUSSIONOFRESULTS

The comparison between the proposed parity generator and the existing generator is being given in detail in table 2 which is dealing with the aspects like the no. of cells each design consumed, the area occupied by them and the number of clocks it is taking to produce the expected output

Circuit	Number of bits	Cell count	Approximated area (μm^2)	Latency(clock)
Parity generator [4]	4	168	0.28	2.75 4
	8	408	0.80	5.25
	16	912	2.09	6.50
	32	1968	5.16	
Parity generator [5]	4	188	0.20	2.25
	8	369	0.49	2.25
	16	847	1.46	3.25
	32	1862	3.58	4.25
Parity generator [6]	4	98	0.11	2
	8	241	0.37	3
	16	537	1.04	4
	32	1167	2.67	5
Parity generator [7]	4	87	0.10	1.75
	8	213	0.30	2.75 3.75
	16	480	0.81	4.75
	32	1044	2.08	
Proposed parity generator	4	26	0.03	0.8
	8	51	0.08	0.8
	16	100	0.15	1
	32	220	0.298	1.25

Table 2 Comparison of proposed parity generator with the existing models

From the table 2 presented we can see that our proposed design beats all the existing ones in the aspects like cell count, area, and latency. The proposed 4-bit generator uses only 26 cells where the design in [7] occupies 87 cells.

Similarly, the highly dense 32-bit generator as shown in fig. 9 occupies over 220 cells which in turn is giving an cell optimization of 824 cells when compared with the earlier best design [7]. The overall improvement of the propose design is shown in fig. 11

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication (BEIESP)

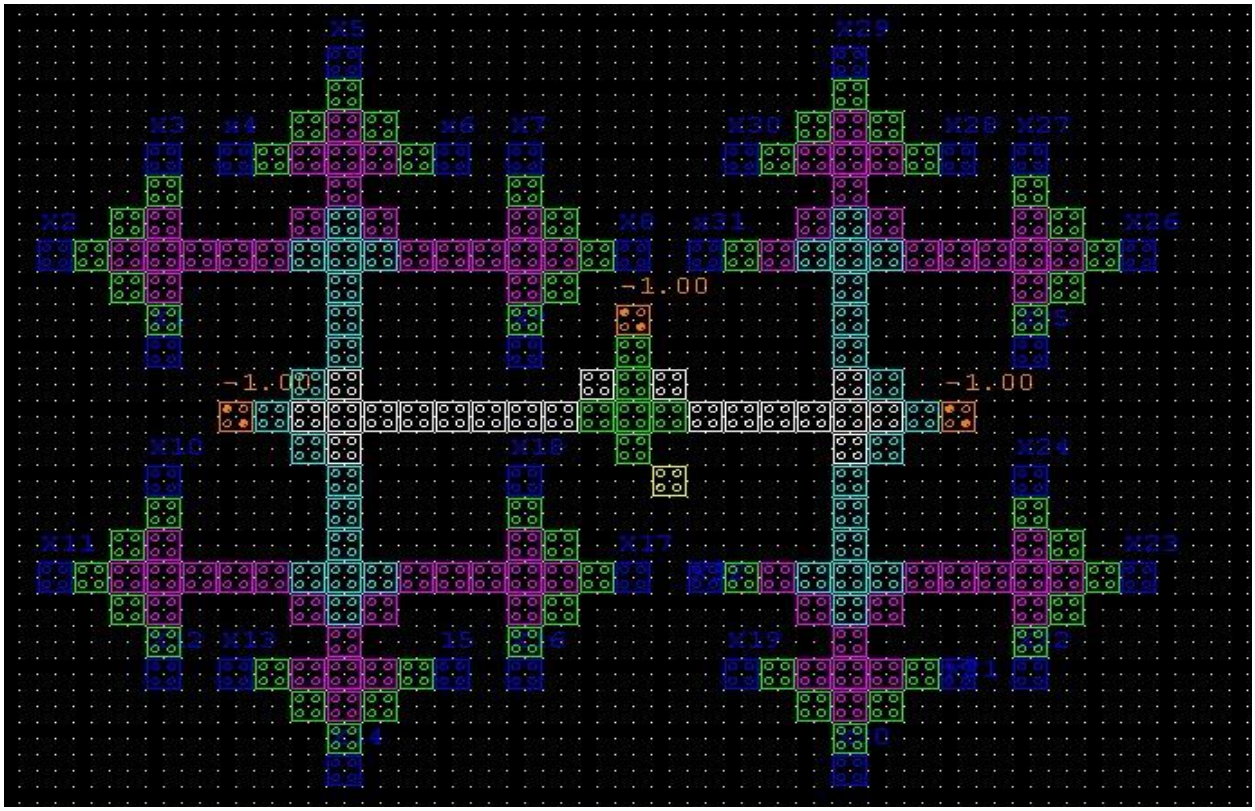


Fig. 9 32-bit odd parity generator

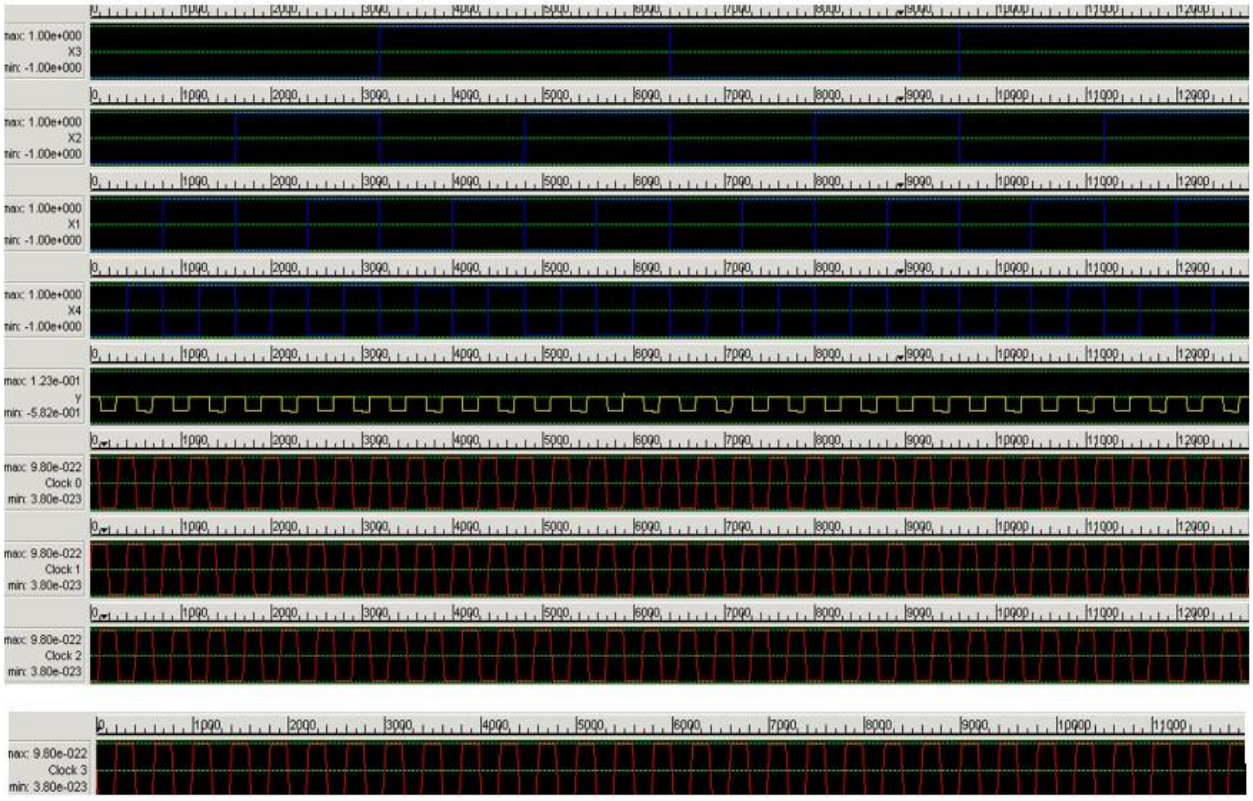
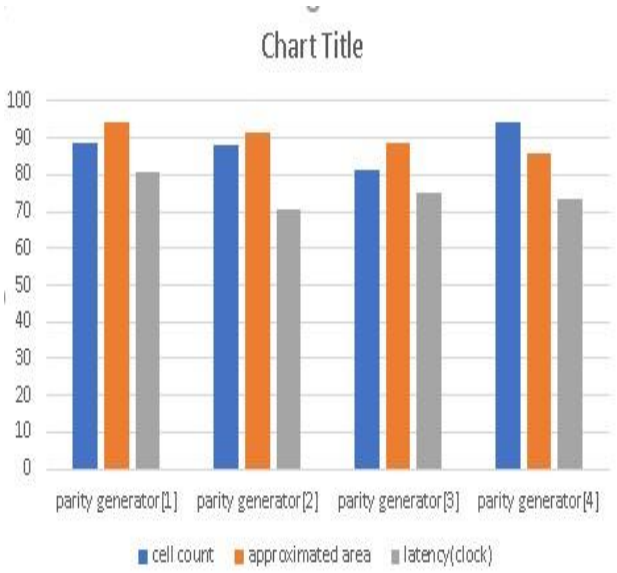


Fig.10 Simulation result of proposed 4-bit odd parity generator

V. CONCLUSION

In this paper, we have proposed parity generators of different lengths. The proposed 32-bit parity generator occupies only about $0.2980\mu m^2$ whereas the previous best one occupies $2.08\mu m^2$area. Hence the proposed design requires 85% less cells compared to [4]. Similarly, the proposed designs of 4-bit, 8-bit and 16-bit parity generator achieved an over-all improvement over the earlier designs [4-8] is shown in graph in fig.11for all the 32-bit generators. In addition, the energy dissipation of the proposed designs can also be realized by QCAPro[10] tools. The proposed designs can attain superiority over the other designs existing in terms of number of cells, the amount of area occupied, latency and energy dissipation.



REFERENCES

1. C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernstein, Quantum cellular automata, Nanotechnology 4 (1993)
2. P.D. Tougaw, C.S. Lent, Logical devices implemented using quantum cellular automata, J. Appl. Phys. 75 (1994) 1818–1825.
3. C.S. Lent, P.D. Tougaw, A device architecture for computing with quantum dots, Proc. IEEE 85 (1997) 541–557
4. S. Hashemi, R. Farazkish, K. Navi, New quantum dot cellular automata cell arrangements, J. Comput. Theor. Nanosci. 10 (2013) 798–809
5. S. Angizi, E. Alkaldy, N. Bagherzadeh, K. Navi, Novel robust single layer wire crossing approach for exclusive OR sum of products logic design with quantum-dot cellular automata, J. Low Power Electron. 10 (2014) 259–271
6. S. Sheikhfaal, S. Angizi, S. Sarmadi, M. Hossein Moaiyeri, S. Sayedsalehi, Designing efficient QCA logical circuits with power dissipation analysis, Microelectron. J. 46 (2015) 462–471
7. G. Singh, R.K. Sarin, B. Raj, A novel robust exclusive-OR function implementation in QCA nanotechnology with energy dissipation analysis, J. Comput. Electron. 15 (2016) 455–465
8. A.N. Bahar, S. Waheed, N. Hossain, M. Asaduzzaman, A novel 3-input XOR function implementation in quantum-dot cellular automata with energy dissipation analysis, Alexandria Eng. J. 56 (2017)
9. K. Walus, T.J. Dysart, G.A. Jullien, R.A. Budiman, QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata, IEEE Trans. Nanotechnol. 3 (2004) 26.
10. S. Srivastava, A. Asthana, S. Bhanja, S. Sarkar, QCAPro – An error-power estimation tool for QCA circuit design, in: 2011 IEEE International Symposium of Circuits and Systems (ISCAS), 2011, pp. 2377–2380

AUTHORS PROFILE

Dr.S.Rooban,currently working as an associate professor in the department of electronics and communication at K.L.E.F, Guntur, Andhra Pradesh, India.

K.Lakshmi Swathi, currently pursuing B.Tech in the streamof electronics and communication engineering at K.LE.F, Guntur,AndhraPradesh,India

Ch.Monica, currently pursuingB.Tech in the streamof electronics and communication engineering at K.LE.F, Guntur,AndhraPradesh,India

B.Shiva Rama Krishna, currently pursuingB.Tech in the stream of electronics and communication engineering at K.LE.F, Guntur,AndhraPradesh,India

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication (BEIESP)