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A Novel Methodology to Ameliorate the Transient Loading of Low Dropout Regulators (LDRs)

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Abstract: ***A new simple and mathematically based design methodology, which makes LDR output nearly insensitive to overshot or undershot jumps of the load current for long times, is proposed. This methodology is categorized on two stages. The first stage is the characterization of the LDR power transistor in the transient mode through the modeling of its terminal currents in terms of the normalized inversion charge density. As a completion of this stage, the channel charge density is computed in terms of the transistor terminal voltages by means of a charge-voltage compact MOS model. Based on this stage, the second one tends to represent the LDR in the transient loading conditions as a current mode feedback stabilizer for the floating terminal voltages of the LDR output transistor. The suggested procedure leans on cross coupling of the time second derivative of the LDR power transistor gate and drain voltages as well as currents. The power transistor transient terminal currents are modeled by the integral form of partial differential continuity equation where the channel charge density is linearly spatial approximated in terms of its boundary conditions. These boundary conditions are modeled in terms of the transistor terminal currents via EKV charge based compact model. The introduced methodology is applied to a standard CMOS of 0.18μm technology for NMOS power transistor which involved within a proposed negative LDR system that is validated using MATLAB R2014a. This technique realizes a pseudo static output keeping low values of the crossly coupled currents in order of nano Ampere or hundreds of micro Ampere for undershot or overshot cases, respectively, for a time period of more than 10^4 seconds. The proposed procedure figures out the principle of realizing a transient mode hardware of LDRs. This hardware can be coincided with the design requirements of LDRs in static and small signal dynamic modes.***

Index Terms: ***Low dropout regulator, transient response, gate and drain voltages cross coupling, channel charge density, EKV model, linearly spatial approximation***

I. INTRODUCTION

The low dropout regulator (LDR) is the system that provides the power managed loads with stable dc voltage source. In this situation of operation, the LDR output must be steady against variations of temperature, power supply voltage, and load current either in monolithic or abrupt way. In addition to the mentioned environmental or circuit parameters, the LDR output rigidity must be realized according to the fabrication parameters such as process variations, chip bonding and packaging. Under these conditions, all of the stability settings except that those suffering from abrupt temporal changes or what is scientifically known as transient events are completely outlined in accordance with the well-known static or small signal dynamic current-voltage model [1]. From this point of view, it is of importance to search some means that ameliorates the behavior of such important electronic device. In this regard, the main question is which approach will be applied to motivate the speed of the LDRs. To answer this question, there are some steps that must be followed to arrive such important goal. Let us now go to review some of the previously proposed algorithms in this field of research. Initially, increasing the AC bandwidth of the regulator circuits, using error current feedback mechanisms, achieves fastening of the LDR [2]. This enlarging in bandwidth is obtained because the current feedback requires a series-series feedback scheme. Such scheme coincides with low input and output impedances of the feedback controller of the LDR [3]. Consequently, the bandwidth will be increased. However, it was founded that this technique withstands the small abrupt changes that is emerged from the circuit bias point. This in turn requires constant LDR biasing current in face of large variations of load current. As a result of this, the design process will be so complicated in order to take into account the above sited conditions. This must be done while satisfying other settings such as small signal stability, high power supply rejection ratio, and noise suppression. Based on this treatment, the later mentioned settings that are originally related to the AC analysis techniques will be precisely estimated in the case where the transient ones will be empirically determined. In order to enhance the previously explained procedure, it is better to correlate the load current and the LDR circuit bias by means of adaptive biasing along with keeping current feedback criteria [4]-[6]. This assists the ability of the LDR to stabilize the small abrupt changes without constraining it to a unique operating point. Thus, the empirical estimation tends to be decreased because of the creation of some controlling parameter which is the load current.

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However, there is a mismatching between the large signal jumps and the defined AC responding time. This is due to the AC modeling which is based on the linearization of the nonlinear large signal model. As a solution to this problem, an additional circuitry must be provided in order to adjust the transient behavior of the LDR according to the large signal operation point of view [7]. This will provide a separate standard for the evaluation of the transient performance of the LDR taking into consideration the nonlinearities which are neglected in the previously proposed approaches. However, this is achieved on the price of increasing the power consumption and the complexity of adjusting the AC performance of the LDR. Additionally, although the large signal nonlinearities are taken into account; the spatial propagation nature of the MOS devices under transient conditions isn't taken into consideration. This effect makes the MOS transistor behaving as a quasi transmission line in which the charge carriers transport is modeled through the continuity equation [8]. Regarding the all of the previously illustrated procedures, it is found that it is wanted to systematically, not empirically, enhance the transient response of LDR. As a tool for this achievement, it is intuitive to relate the continuity equation based transient of MOS device to the mathematical frame of the transient loading of LDRs. From this point of view, this paper is organized as follows. Section II discusses the proposed approach. The simulation results are outlined in section III. The final conclusions are extracted in section IV.

II. THE PROPOSED APPROACH

The goal of this section is to establish a general mathematical frame available to be coupled to any design procedure of LDR system. Based on this mathematical tool, the introduced methodology depends on stabilizing the transient loading of the LDR output power transistor which is the common device for all LDR schematics whatever they are. Additionally, it is assumed that there is no body effect and the power supply voltage, which is supposed un-switchable and required to be regulated, is connected to the power transistor source. According to these assumptions, the remaining controlling parameters are the power transistor's gate and drain voltages as well as currents. Before going forward to formulation of the proposed methodology, it is of importance to retrieve the relationship of the previously mentioned controlling parameters. In this regard, the transient currents of MOS device are determined in terms of its normalized channel inversion charge density which can be obtained by solving the partial differential continuity equation. In the case of LDR power transistor, the channel length is short and the difference between the drain and source voltages is small. As a result, the normalized channel charge density can be approximated as a spatial linear function in terms of the boundary conditions of the continuity equation. Accordingly, the channel normalized charge density, $r_s(\xi, t)$, as a function of the normalized, with respect to its length, channel position, ξ, and time, t, can be determined as:

$$r_s(\xi,t) \cong r_s(0,t) + \left[r_s(1,t) - r_s(0,t) \right] \xi \quad (1)$$

where $r_s(0, t)$, & $r_s(1, t)$ are the boundary conditions of the continuity equation at the channel's source and drain, respectively. These conditions are mathematically compact described by means of EKV charge-voltage formula as [9]:

$$\frac{1}{V_T}\left\{\frac{|V_G(t)-V_B(t)|-|V_{th}|}{N_V} - \left[|V_S(t)-V_B(t)|\right]\right\} = \ln r_s(0,t) + \theta r_s(0,t) \quad (2)$$

and

$$\frac{1}{V_T}\left\{\frac{|V_G(t)-V_B(t)|-|V_{th}|}{N_V} - \left[|V_D(t)-V_B(t)|\right]\right\} = \ln r_s(1,t) + \theta r_s(1,t) \quad (3)$$

Referring to the previous equations, V_T is the thermal electro-dynamic voltage, V_G is the gate voltage, V_B is the bulk voltage, V_{th} is the threshold voltage, N_V is the voltage slope factor, V_S is the source voltage, θ denotes a dimensionless factor which models the quantum non-idealities effects resulted from band gap widening, and V_D is the drain voltage. The transient terminal currents, on the other hand, of MOS transistor in terms of EKV model can be formulated as [8]-[9]:

$$I_D(t) = I_{avr}(t) - \theta N_\rho C_{ox} V_T W L \frac{d}{dt}\int_0^1 \xi\, r_s(\xi,t)\, d\xi \quad (4)$$

$$I_{avr}(t) = -\theta \mu_0 \frac{K_1}{K_2} V_T^{\,2} N_\rho C_{ox} \frac{W}{L} * \left\{ r_s(1,t) - r_s(0,t) + \frac{1}{2}\left(\theta - \frac{1}{K_2}\right) + \left[r_s^{\,2}(1,t) - r_s^{\,2}(0,t)\right]\right\} - \frac{\theta}{3K_2}\left[r_s^{\,2}(1,t) - r_s^{\,2}(0,t)\right]\Big\} \quad (5)$$

and

$$I_G(t) = W L C_{ox} \frac{d}{dt}\left\{\kappa\, \theta\, V_T \int_0^1 r_s(\xi,t)\, d\xi - \kappa \left|\psi_p\right| - \left[V_G(t) - V_B(t)\right]\right\}$$

$$\& \quad \kappa \triangleq \begin{cases} -1 & for\ NMOS \\ 1 & for\ PMOS \end{cases} \quad (6)$$

In this set of formulas, I_D is the dynamic drain current, I_{avr} is the spatial average current, N_ρ is the charge slope factor, C_{ox} is the oxide capacitance per unit channel area, W is the channel width, L is the channel length, μ_0 is the low field mobility, K_1 & K_2 are terminal voltage dependent parameters that model the mobility reduction effect, I_G is the dynamic gate current rejecting the tunnelling effect, κ is an indicator of the type of MOS transistor, and ψ_p is the pinch-off surface potential. The substitution of Eq.(1) into Eqs.(4-6) leads to making terminal currents to become:

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$$I_D(t) = I_{avr}(t) - \theta C_{ox} N_\rho V_T W L \frac{d}{dt}\left(\frac{r_s(0,t)}{6} + \frac{r_s(1,t)}{3}\right) \quad (7)$$

and $$T_G(t) = -wLC_{ox}\frac{d}{dt}\{0.5\ \theta V_T [r_s(0,t) + r_s(1,t)] - V_G - \psi_P\} \quad (8)$$

The EKV model parameters, that are depending upon the terminal voltages, can mathematically be represented as:

$$\theta = 2\left(1 + A_{qm} C_{ox}\left[1 - \frac{N_\rho}{4}\right]\{2 q \varepsilon_{Si} N_{bch} |\psi_p|\}^{-1/6}\right)^{-1} \quad (9)$$

$$|V_{th}| = \begin{cases} V_{fb} + 2\phi_F + V_{sh} + \frac{\Gamma^2}{2}\left(\xi_c\left\{1 - \frac{N_b}{N_{bch}}\right\} + \sqrt{\left[\xi_c \frac{N_b}{N_{bch}}\right]^2 - \frac{N_b}{N_{bch}}\left\{\xi_c^2 - \frac{8\phi_F + 4V_{sh}}{\Gamma^2}\right\}}\right) - T_G\left[\frac{\Gamma^2}{\Gamma_g^2}(2\phi_F + V_{sh}) - \frac{2\Gamma\rho_{fc}}{\Gamma_g^2 C_{ox}}\sqrt{2\phi_F + V_{sh}}\right] & \text{for } N_b > N_{bch} \\ V_{fb} + 2\phi_F + V_{sh} + \Gamma\sqrt{2\phi_F + V_{sh}} + \left[\left(\frac{\Gamma\xi_c}{2}\right)^2 - 2\phi_F - V_{sh}\right] * \left\{\frac{\Gamma}{2}\left[2\phi + |V_{SB}|\right]^{-0.5} + \frac{N_b}{N_{bch}}\left[\left(\xi_c \frac{N_b}{N_{bch}}\right)^2 - \frac{N_b}{N_{bch}}\left(\xi_c^2 - \frac{8\phi_F + 4|V_{SB}|}{\Gamma^2}\right)\right]^{-0.5}\right\} - T_G\left[\frac{\Gamma^2}{\Gamma_g^2}(2\phi_F + V_{sh}) - V_{sh}\right] - \frac{2\Gamma\rho_{fc}}{\Gamma_g^2 C_{ox}}\sqrt{2\phi_F + V_{sh}} & \text{Otherwise} \end{cases} \quad (10)$$

$$N_V = 1 + N_\rho - T_G\frac{\Gamma^2}{\Gamma_g^2}\left[1 - \frac{\rho_{fc}}{\Gamma C_{ox}}(2\phi_F + |V_{SB}|)^{-0.5}\right] + \left\{1 - T_G\frac{2}{\Gamma_g^2}\left(\Gamma\sqrt{2\phi_F + |V_{SB}|} - \frac{\rho_{fc}}{C_{ox}}\right)\right\}^{-1} \quad (11)$$

$$N_\rho = \left(\frac{N_{bch}}{N_b}\left[\xi_c^2\left\{\frac{N_b}{N_{bch}} - 1\right\} + \frac{8\phi_F + 4|V_{SB}|}{\Gamma^2}\right]\right)^{-0.5} + \left\{1 - T_G\frac{2}{\Gamma_g^2}\left(\Gamma\sqrt{2\phi_F + |V_{SB}|} - \frac{\rho_{fc}}{C_{ox}}\right)\right\}^{-1} \quad (12)$$

$$K_1 = \frac{\varepsilon_{si} E_0}{\theta C_{ox} N_\rho V_T}\left\{0.5 - \left(1 + 2\Gamma^{-1}\sqrt{|\psi_p|}\right)^{-1}\right\}^{-1} \quad (13)$$

$$K_2 = K_1 + \frac{2|\psi_p|}{V_T}\left(-1 + 2\Gamma^{-1}\sqrt{|\psi_p|}\right)^{-1} \quad (14)$$

$$V_{sh} = V_T \ln\left(2\theta N_\rho \Gamma^{-1}\sqrt{|\psi_p|}\right) + A_{qm} * \sqrt[3]{2 q \varepsilon_{Si} N_{bch} |\psi_p|} \quad (15)$$

$$|\psi_p| = \begin{cases} \left(\frac{\Gamma_g/2}{\Gamma^2 + \Gamma_g^2}\sqrt{4\left(\Gamma^2 + \Gamma_g^2\right)\left[|V_G - V_B| - V_{fb}\right] + \left\{\Gamma\Gamma_g\right\}^2} - \Gamma\Gamma_g\right)^2 & \text{for } T_G = -1 \\ |V_G - V_B| - V_{fb} - \Gamma^2\left(\sqrt{\frac{|V_G - V_B| - V_{fb}}{\Gamma^2} + \frac{1}{4}} - \frac{1}{2}\right) & \text{for } T_G = 1 \end{cases} \quad (16)$$

In the above mathematical formulas, A_{qm} represents the proportionality constant between the silicon band-gab voltage shift and the silicon charge, q is the electron charge, ε_{si} is the silicon permittivity, N_{bch} is the channel doping concentration of the substrate, V_{fb} is the flat band voltage, ϕ_F is the Fermi potential, V_{sh} is the channel voltage shift, Γ is the body effect coefficient, ξ_c is the normalized characteristic depth, N_b is the substrate doping, T_G is an indicating parameter of similarity (T_G = 1) of the gate doping corresponding to the substrate doping, Γ_g is the depletion factor in the poly-silicon gate, ρ_{fc} is the fixed charge density, and E_0 is the starting electric field of mobility reduction effect. The controlling terminal voltage parameters of the studied power transistor and/or their temporal derivatives can form a stabilization feedback system consisting of two differential equations. These equations can be put in any formula at the cost of hardness of hardware realization. Additionally, the equation parameters are so hard to be optimized. The proposed set, resulting from the feedback modulation, aims at stabilization of the LDR output. This output is located at the drain terminal of the power transistor. Ideally, the LDR nominal output value must be rapidly restored keeping low power consumption and allowable voltage ranges when it is objected to impact loading.

For sake of simplicity, we suppose a simple second order system, the operation of which depends on cross-coupling control between the gate and drain voltages as well as currents and the input of which is the load current. This system can be described by the following mathematical relations:

$$I_R = I_D - I_L \quad (17)$$

$$\frac{d^2 V_G}{dt^2} = a_1 I_R \quad (18)$$

$$\frac{d^2 V_D}{dt^2} = a_2 I_G \quad (19)$$

Here, I_L denotes the load current, and a_1 & a_2 represent the parameters of the proposed system of equations. The equation parameters are optimized in such a way that the aimed goals of our methodology will be realized. This cross coupled system is the simplest one, the terminal voltage of which can't be controlled by its own current in the transient mode, that can be introduced. As the least order, the second order system is selected to include the probability of scillation for some of its parameters in order to realize bounding of other parameters in their allowed limits.

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This proposed methodology will be validated in the next section. The load current transition of the suggested system is assigned to vary as:

$$I_L = I_{L_f} - \left(I_{L_f} - I_{L_i}\right)e^{-S_c t} \quad (20)$$

In this situation of mathematical representation, I_{Lf} symbolizes the final value of the load current transition, I_{Li} denotes its initial value, and S_c stands for a transition scaling factor. Taking this equation into consideration, the load transition is supposed to be represented as an exponential sweep from the initial to the final values with sweeping width lies in the range of the load current. This exponential representation of the load transient is selected to simplify the differentiation of the load currents without trapping into temporal jumps of derivatives. As an overall, our procedure can be summarized through the following few steps:

Step 1: Modeling of the channel inversion charge density of the LDR power transistor in terms of its value at the channel position bounds as depicted by Eq.(1).

Step 2: Formulating of the channel charge density at the channel bounds of the LDR output transistor as a function of the terminal voltages by means of a compact charge based MOS model as described by Eqs.(2 & 3), Eqs.(9-16).

Step 3: Determining the transient transistor currents via the integral form of the continuity equation as shown by Eqs.(4-8).

Step 4: Making a system of non linear temporal differential equations in terms of the floating voltages of the LDR output transistor such that the input of this system is the transistor transient load current as represented by Eqs.(17-19).

Step 5: Modeling of the transient load current in a proper way according to the physical switching response as introduced by Eq.(20).

Step 5: Optimizing of the parameters of the proposed system of the differential equations to match the requirement of a stable voltages under the constraint of low power consumption.

Step 6: Realizing the LDR hardware taking into account the proposed methodology, the transient model of general purpose MOS transistors [7], and static as well as small signal dynamic modes design requirements.

III. SIMULATION AND RESULTS DISCUSSION

Here, it is the time to turn our attention to the methodology of the proposed design that enhances the LDR transient response. To carry out this task, we are going to solve the system of Eqs.(18-19) in order to optimize the values of the parameters a_1 and a_2 required to achieve a better transient regulation simultaneously with low power consumption. The simulation settings is depicted in Table I.

Table I: Simulation Settings for Testing The New Design Methodology of LDR.

Simulation Settings		Value
Power transistor		NMOS
CMOS technology [10]-[11]		0.18µm
V_B		-1V
V_S		-1V
Temperature		300K
W		9000µm.
L		0.46µm
I_L		[0,0.1]A
S		$2x10^{11}$ A/sec
Time duration of all simulations		10^4sec
$r_s(0/1,t)$ calculation in terms of terminal voltages		using MATLAB 2014a defined inverse function "lambertw"
Solver		ode23tb
In case of overshoot	a_1	-0.01
	a_2	1
	$V_G(0)$	0
	$V_D(0)$	-0.9
	The remaining initial conditions	0
In case of undershoot	a_1	0.01
	a_2	1
	$V_G(0)$	-0.9
	$V_D(0)$	-0.9
	The remaining initial conditions	0

In order to satisfy the illustrated objective of our methodology, the model equation parameters along with the initial conditions are setting according to that indicated in Table I. In this regard, the switched parameters a_1 and $V_G(0)$ change their values associated with the load current transition case. This switching action matches with the load current transition mechanism which is actually based on the switching of the loads that represent the power circuits managed by the LDR [3]. This indicates that abruptly changing of the load current means switching events. Based on this behavior, it is intuitive to assume switched parameters or initial conditions.

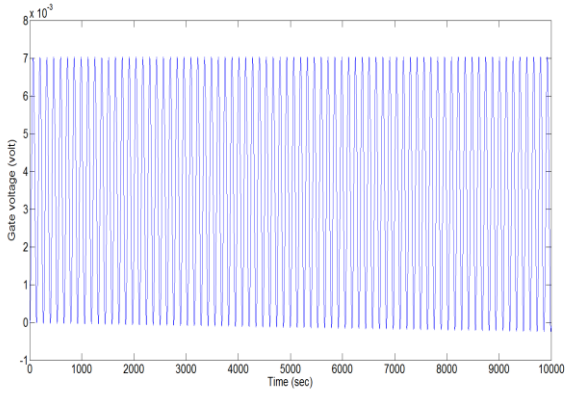

Fig.(1) Dynamic gate voltage versus time in case of overshot

Fig.(1) illustrates the dynamic gate voltage in the case of load current overshot which oscillates within a small range of mV. The deviation of the output voltage from initial value in this transition situation is shown in Fig.(2).

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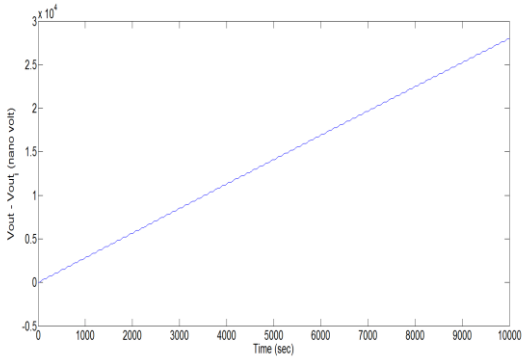

Fig.(2) Deviation of the output voltage from initial value versus time in case of overshot

Regarding to this graph, it is noted that there is an increasing case of instability. However, having a big insight look to the amount of temporal deviation, it is found that its value is in order of μV during a time of about 10^4sec. This allows the small signal noise suppression techniques to easily restore the nominal value of the output voltage. To continue our plane of optimization, Fig.(3) depicts the gate current for overshot state of load current transition.

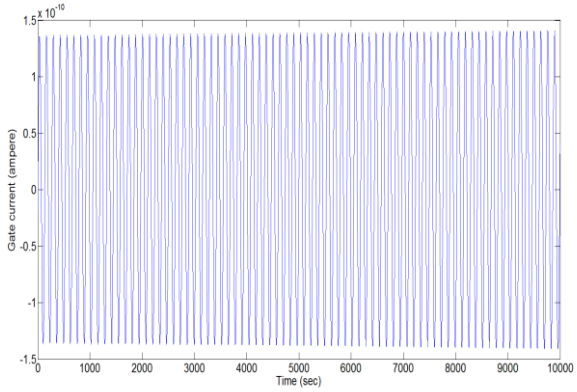

Fig.(3) Gate current versus time in case of overshot

In this plot, it is observed that the gate current oscillates within a very low range in the order of parts of nA. On the other hand, the difference between the drain and load currents in the case of upward jump is plotted in Fig.(4).

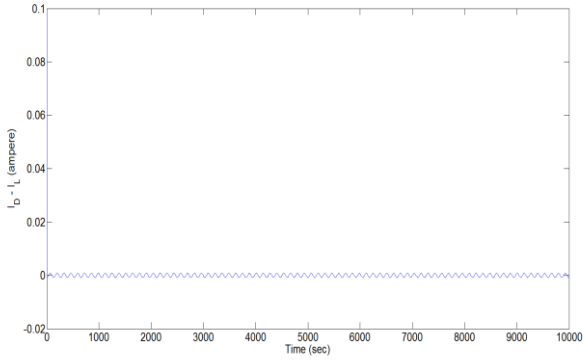

Fig.(4) Difference of the drain current and load current versus time in case of overshot

It is turned out to note that this difference acts as a quasi impulse initiated at the starting instant of time and then instantaneously goes to oscillate in hundred ranges of μA. The deviation of the output voltage from initial value, on the other hand, in case of undershot is displayed in Fig.(5). This plot shows the same results outlined in Fig.(2) with the exception that the output voltage is decreasingly varied.

Fig.(6) indicates the dynamic gate voltage in downward transition of the load current. The variation of this figure demonstrates that the gate voltage degenerates in the range of about -0.2 volts during the specified time of simulation. Additionally, the very slow variation rate illustrated in this graph allows the small signal stabilization procedures to adjust the gate voltage. The gate current in the state of down jumping is drawn in Fig.(7). That current has initial jumps and stabilizes, in quasi no time, at a specified value in the range of tenths of nA. This behaviour of the gate current transition allows restoring its nominal zero average value.

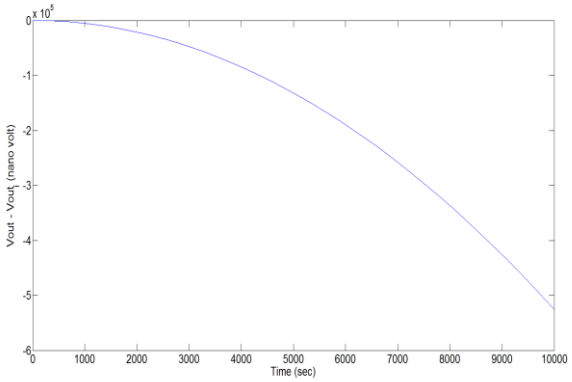

Fig.(5) Deviation of the output voltage from initial value versus time in case of undershot

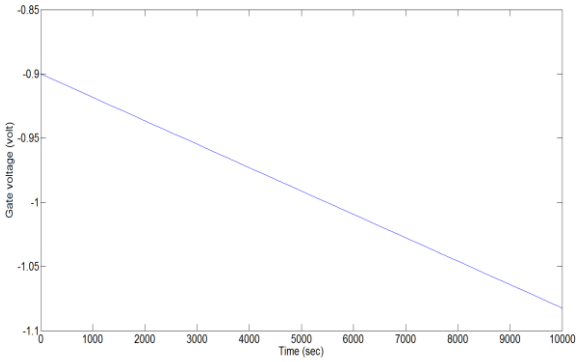

Fig.(6) Dynamic gate voltage versus time in case of undershot

Fig.(8) demonstrates the difference of the drain and load currents in the state of downward transition. This graph illustrates a jump of the concerned parameter at the initial time point and then an instantaneous decaying to values in the order of nA.

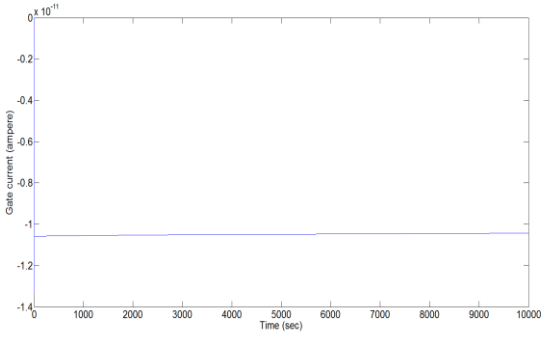

Fig.(7) Gate current versus time in case of undershot

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As an overview of the illustrated figures, it is noted that in spite of rather high difference of the load and drain currents in case of overshot, this difference is still less than 0.1% of the load current. Accordingly, it lies in an allowable range for restoring LDR steady state conditions. All of the introduced results confirm that our proposed methodology introduces an LDR of a quasi insensitive response to load current transitions in conjunction with keeping low power consumption. This is carried out on the merit of systematic transient approach as well as the ability of model parameters tolerating.

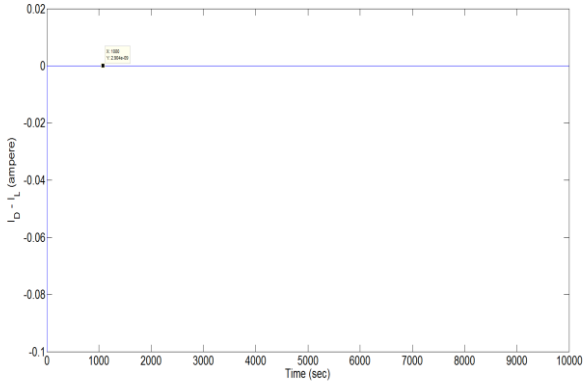

Fig.(8) Difference of the drain current and load current versus time in case of undershot

Finally, the simulation results can be summarized as Table II illustrates.

Table II: Maximum Values of Simulation Results

Item	overshot transient loading	undershot transient loading
maximum gate voltage variation during 10^4 sec	7 mV	170 mV
maximum output voltage variation during 10^4 sec	0.03 mV	0.52 mV
maximum gate current variation during 10^4 sec	0.25 nA	0.1 pA
maximum regulator current of output transistor during 10^4 sec	1 mA	2.9 nA

IV. CONCLUSION

Verification of the proposed methodology creates a mathematical frame of realizing circuits to treat transient loading of LDR considering the actual MOS transient model. This is realized along with the achieving of both static and small signal dynamic design requirements. Forming a load current initiated voltage stabilizer is represented by a set of nonlinear differential equations. It is demonstrated that the cross-coupling control between gate and drain voltages as well as currents achieves the regulation function with low power consumption. The optimization of the feedback stabilizing system proves that stabilization must be done under the constraint of switched biasing. Such biasing must be related to switched transient load current in order to satisfy the convenient initial conditions. Additionally, the modeling of the channel charge density in terms of a charge based model such as EKV gives the ability of nested functions to model equation parameters. That gives us the ability of developing the suggested approach. Moreover, under the existence of the small signal noise suppression techniques, the instability of the output voltage, with very slow variations, can be avoided by using these mechanisms of noise suppression.

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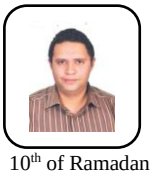
AUTHORS PROFILE



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