A Leakage Power Aware Transmission Gate Level Shifter

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Abstract: The clustered voltage scaling systems are ultimate power reduction techniques, uses voltage level shifters (LSs) to interface multi voltage domains to reduce power at system level. The LS may become overhead when its own power consumption and delay is high. In this paper we presented a new schematic of level shifter with single supply voltage to perform voltage level shift, which uses Transmission gate based circuit topology. The simulation results says it has energy per transition is 1.80E-14 J at 1 MHz frequency and the level shifter delay is 2.6 ns at VDDL 0.3V and VDDH 1V. The design has simulated by using 90nm CMOS technology files. This new architecture is more efficient then existing architectures.

Index Terms: Delay, Level Shifter, new architecture, Power consumption, Transmission gate.

I. INTRODUCTION

The uses of portable electronic devices like cellular phones, digital cameras, and pace makers are increasing rapidly day by day, and power consumption has to be reduced at system level to attain more user satisfaction. The ultimate solution is Multi VDD systems and System-on-Chip (SoC)s [1]. These are becoming more popular and common in many practical applications. Such a multi VDD and SoCs are needed to be operated with different supply voltages. For such compute theory, energy and power consumptions are crucial design elements. Both the power and Delay of a digital IC depends on its supply voltage.

Based on power consumption and delay constraint, it is common and recommended to decrease the supply voltage in the non-speed sensitive parts of multi-core processors and SoCs to decrease the power consumption. And speed sensitive parts of the multi-core processor and SoCs are operated with higher supply voltages to increase the speed performance [2], [3]. This leads to a situation there are number of parts/blocks in a SoC design need to be operated at different supply voltages, in order to reduce the power consumption at system level. Therefore, the efficient Level Shifters (LS) are need to be used to interface the different voltage domains to efficiently convert the given voltage level to desired voltage level [4].

Block diagram of conventional LS with multiple VDD cores have shown in Fig. 1. The interfacing module is LS which requires two supply voltages (VDDL, and VDDH). Where the VDDL and VDDH are the core voltages of core 1 and core 2 respectively. It is a tedious task to have a dual VDD wires at LS, particularly when the cores are separated with wider distances, leads to routing congestion at physical design, and resulting in Parasitic capacitance between wires and large area penalty, which is undesirable [5]. This routing congestion, parasitic capacitance, and area penalties are more aggressive when the voltage domains or cores are becoming more in SoC architectures.
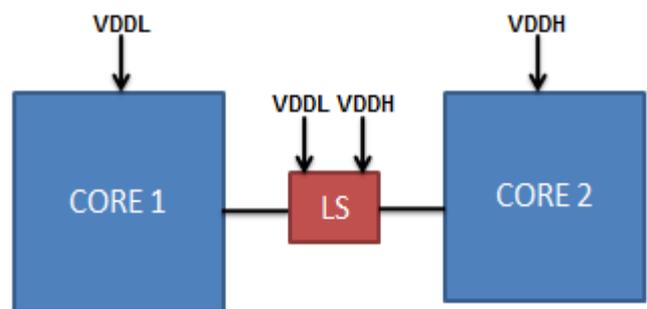

Fig. 1. Block diagram of Multi supply LS

Fig. 2. Shows block diagram of single supply Level shifter which uses the single supply voltage VDDH to perform level up shift. This kind of design is beneficial at routing congestion, parasitic capacitance, and area penalties. The main task in multi VDD systems and SoCs is the identification of efficient LS. In this paper we have introduced a new LS called Transmission gate Level Shifter (TGLS). This new LS architecture utilizes transmission gate circuit configuration to perform the level shifting action. The remaining part of the paper has described as follows. Chapter II describes about review on existing LSs. Chapter III deals with proposed design; Chapter IV is experimental results and comparison with other designs, and ends with conclusion chapter.
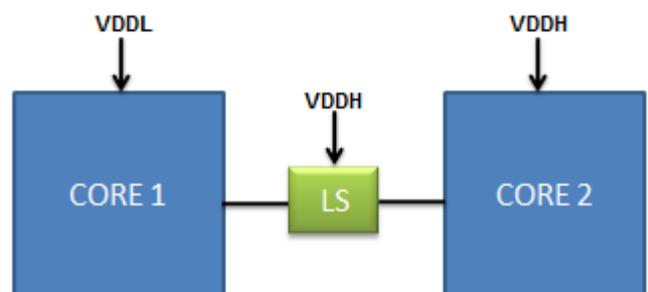

Fig. 2. Block diagram of Single supply LS

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Retrieval Number D6428048419/19©BEIESP
Journal Website: www.ijeat.org

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II. REVIEW ON EXISTING LEVEL SHIFTERS

The circuit shown in the Figure 3 is a cross coupled PMOS conventional LS useful to interface between two cores or voltage domains provided the input voltage (VIN) has to be above the threshold voltage (Vt) of NMOS transistors MN1 and MN2. This LS operation can be described as follows. When the VIN equals to VDDL, MN2 becomes turned ON and MN3 becomes off. Then, the node voltage at NH is pulls downs to the VSS by the low resistance path established by MN2, then MP3 becomes turned ON and pulls node NL HIGH. As NH pulls downs to VSS then MP4 becomes turned ON, then VOUT equals to VDDH. The faithful voltage shift results only if the pull-up to pull-down ratio is almost same. If the pull up to pull down ratio is not same then there will be increase in delay and power consumption [6], [10]. This is called contention problem, at least a small amount of contention problem will be in DCVS logic even optimized multi V_t devices are used in the design. To reduce the static power consumption the lower inverter has biased with VDDL. The design has utilizes to power supplies VDDH and VDDL, will results routing congestion in physical design.
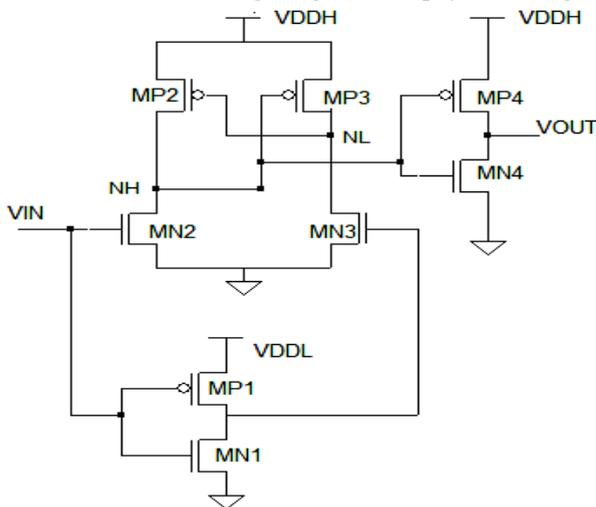

Fig. 3. PMOS cross coupled conventional LS

The LS proposed in [11] have used multiple power supplies to perform level shifting operation and estimated that a NMOS to PMOS ratio of approximately 2400 is needed to perform a full functional DCVS LS that converts 0.2V VIN to 1V VOUT.

The LS in [8] uses only two stages: the primary one make use of a DCVSL circuit with ON diode connected NMOS transistor at the top, whereas the secondary stage is a conventional DCVSL circuit for achieving full rail to rail swing. Being two stages DCVSL, contention problem may arises and design may lag in speed performance.

A WRLS using MWCM in [9] useful in wide range shifting application, and having a provision for bidirectional level shifting, balancing transition time delays, and it poses DCVSL kind of circuit topology utilizes dual power supplies. Being dual power supplies routing congestion may occurs at physical design.

III. PROPOSED TRANSMISSION GATE LEVEL SHIFTER

The proposed TGLS circuit design is shown in figure 4. This circuit design is quite simple and different from other LSs. All most all existing LSs are DCVSL based and biased with dual power supplies capable to perform level up shift.

This projected novel TGLS circuit utilizes only single power supply (VDDH) with 7 MOS transistors. The basic circuit element is the transmission gate; its ON resistance is very lower, typically lower than the ON resistance of NMOS. As resistance is very low better power and delay constraints can be met. The design has utilizes two transmission gates. The upper transmission gate MN2-MP2 is configured such that when VIN is equal to VDDL then VOUT is VDDH and lower transmission gate is configured such that when VIN is equal to VSS then VOUT is VSS. Never both transmission gates are simultaneously ON or OFF. In other words when upper gate is ON state then lower one will be in OFF state and vice versa.
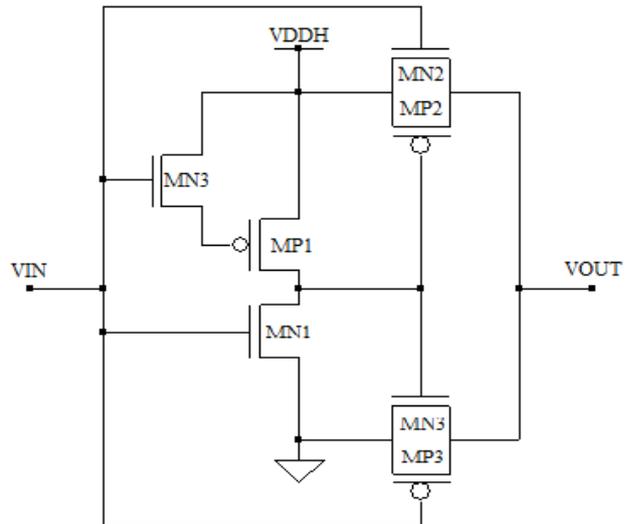

Fig. 4 Proposed Transmission gate Level Shifter

To analyze the circuit behavior VIN is taken 0.4V, which is equal to logic '1' input of the LS. And VDDH have taken 1V would be as logic '1' output at VOUT.

When VIN is 0.4V, the NMOS transistors MN1and MN3 becomes ON, as MN3 is ON the Gate voltage at MP1 is equals to VDDH then MP1 becomes OFF, the upper transmission gate MN2-MP2 becomes ON, as it is ON then VOUT node will be charged to strong VDDH, which is equal to 1V, Voltage Level up is the resultant.

When VIN is 0V, the NMOS transistors MN1and MN3 becomes OFF, as MN3 is OFF the Gate voltage at MP1 is very low, approximately equals to VSS then MP1 becomes ON, the lower transmission gate MN3-MP3 becomes ON, as it is ON then VOUT node will be discharged to strong VSS, which is equal to 0V.

IV. SIMULATION RESULTS AND COMPARISON

The novel TGLS circuit design has stimulated by Synopsis HSPICE with Predictive Technology Model (PTM) 90 nm technology model files. The Length of the MOS devices L = 90 nm, NMOS W=180nm, and PMOS W=360nm have taken. The robustness of the design is tested with a varying load capacitance from 10 fF to 90 fF, at temperature of 27 ^{0}C, and at the frequencies of 1 MHz, 500 KHz, and 100 KHz.

A. Functional simulation

The functional simulation of the proposed TGLS has shown in the figure 5. As a level-up shifting, the VDDL called VIN has kept at 0.3V and VDDH called VOUT kept at 1V, with load capacitance of 40 fF at a frequency 1MHz.
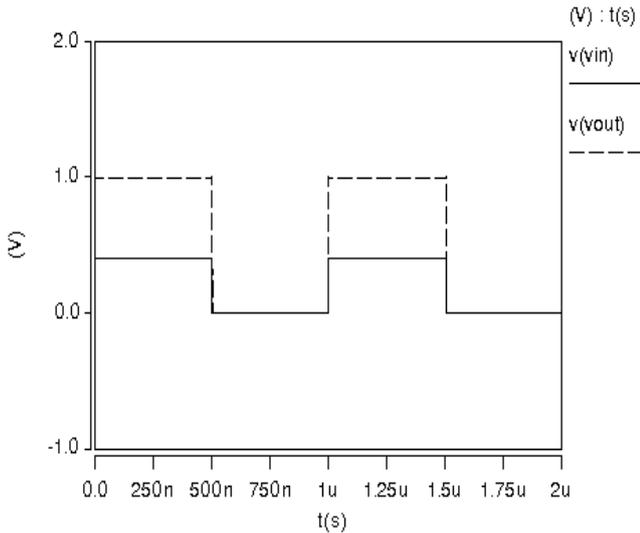

Fig. 5 Functional simulation.

B. Power analysis of the design

The average power analysis of the proposed TGLS circuit has shown in the fig. 6 and 7. The design behavior has examined at three different frequencies 1MHz, 500 KHz, and 100 MHz at a load capacitance 40fF. Fig. 6 depicts the behavior of the proposed LS at varying VIN between 0.275V to 0.475V with a constant VDDH 1V. Fig. 7 describes the behavior of the proposed LS at varying VDDH between 0.9V to 1.1V with a constant VIN 0.3V. The gate leakage is expected to be negligible.
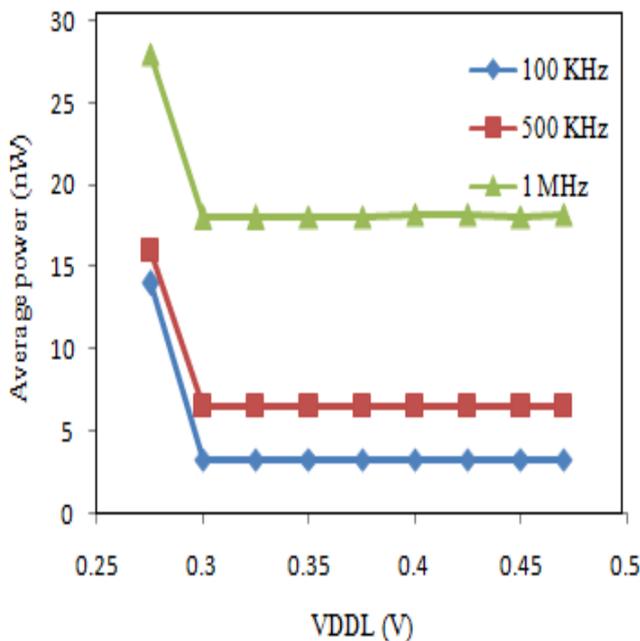

Fig. 6 Average power consumption of TGLS under varying VDDL, at a constant VDDH 1V and CL 40fF.
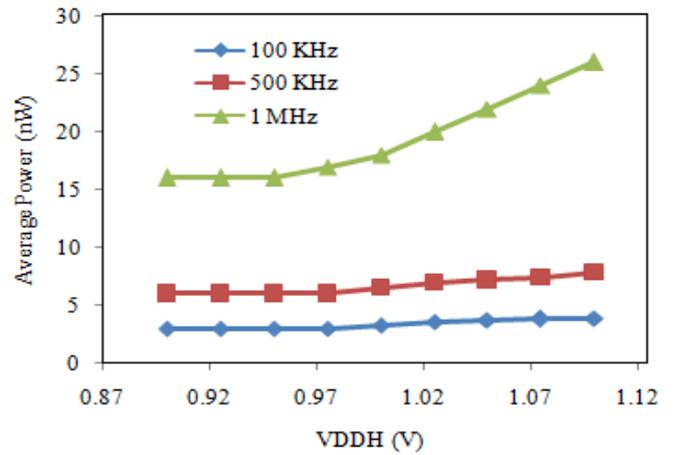

Fig. 7 Average power of TGLS under varying VDDH, at a constant VDDL 0.3V and CL 40fF.

C. Delay analysis

The Delay analysis of the TGLS circuit design has shown in the fig. 8 and 9. The delay behavior has examined at three different frequencies 1MHz, 500 KHz, and 100 MHz, with 1 ns rise and 1 ns fall times of the input signal, at a load capacitance 40fF. Fig. 8 depicts the Delay behavior of the proposed LS at varying VDDH from 0.9V to 1.1V with a constant VIN 0.3V. Fig. 9 describes the behavior of the proposed LS at varying VDDL from 0.275V to 0.475V with a constant VDDH 1V, the circuit incurs more delay when VIN less than 0.3V.
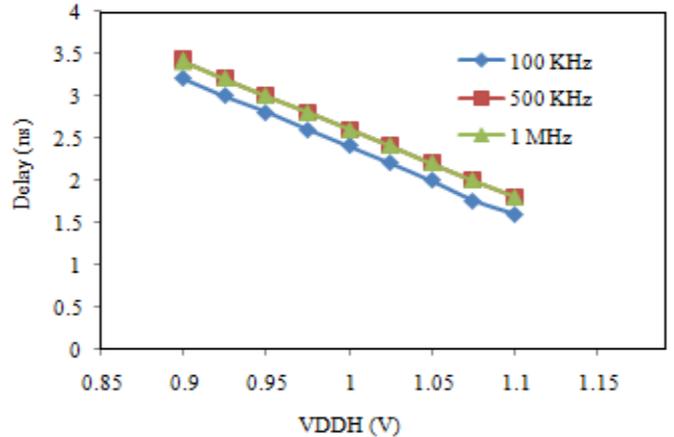

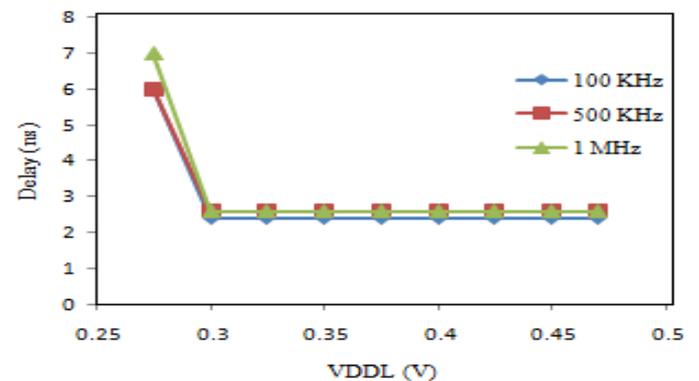**Fig. 8 Delay of TGLS under varying VDDH, at a constant VDDL 0.3V and CL 40fF**

Fig. 9 Delay of TGLS under varying VDDL, at a constant VDDH 1V and CL 40fF

D. Load Analysis

The Load analysis is useful to analyze the loading effects on the circuit design. The higher VDD core input impedance may show capacitive loading effect on the driving LS. The behavior of the proposed LS under varying load capacitance from 10 fF to 90 fF have described in the fig. 10 and 11. From the fig. 10 it is apparent that there is no much difference in the average power consumption under varying loads. It can be recommended that the proposed LS can be positioned in any segment of a target design as its power consumption is uniform and low at any given load capacitance. Fig. 11 describes Delay vs. Load capacitance, as load increase there is a slightly increases in Delay.
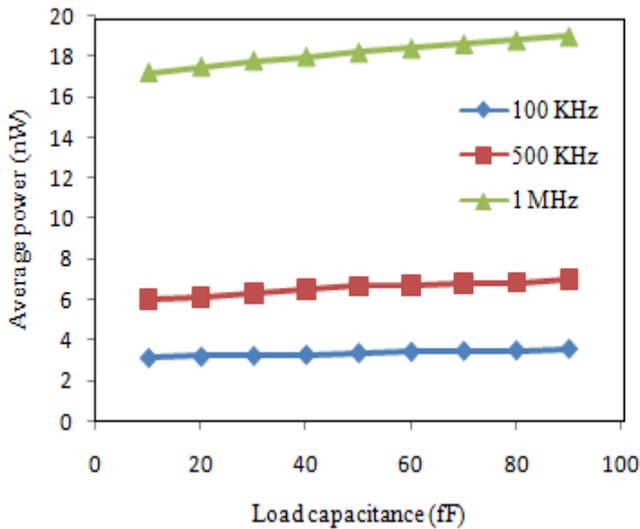

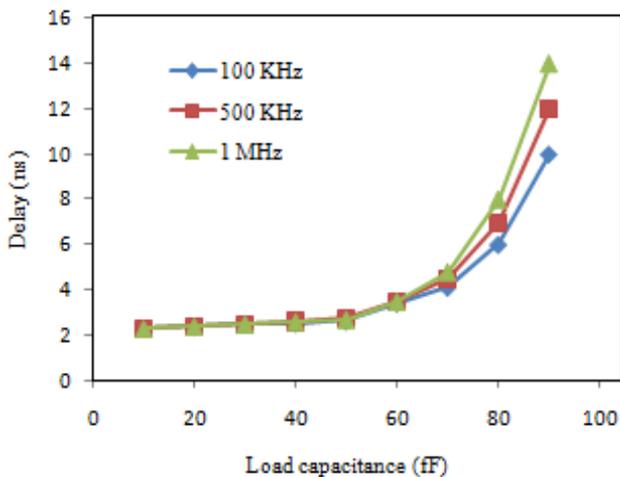**Fig. 10 Average power Vs. Load capacitance at VIN 0.3V, and VDDH 1V.**

Fig. 11 Delay vs. Load capacitance at VIN 0.3V, and VDDH 1V.

E. Comparative Analysis

The proposed TGLS can be comparable with other benchmark designs. The table 1 shows the characteristics of the various LSs. The proposed design is the dominating LS, it has active power consumption is 18 nW, the estimated energy per transition is 1.80E-14J, delay 2.6ns and the Power Delay Product (PDP) 0.05 fJ at 1 MHz frequency. The proposed LS outperforms compared with other existing LSs by considering all constraints of VLSI constraints.

Work/ Ref.	Type of	Frequency (Hz)	VDDL (V)	VDDH (V)	Active Power	PDP (fJ)
	shift				(nW)	
[7]	Up	1M	0.18	1	74	1.03
[8]	Up	1M	0.188	1.2	90	0.9
[9]	Up & Down	20K	0.4	1.2	----	---
[10]	Up	10K	0.4	3	150	1.5
[11]	Up	1M	0.2	1	93.6	1.72
Proposed	Up	1M	0.3	1	18	0.05

V. CONCLUSION

The designed and simulated transmission gate Level Shifter with 2 transmission gates with static power aware CMOS inverter to perform the voltage level shifting from 0.3V to 1V. Simulation results shows that proposed circuit is able to shift any voltage from 0.3V to 1V. The TGLS can be said as robust because, the design has no much difference in the active power consumption and Delay under varying loads between 10 fF to 90 fF, and its active power consumption is 20% of the other best benchmark designs [8]. Delay and PDP also the Best values compared with others designs. Delay at lower VDDL can be further improved by adopting lower threshold and Multi threshold devices.

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AUTHORS PROFILE

Srinivasulu Gundala have completed the Doctoral degree program in VLSI design from JNTUA, Anantapuramu, having 14 years of teaching experience, 15 research article publications in reputed journals, and member of ISTE, IETE .