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A Novel Design of Synchronous Counter for Low Power and High-Speed Applications

Kuruvilla John, Vinod Kumar R. S., Kumar S. S.

Abstract*: In this paper, a new power efficient and high-speed synchronous up-counter design suitable for low power and high-speed applications is proposed. The clock gating concept embedded in this design reduces unwanted switching activities at sleep/idle mode of operation and thereby reducing dynamic power consumption. The proposed design achieves better speed and power performance by successfully solving the longest discharging path problem and unwanted switching activities. This design can be used in many applications such as memory systems, microcontroller circuits, frequency dividers etc. The simulation results in Cadence Virtuoso based on CMOS 90-nm technology shows that the proposed design features less power dissipation, and better power delay performance (PDP) when compared with conventional designs. The proposed design is having the advantage of 33.50% in power and 30.66% in speed when compared with conventional design. The proposed counter is implemented in Xilinx Spartan-3 FPGA.

***Index Terms*: Clock gating, counter, low power, pulse flip-flop.**

I. INTRODUCTION

Flip-Flops are the widely used fundamental storage element in all types of digital structures. Synchronous counters are widely used in many applications such as memory systems, microcontroller circuits, frequency dividers etc [1]. Hence it is important to reduce the power consumption and delay involved in the operation of counter. It is also approximate that above 25% of the total system power is consumed by the clock system [2]. Thus, a major part of the area and power consumption of the total counter system is contributed by the flip-flops. In low power and high-speed applications, counter design based on Pulse flip-flop (P-FF) exhibits better performance than conventional master-slave FF designs. The single latch structure design of P-FFs made them more popular than conservative master-slave and transmission gate-based FF designs in low power and high-speed applications [3].

Pulse generator and latches are the two basic parts in the structure of a P-FF design. The trigger pulses are generated by the pulse generator at any edges of clock signals or at both edges of clock signals. The latch structure performs the latching or sampling of the input data into the output based on the generation trigger pulses. Depending upon the triggering pulse generation mechanism, P-FFs are classified as a single and double edge triggered types [4].

Based on the connection of pulse generation logic and latch, P-FFs are classified as implicit and explicit types [5-6]. In implicit case, the pulse generator is inbuilt in the latch structure and in explicit it is external to the latch structure. It is estimated that power efficiency is more for implicit P-FFs than explicit types. It is due to the fact that control of discharging the path takes place in implicit P-FF but in the explicit P-FF physical generation of the pulses needed. However, explicit P-FF has an advantage of sharing of pulse generator among neighboring latches. Both implicit and explicit P-FFs face the longest discharging path problem in latch structure. This increases the size of the transistors used at the pulse generator to enlarge the width and height of triggering pulses for the sufficient capturing of data.

A lot of wastage in power consumption takes place due to the unnecessary switching activity in a P-FF. Using various technologies such as conditional discharging [7], conditional data mapping [8], conditional capturing [9], and clock gating [10-11], unwanted switching activities can be avoided and thus the power consumption can be reduced [12].

In this paper, a low power and high-speed synchronous counter using implicit P-FF is presented. This structure solves the unwanted switching activities at sleep/idle mode of operation and the longest discharging path problem in the latch. The remaining part of the paper is organized as follows: Section II describes counter design using conventional P-FF. Section III describes proposed counter design. Section IV compares the counters and presents the results after simulation. The paper concluded in section V.

II. CONVENTIONAL COUNTER DESIGN

A 3-bit synchronous up counter embedded with conditional pulse enhancement (CPE) [13] scheme and signal feed-through (SFT) [14] mechanism is explained in this section. In CPESFT flip-flop based counter, the enhancement in width and height of triggering pulse when output changes from LOW to HIGH value and the direct coupling of input to output are the key features [15]. Fig.1 shows the circuit diagram of CPESFT flip-flop. In CPESFTFF the LOW to HIGH transitions of input data causes the discharging of the internal node X through the nMOS transistors N4, N5, and N1. This is the longest discharging path at latch structure.

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* Correspondence Author (s)
Kuruvilla John*, Research Scholar, Department of Electronics and Communication, Noorul Islam Centre for Higher Education, Thucklay, India, and Assistant Professor, Department of Electronics and Communication, Providence College of Engineering, Chengannur, India.
Vinod Kumar R. S., Professor, Department of Electronics and Communication, Noorul Islam Centre for Higher Education, Thucklay, India.
Kumar S. S., Associate Professor, Department of Electronics and Instrumentation, Noorul Islam Centre for Higher Education, Thucklay, India.

During normal conditions other than longest discharging path occurs, then node Z value produced by N type PTL AND gate is VDD-Vtn. The longest discharging path is formed when both input data and output are HIGH. When longest discharging path occurs, then transistor P3 is used to increase the speed of discharging. Transistor P3 is in the turned OFF state until node X is pulled down to LOW value. Turning ON of transistor P3 takes place when node X is discharged to Vtp (threshold voltage required to turn ON pMOS transistor) below the VDD. The turning ON of transistor P3 provides additional boost to triggering pulse at node Z from VDD-Vtn to VDD. This boosted pulse reaches the gate of transistor N6 and enhance the speed of operation.

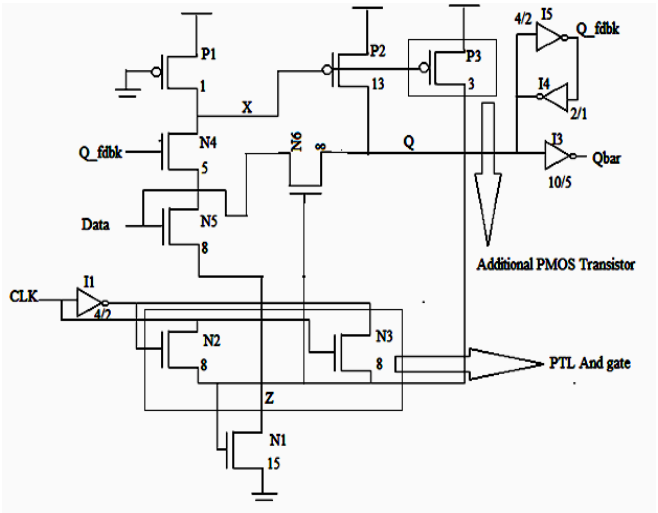

Fig.1. Circuit diagram of CPESFTFF [15]

The shutdown of discharging path takes place after the rising edge of the clock signals. During this time the delay of inverter I1 drives PTL AND gate output at node Z back to zero and closing of discharging path takes place. The node X voltage values increases above Vtp and turns OFF pMOS transistor P3. Thus, the embedded features like conditional enhancement in width and height of triggering pulses by using an additional pMOS transistor and a pulse-triggered structure with a modified signal feed-through mechanism which directly samples the input to output by using an nMOS pass transistor increases the speed and power performance of proposed design when compared with conventional implicit and explicit P-FFs. In the CPESFTFF based counter, unwanted switching activities take place on sleep/idle mode of operation because of the active operation of the clock at this mode. This will increase the total power consumption and thus degrades the performance.

III. PROPOSED COUNTER DESIGN

In this section a new design for 3-bit synchronous up counter is proposed. This counter design is embedded with clock gating concept which reduces the unwanted switching activities at sleep/idle mode of operation, thereby reducing the power consumption. Clock gating concept is specially designed for low power applications [16]. This concept solves unwanted switching activities at sleep/idle mode of operation with an additional NOR gate. In this technique, there is a separation in the power exerted by the clock circuit and a remaining circuit. The power consumption of both the clock and remaining circuit in sleep/idle mode can be reduced by disabling the clock circuit. The proposed clock gating technique can be implemented by disabling the inverter gates present in the pulse generation logic of the conventional P-FF. This can be achieved by replacing the inverter I1 present in CPESFTFF with a NOR gate as shown in Fig.2.

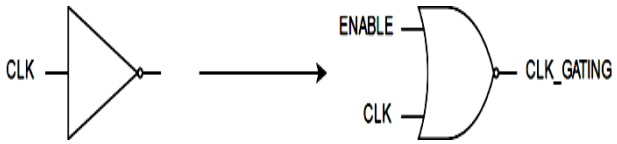

Fig.2. Clock gating concept

The circuit diagram of proposed counter is shown in Fig.3. This design is embedded with three important features. The unwanted switching activities in the sleep/idle mode of operations can be overcome by using clock gating concept. The speed of the discharging path can be improved by the conditional enhancement in width and height of triggering pulses. The speed of latching of input data into the output can be increased by signal feed-through concept. The embedding of these three features makes the proposed counter, more speed and power efficient.

This counter design requires three flip-flops and some logic gates. The expression for the inputs to each flip-flop is represented as in (1), (2) and (3) [17].

$$D0 = Q0' \quad (1)$$

$$D1 = Q1'Q0 + Q1\,Q0' \quad (2)$$

$$\text{and } D2 = Q2'Q1Q0 + Q2Q1' + Q2\,Q0' \quad (3)$$

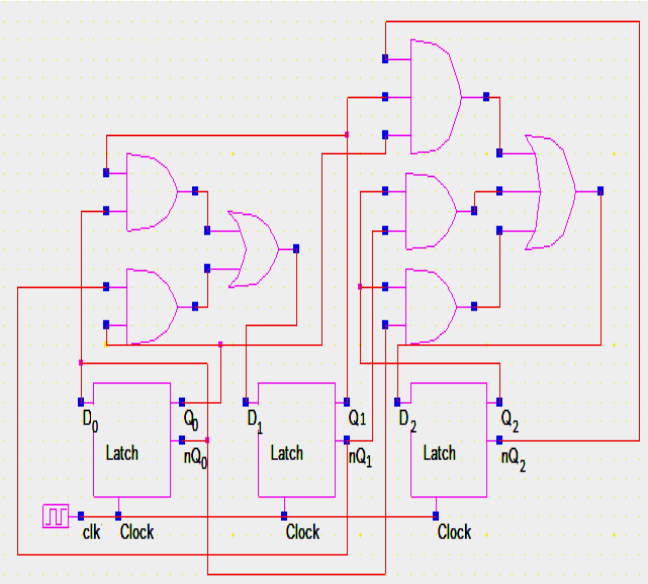

Fig.3. Circuit diagram of Proposed Counter

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IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed and conventional counters are simulated in CMOS 90nm technology. The operating condition used in simulation is 500 MHz/1.5V and temperature of 298K. Cadence virtuoso software is the simulation tool used to implement the various counter designs. Fig.4 shows the simulation setup model and Fig.5 represents the waveform of proposed counter. From the simulation waveform it is clear that counting takes place in the correct sequence.

Due to the embedding of clock gating concept, the proposed counter reduces the average power consumption to 131.84µW. The power waveform of proposed counter is shown in Fig.6. Thus the introduction of the clock gating concept in CPESFTFF based counter make an advantage of 27.94% in power consumption. The functional verification of proposed counter is done by using Xilinx Spartan-3 FPGA. The implementation of proposed counter in FPGA is shown in Fig.7.

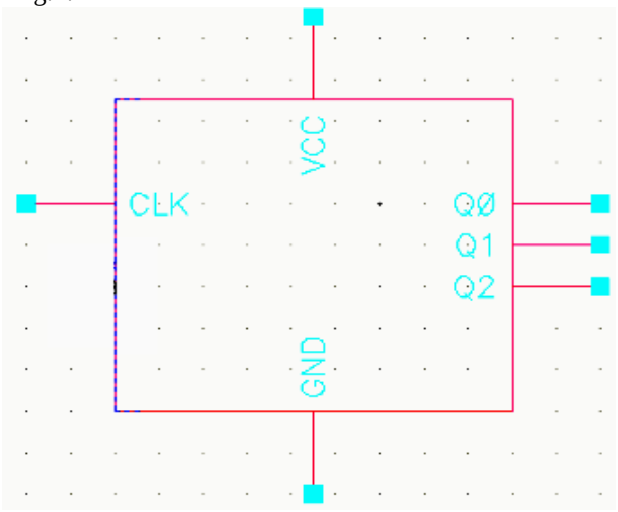

Fig.4. Simulation setup model of Proposed Counter

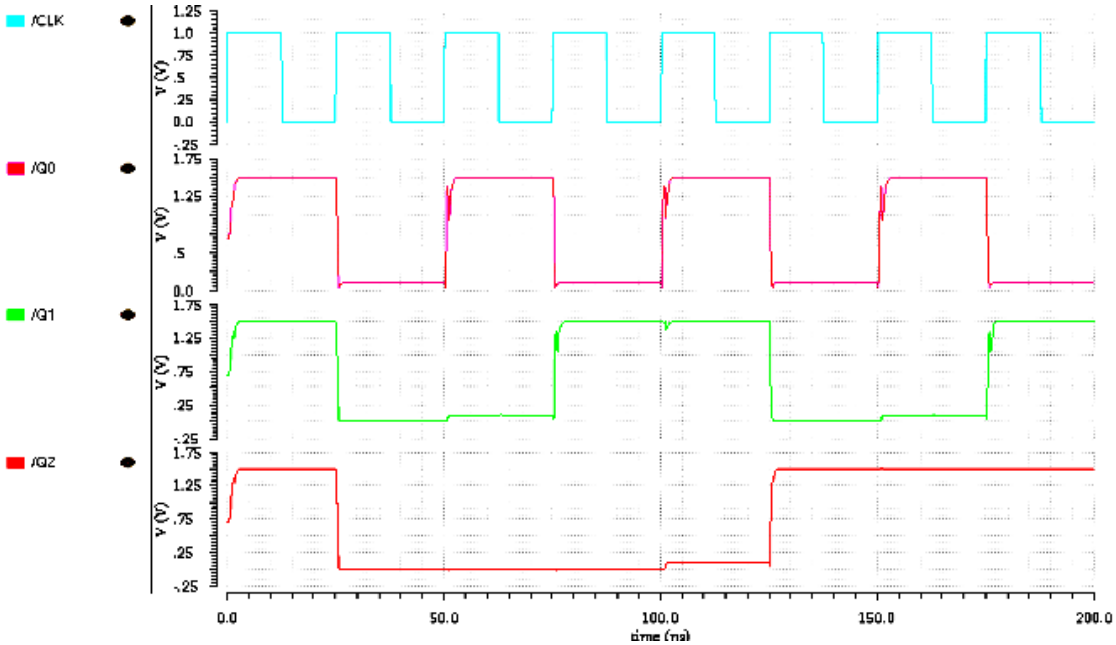

Fig.5. Simulation waveform of proposed counter

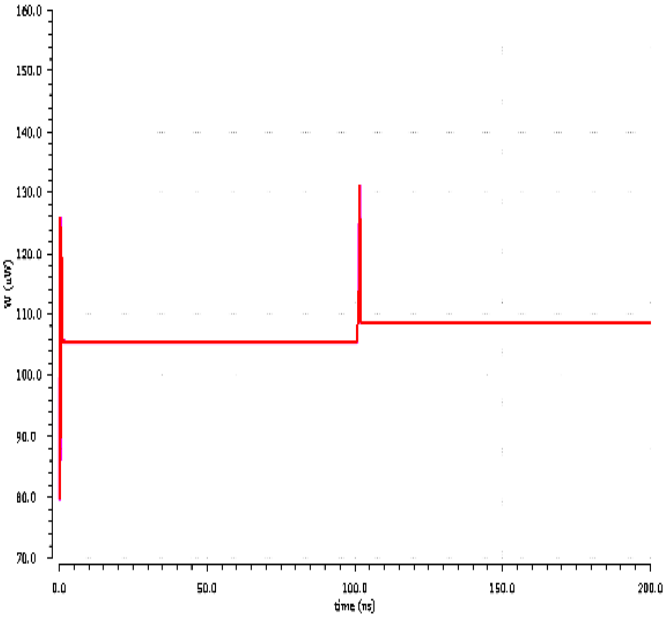

Fig.6. Power waveform of proposed counter

A. Performance Comparison of Counters

To assess the performance of the proposed counter, simulation of other designs is done under similar conditions. Table I shows the comparison of various performance parameters of proposed counter with other conventional designs. It includes transistor count, average power consumption, minimum CLK to Q delay, and power-delay product performance. The simulation result shows that due to the embedding of conditional pulse enhancement technique, clock gating concept and signal feed-through mechanism, the proposed counter have better performance in power, and power-delay product than conservative counters.

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Fig.7. Implementation of proposed counter in FPGA

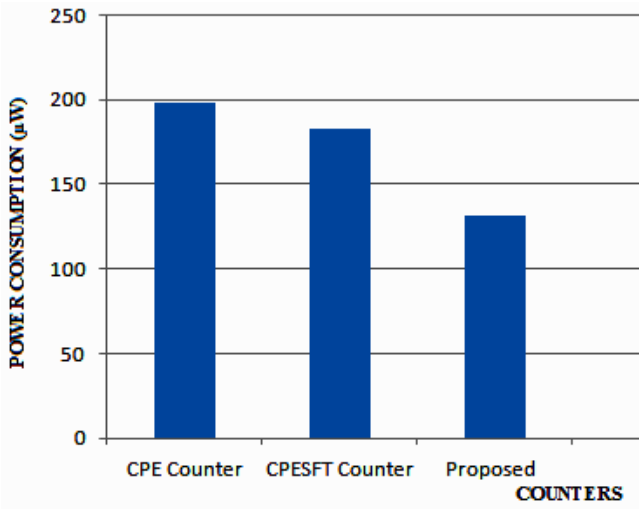

Fig.8. Comparison of Power Consumption in Counters

Table I. Observation of Design Parameters

P-FFs	CPEFF based Counter	CPESFTFF based Counter	Proposed Counter
Number of Transistors	103	97	103
Power Consumption (μW)	198.28	182.98	131.84
CLK-to-Q Delay (pS)	478.49	299.81	331.76
Power-Delay Product (fJ)	94.87	54.85	43.73

Fig.8 shows the power comparison of proposed counter with CPEFF based counter and CPESFTFF based counter. The power consumption of the proposed design outperforms the conventional CPEFF based counter by a margin of 33.50%. The proposed design is having the advantage of 27.94% in power consumption when compared with conventional implicit CPESFTFF based counter. The proposed counter is having 30.66% of advantage in CLK to output Q delay when compared with CPEFF based counter. Among the compared counter design, the proposed counter is having the best power-delay product performance due to its reduced power consumption and increased speed of operation. Fig.9 shows power-delay-product comparison among the three counter designs.

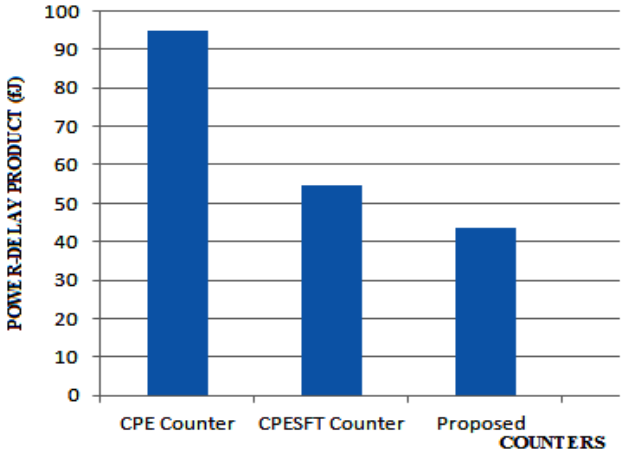

Fig.9. Comparison of Power Consumption in Counter

V. CONCLUSIONS

In this paper, a novel low power and high-speed synchronous 3-bit up counter is presented. The two features conditional enhancement in trigger pulse and signal feed-through mechanism reduces the longest discharging path problem and increases the speed of operation by direct coupling of input to output. The clock gating concept reduces the dynamic power consumption. Cadence simulation results indicate that the proposed counter design is having the best performance in power and power-delay product (PDP).

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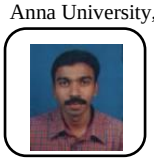
AUTHORS PROFILE

Mr. Kuruvilla John received his B.Tech and M.Tech degrees in Electronics and Communication Engineering from the Mahatma Gandhi University, Kerala, India, in 2010 and 2014 respectively. He is currently doing his research in Low Power VLSI from Noorul Islam Centre for Higher Education, Tamilnadu, India. He is an Assistant Professor of the Department of Electronics and Communication Engineering, Providence College of Engineering, APJ Abdul Kalam Technological University, Kerala, India. He has more than 5 years of teaching experience, and many publications in journals and conferences. His research interest includes Low Power VLSI, VLSI Signal Processing, and Digital Design Principles.

Dr. Vinod Kumar R. S. received his B.E. degree in Electronics and Communication Engineering in 1991 and M.E. degree in Communication Systems in 2000, both from Madurai Kamaraj University, Tamil Nadu, India. He pursued his Ph.D degree from Anna University, Chennai, India, in 2015. His areas of research are VLSI Design, Multiresolution Patch-based Texture Synthesis, Steganography, and Medical Imaging. He has contributed 30 technical papers in various journals, and International/National Conferences. He started his career as Lecturer in Noorul Islam College of Engineering, Tamil Nadu, India in 1993 and presently working as Professor & Head, Department of Electronics & Communication Engineering and Dean, Faculty of Electrical & Electronics Engineering, Noorul Islam Centre for Higher Education, Kumaracoil. He has more than 25 years of teaching experience and thirteen years of research experience. His areas of interest include VLSI, Digital Image Processing, Analog Modulation Systems, Digital Communications, Linear Integrated Circuits and Digital Electronics. At present he is guiding 8 Ph.D scholars. He is a Doctoral Committee member for twelve Ph.D Part-time/Full-time scholars, in the faculty of Information and Communication Engineering, Anna University, Chennai.



Dr. Kumar S. S. received his B.E. degree in Electronics and Instrumentation Engineering from Manonmaniam Sundaranar University, Tirunelveli, India and M.E. degree in Applied Electronics from Anna University, Chennai, India. He pursued his Ph.D degree from Anna University, Chennai, India. His areas of research are VLSI, Medical Image Processing, Satellite Image Processing, Multiresolution Techniques and Artificial Intelligence. He has published several technical papers in various journals, and conferences. He started his career as Lecturer in Noorul Islam College of Engineering, Tamil Nadu, India in 2005 and presently working as Head, Department of Electronics & Instrumentation Engineering, Noorul Islam Centre for Higher Education, Kumaracoil. He has more than fourteen years of teaching experience and ten years of research experience. He has produced three Ph.D scholars and at present he is guiding 6 Ph.D scholars. He is a Doctoral Committee member for ten Ph.D Part-time/Full-time scholars, in the faculty of Information and Communication Engineering, Anna University, Chennai.

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