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Hybrid Variable Latency Carry Skip Adder in Multiplier Structures

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Abstract: ***One of the chief successful adder structures is the Carry Skip Adder (CSKA). This is mainly due to its power scattering and lesser area. Truth be told, when compared with the Ripple carry adder (RCA) its speed is higher. The Carry Select Adder (CSLA) is described by a decent productivity in the exchange off between power dissemination and speed when compared to Carry Lookahead Adder (CLA). Area utilization and power utilization of CSKA is almost proportional to RCA, the only difference is the carry propagation delay in RCA. Certain speed limitation in CSKA makes it not useful for high speed applications. Distinctive methodologies are used for the conventional CSKA to make it more efficient in its performance. The proposed CSKA comprises of reversible carry skip logic with incrementation scheme produces less delay and low power consumption. Further when this proposed logic is used in multiplier area, delay and power decreases by 15.87%, 17.63% and 22.68% for Baugh-Wooley multiplier and 16.8%, 42% and 15.01% for Wallace multiplier respectively.***

Keywords: Carry Skip Adder (CSKA), Ripple carry adder (RCA), Skip logic, Concatenation Incrementation, Baugh-Wooley multiplier, Wallace multiplier.

I. INTRODUCTION

In normal microprocessor or digital signal processor, the core of the data path consists of arithmetic operations like addition, subtraction, multiplication and division. In the normal data path operations, addition plays a key role in executing the operation. So, for the quick computation of the addition, adders play an important role. So, designing the efficient adders is in the front line. Further due to the advancement in the technology, several parameters like wire length, number of fan outs are also taken into account. An eye should be kept on designing the adder with minimum area and delay [1] which has a vital and direct impact on the performance of the circuits. Addition is a key task for any computerized framework. A quick and precise task of an advanced framework is incredibly impacted by the execution of the inhabitant adders. Adders are likewise imperative part in advanced Frameworks due to their broad use in other fundamental computerized tasks, for example, subtraction, multiplication and division.

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II. CARRY SKIP ADDER

The conventional CSKA [2] structure comprises of phases of RCA blocks and 2:1 multiplexer and all the RCA blocks are associated with one another via 2:1 multiplexers. The structure of a N-bit customary CSKA, which is constructed generally in light of blocks of the RCA, is appeared in Figure 1.Not withstanding the chain of full adders in each organize, there is carry skip logic. For a RCA that has N cascaded Full Adders, the greatest combinational path delay is the aggregate of two N-bit numbers, An and Bn.

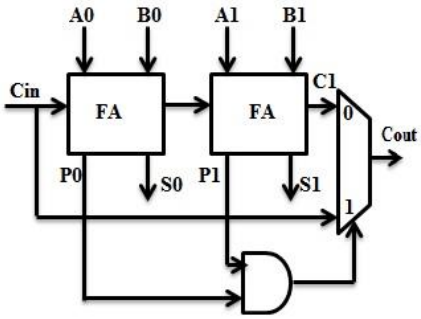

Fig 1: Schematic of 2 bit Carry Skip Adder

A. Concatenation-Incrementation CSKA

The structure depends on applying the connection and incrementation systems to the Traditional CSKA structure and in this way, is known as Concatenation-Incrementation (CI-CSKA), is appeared in Figure 4.2. It gives us with the capacity to utilize considerably more straightforward skip logic. The skip logic replaces 2:1 multiplexers by AND-OR-Invert or potentially AND-Invert complex gates. When compared with the conventional CSKA structure CI-CSKA has lesser area and higher speed. The CI-CSKA has two information sources (An and Bn) and Q stages. Each single stage comprises of a Ripple Carry adder with the measure of Mj. For this adder arrangement, the carry contribution of all the Ripple Carry Adder unit, with the exception of the underlying block which is Ci is zero. Along these lines, every one of the blocks executes their employments in the meantime. In this structure, when the underlying block processes the whole of its input bits, alternate blocks likewise register their moderate outcomes, and carry out (Cj) signals at the same time. In the CI-CSKA structure, the initial stage has a just single block, which is Ripple Carry Adder.

The remaining stages comprise of both the RCA block and incrementation scheme. The halfway outcomes delivered by the Ripple Carry Adder block and the carry output of the prior stage is used by the incrementation scheme to give the extreme sum of the stage.As a rule full Adder function can present either utilizing Boolean logic work traditional engineering or the dominant part work. Subsequently it is seen that the carry complement is generated at even stages of the skip logic output.

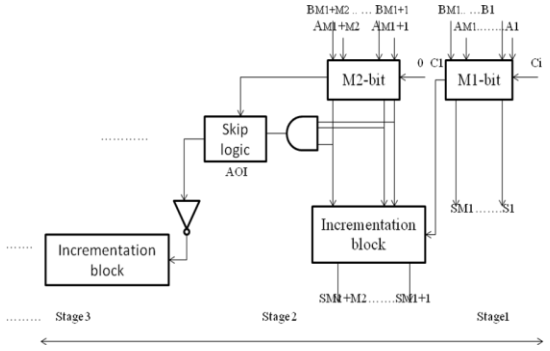

Fig 2: Schematic of Concatenation-Incrementation scheme

Even though there is a slight increase in area, the propagation delay is somewhat lesser when compared to the conventional CSLA. Here the multiplexer is replaced by AOI or OAI complex gates. These complex gates have low power utilization when compared to the multiplexer. Thus the power utilization of the proposed CI CSKA is somewhat less than that of the regular one. In this technique the first column starting from the right has one block of RCA followed by two blocks of RCA and incrementation scheme starting from the stages two to Q. The second stage is followed by the skip logic. The strategies anyway cause area and power increment impressively and less consistent design.

B. Incrementation Scheme

The incrementation block uses the halfway outcomes created by the RCA block and the carry output of the past stage to figure the final summation of the stage. The inner structure of the incrementation block which contains a chain of half-adders (HAs) is appeared in Figure 3.

Furthermore, take note of that to diminish the delay impressively, it is seen that to process the output carry, the output carry of the incrementation scheme is not utilized. The output carry is decided by the skip logic. The skip logic decides the output carry based on the j^{th} level denoted by (Co,j) which is mainly based on the past stage(Co,j-1) of the intermediate consequences of j^{th} arrange and output carry. This also depend on the output carry of the comparing RCA block (Cj) At the point when Cj is equivalent to one Co,j will be one.

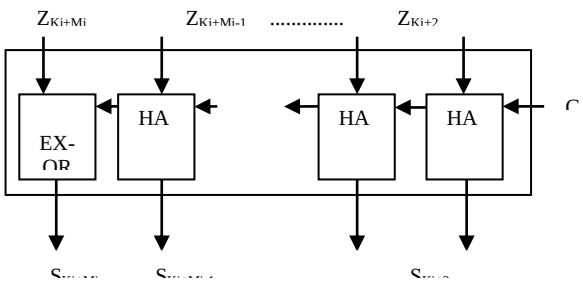

Fig 3: Block diagram of Incrementation Scheme

C. Skip Logic

AND-OR-INVERT (AOI) Logic Gates

AND-OR-Invert (AOI) logic are the two-level rationale capacities built from the mix of at least one AND gate taken after by a NOR gate. AOI and OAI gates can be promptly executed in CMOS hardware.

AOI gates are especially advantaged in that the aggregate number of transistors or gates is less if the AND, NOT, and additionally gates were executed independently. These outcomes in expanded speed, decreased power, littler area, and conceivably bring down manufacture cost. For instance a 2 to 1 AOI gate can be built with 6 transistors in CMOS contrasted with 10 transistors utilizing a 2 input NAND gate (4 transistors), an inverter (2 transistors) and a 2 input NOR gate (4 transistors).

OR-AND-INVERT (OAI) Logic Gates

The complement of AOI Logic is OAI logic where the OR gate go before a NAND gate. The purpose behind utilizing the two different logic complex gates is that they act like the complementing elements in the standard cell libraries. Further the inverter gates consumes low power utilization and the delay is also disposed of. When one of the skip logic uses AOI gates then the following Skip logic should be replaced by OAI gates. Thus alternate complex gates should represent the structure. When these skip logic scheme is introduced in the conventional CSKA, it may leads to the increase in the delay of the conventional scheme. This is mainly due to the skip logic complex gates can't sidestep the zero carry contribution until the point when the zero carry input engenders from the relating RCA block. To take care of this issue in the proposed structure it has utilized a RCA block with a carry contribution of zero utilizing the link approach. Along these lines it is noted that the RCA block need not to wait for the past stage carry output and the carry output of the blocks are ascertained in parallel.

The main aim of utilizing the skip logic is the number of transistors. The number of transistors when using the OAI or AOI skip logic complex gates is only six when compared to the Conventional method of using CSKA having the 2:1 multiplexer which has 12 transistors. The increase in the number of transistors leads to the increase in the area consumption which may further increase the power and delay of the circuit. Since the first stage in the proposed method has only one block of RCA having the input carry as zero, this is replaced by the half adder. As a result in the total configuration, the number of full adders has been reduced by one which may further decrease the area. It should be noted that the incrementation scheme does not present in the traditional CSKA.

The function of the skip logic is similar to the multiplexer used in the conventional one. The only change is the proposed skip logic utilizes XOR and AND gates for its operation. This is mainly to reduce the area consumption of the circuit design. Thus as a whole the proposed CI-CSKA consists of three arranges starting from the first stage of one block of RCA followed by two blocks of RCA, skip logic and final stage by the incrementation scheme.

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III. HYBRID VARIABLE LATENCY CSKA

A. Adaptive Clock Stretching VL CSKA

The main aim of utilizing the Variable latency adder [3],[4] is that the adder's critical path is actuated once in a while.

Subsequently the supply voltage might be downsized without diminishing the clock recurrence. If the critical path is not initiated, it is enough that a single clock period is used for finishing the activity. But on the other hand when the critical path is initiated, two clock periods are required to finish the task. So there arises a slack between the longest critical path and longest off critical path in this structure of adaptive clock stretching Variable Latency (VL) CSKA. Further for deciding the critical path initiation in VL adders, the predictor block is used. Based on the design of data sources the predictor block works. So this is one of the disadvantage of using the Adaptive Clock stretching VL adders.

The basic idea behind the supply voltage scaling and clock extending in the N bit ripple carry adder can be clarified. For the desired bit positions, the product of the propagate signals is decided by the predictor blocks. The predictor block consists of XOR and AND gates. Though there is some area and power constraints for this block just couple of center bits is utilized to foresee the initiation of the critical paths at cost of expectation exactness diminish. It is abused to foresee the propagation of the j^{th} arrange output carry to the j+m output carry. This leads to the concept of longest latency path (LLP). LLP is defined as in the longest critical path, the propagation way to the final N stage from the initial stage.

The Shortest latency Path is represented by SLP and is called as the longest off critical path. The carry propagation way to the j+m arrange from the first or initial stage is called as Short Latency Path one (SLP1) and the carry propagation way to the final N stage from the j+1 arrange called Short Latency Path two (SLP2).For the desired given sets of inputs given by the predictor block some paths are not active and are called as the critical off paths. The critical off path is set to minimum by having the bits in the center abatements. The slack time is determined by the voltage scaling range [5], [6]. The slack time is defined as the difference between the delay time of longest latency path delay and the maximum of SLP1 and SLP2.

B. Proposed Hybrid VL Structure

The fundamental thought of using the variable stage size adder is that the delay of the critical path is low when compared with the fixed stage size adder of carry skip scheme. So there is no need of using the slack time for scaling of the supply voltage. In order to incorporate the variable latency scheme certain stages at the middle are replaced by the parallel prefix adder (PPA). This forms our new proposed Hybrid VL adder. In the proposed structure the p^{th} arrange core structure is the Mp bit altered PPA. Further core arrange is of largest size and delay due to SLP1 and SLP2 are overcome by replacing with PPA. The longest delay has been reduced by the introduction of PPA.

The utilization of the quick PPA enables expanding the accessible slack time in the variable latency [7] structure. It ought to be said that since the information bits of the PPA blocks are utilized in the predictor block, this block moves toward becoming parts of both SLP1 and SLP2. The proposed methodology considers the fast-parallel prefix Brent Kung adder [8], [9] as the prefix system. This Parallel Prefix Brent kung adder is used for building the core and is used as the core arrange. The main advantage of using this Brent Kung adder is that it uses both forward and backward paths. Forward path is used for calculating the longest carry and the backward path is used for calculating the intermediate carries. Other advantages of this adder are the wire length and number of fan-out. They are less when compared to the other Parallel Prefix adders. At long last it has a straightforward and normal design.

The carry propagate and the carry generate for the input data sources are computed at the preprocessing level. The number of bits used for the calculation is assumed to 8(Mp=8). The following level has the Brent Kung as the prefix network and the longest carry (G8:1) based on the generate of the prefix network and product of the propagate of all the input signals (P8:1) is calculated. The Block diagram of Proposed Hybrid Variable Latency CSKA structure is shown in the figure 4.

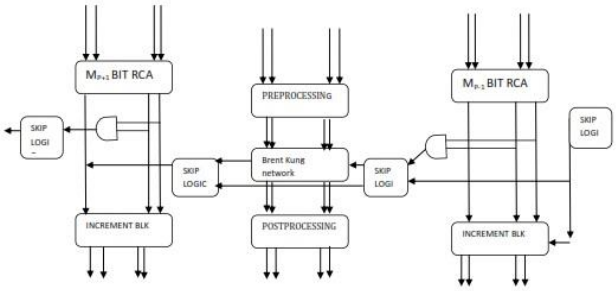

Fig 4 Block diagram of Proposed Hybrid Variable Latency CSKA structure

To skip or retain the output carry of the past stage is decided by the skip logic based on the propagate signal (P8:1).The output carry of the past stage is represented by Co,P-1.In the normal VL adder this propagate signal is abused as the predictor signal. Note that all these operations are performed simultaneously in a parallel manner. When ((P8:1) =1) the output carry (Co, P-1) of the past stage is skipped assuming one of the critical path is activated. On the other hand when ((P8:1) =0) Co, P is equals to G8:1 and there is no activation of the critical path. Later based on the parallel prefix network, the output carry of the past stages Co, P-1 which are the functions of the intermediate signals are calculated. The final sum is calculated at the final post processing stage.

It ought to be noticed that the final part of short latency path 1 (SPL1) from the output carry of the past stage (Co, P-1) to the end final results of the parallel prefix adder block and starting piece of the short latency path2(SLP2) from the input of this block to the output carry (Co, P) where all depends on PPA blocks. It should be noted that the first input for the starting stage is the starting point of SPL1and the final point of SPL2 is the final piece of the aggregate output of the stage Q incrementation block.

Since the PPA structure is more proficient when its size is equivalent to the power of two it can choose a bigger size for the core arrange appropriately. So a modification can be done at the third stage.

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Because of the large size of the core arrange, the number of bits and the size of the bits used for the core arrange can be increased. This may in-turn decrease the number of stages and delay in the circuit design (SLP1&SLP2). The maximum off critical path has been reduced by having the bits in the center and further the voltage scaling range can be also controlled.

C. Proposed Hybrid VL Reversible Structure

In this Proposed reversible structure, the RCA block have been replaced by reversible RCA block comprising of Reversible full adders. The reversible full adder is constructed using reversible gate called Peres gate. The combination of two reversible Peres will leads to the reversible full adder. The combination of reversible full adder will leads to ripple carry adder. Similarly the incrementation block is constructed using half adder and EXOR gates. These gates are also replaced by reversible gates. Further OR, AND and NOT gates are also replaced by reversible gates for the implementation of AOI and OAI Skip logic. The parallel prefix adder which is used as the core arrange is replaced by reversible Brent Kung adder. The reversible Brent Kung adder comprises of Post Generate (PG) block made of Peres gate, Grey cell made of two Peres gate and Black cell made of Grey cell and one Peres gate. The results prove that the delay is further reduced by using this proposed method of Hybrid Variable Latency Reversible CSKA Structure. The overall schematic of Proposed Hybrid Variable Latency Reversible CSKA Structure using Reversible Brent Kung as core structure is shown in the Figure 5.

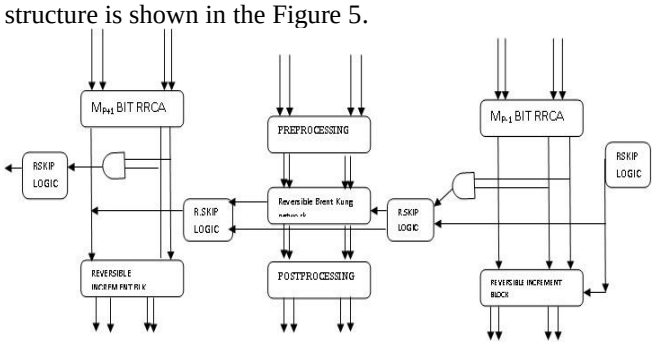

Fig 5: Proposed Hybrid Variable Latency Reversible CSKA Structure using Reversible Brent Kung as core structure

Table 1 describes about the different types of adder delays for both 16 and 32 bit. It is seen that the proposed carry skip adder with Brent kung adder as core arrange has the minimum delay and it is validated by Xilinx ISE Design Suite 14.5 tool for Spartan 3E family, the XC3S500E device with a speed grade of -7.

Table 1 Performance of different types of adder of 16 and 32 bit width

ADDERS	16 Bit width Delay(nS)	32 Bit width Delay(nS)
RCA	27.331	38.548
Conv.CSKA	24.667	34.913
FSS-CI-CSKA	23.882	29.408
VSS-CI-CSKA	22.456	28.773
Han Carlson Adder	19.187	27.563
Sklansky Adder	19.751	28.112
Ladner Fischer Adder	20.832	28.972
Brent Kung Adder	18.651	26.429
Han Carlson as core arrange	17.671	25.212
Brent Kung as core arrange	16.932	23.603
Reversible Brent Kung as core arrange	15.453	22.194

IV. BAUGH-WOOLEY MULTIPLER

The time taken for the generation of the partial products and the total number of partial products generated in the signed multiplication is high. So a new algorithm was designed for signed multiplication called Baugh-Wooley multiplier algorithm. To hold the signed bits Baugh–wooley is one of the effective way. The effective way of implementing the two's complement numbers is developed with the help of this algorithm. The structure of the Baugh wooley multiplier is shown in the Figure 6. Left shift algorithm is followed in this method. Multiplexer is used for selecting which bit is to be multiplied. The proposed Reversible carry skip adder with Reversible Brent Kung as its core is implanted in this multiplier and the simulation is performed.

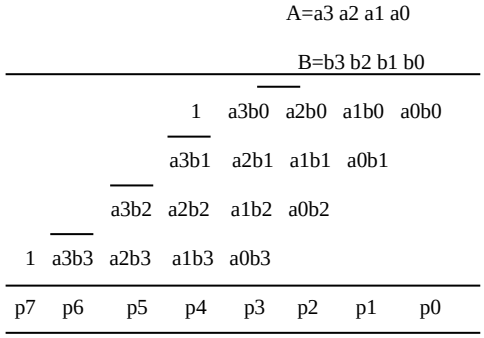

Fig 6: Structure of Baugh-Wooley Multiplier

V. WALLACE TREE MULTIPLIER

The delay of the Wallace tree multiplier is in the order of O (log n). This is very low when compared with the array multiplier. As the operand size increase the delay also increases as it is logarithmically proportional, whereas there is a linear increase in the delay in the array multiplier.

Without propagating the carry to the next stage, all the partial products generated in the column are added together in parallel. The operation continues until two stage at the final stage is reached. Then finally two rows of the matrix are added using the proposed Reversible carry skip adder using Reversible Brent Kung as the core adder. Here 3:2 compressor is used which is also based on carry skip adder. The schematic of 8*8 Wallace tree multiplier is shown in the Figure 7.

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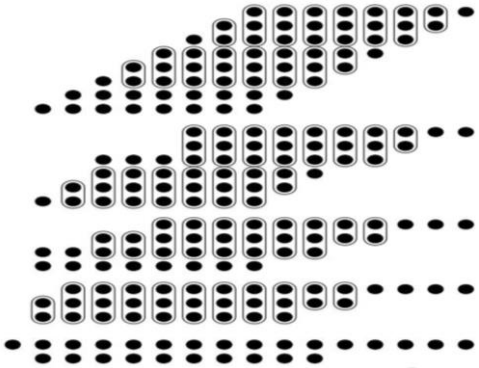

Fig 7 Structure of Wallace Tree Multiplier

Table 2: Comparison of Area, delay, power and energy of Multipliers

MULTIPLIER	BAUGH WOOLEY		WALLACE TREE	
	EXISTING	PROPOSED	EXISTING	PROPOSED
AREA	1342	1129	5230	4351
DELAY (nS)	51.72	42.6	7.327	4.248
POWER (mW)	23.72	18.34	27.44	23.32
ENERGY	1226.79	781.284	201.05	99.063

Table 2 shows the comparison of area, power, delay and energy of Baugh-Wooley and Wallace tree multipliers. It is seen that by using the proposed Reversible carry skip adder with Reversible Brent Kung adder as core structure the area, delay and power decreases by 15.87%, 17.63% and 22.68% for Baugh-Wooley multiplier and 16.8%, 42% and 15.01% for Wallace tree multiplier respectively.

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