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Design of Low Power 8T SRAM Array With Enhanced RNM

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Abstract*: *The paper discusses about the power reduction techniques in a memory cell. Two commonly used SRAM cells, 6T and 8T SRAM are compared in terms of their stability and power gating and MTCMOS technique is implemented to observe power reduction. 8T SRAM cell proves to be more reliable and stable as this has decoupled read and write control paths. The 8T SRAM cell is optimized for better RNM and an array of 4x8 bit cell is constructed with proposed 8T cell. The array with the MTCMOS technique used in the decoder proves 6.9 % power reduction than the circuit without the MTCMOS technique. The 32-bit cell array is constructed with gpdk 180 and consists of 8 write driver circuit, 8 precharge circuit and 8 sense amplifier along with 2:4 decoder and 32 SRAM cells.

Keywords: Low Power, RNM, SRAM, Array, 6T, 8T.

I. INTRODUCTION

Today's technologically connected world generates numerous amount of data and the technology involved in everyday use is required to compute and store this huge amount of data. Memory is an integral part of each electronic device either for storing instructions or data generated by process computation. The most commonly used memory type is the SRAM. This cell is capable of storing single bit of data as long as power is supplied to the cell and does not require periodic refreshing as in the case of the DRAM's. The low power applications such as implantable biomedical devices, handheld devices demands higher energy efficiency to achieve extensive battery life [1-3]. The SRAM memory is used as cache memory in super computers and workstations because of low power and high speed operation. The leakage current comprises of more than 40 % of energy consumption in the high performance IC's [4-5] . SRAM memory array in SOC contributes to most of the leakage and hence designing a low leakage and less power consuming memory block is desirable. In addition to this, the stability of the memory cell for writing and reading the bit stored is of concern and with reduced supply voltage the delay increases. Therefore, a balanced method needs to be proposed to reduce leakage, power consumption and increase stability of the cell.

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The most commonly used 6T SRAM cell has the disadvantage of maintaining required Read Noise Margin (RNM) and Write Noise Margin (WNM) as the technology is scaled down [6]. To overcome this, memory cells with 7T, 8T and 9T were constructed to show they achieve better result than the conventional 6T cell [7-9]. Many researchers have been conducted to reduce the power consumption and leakage current. Quasi power gating approach was implemented to show increased stability and power reduction in the 6T cell [10]. The energy consumption in a memory array is given by [11].

$$E_{total} = E_{switching} + E_{leakage} \qquad (1)$$

Where the $E_{leakage}$ is the energy consumption due to leakage current in the SRAM cell and $E_{switching}$ is the energy consumed during switching activities. In [12] the MTCMOS technique is implemented in 7T cell showing good improvement in reducing power consumption. Dual threshold voltage and stacking technique is implemented in a 9T cell [13] . The research in [14-17] concludes MTCMOS technique proves to be a better choice to reduce leakage power in SRAM's. In this paper we have compared the two commonly used power reduction technique and implemented the best one to construct a 4x8 memory array. Furthermore, in place of the conventional 6T SRAM cell, we have made use of 8T cell with pass transistors and optimized the sizing to achieve better RNM and WNM. The memory array is constructed with gpdk 180 in Cadence Virtuoso and the simulated results are shown.

II. SRAM ARCHITECTURE

SRAM cell is the core element in the SRAM array. Each cell stores a single bit of information. The SRAM cell does not require periodic refreshing and as long as the power supply and is provided the SRAM cell provides constant read and write operations to be performed in it. The traditional 6T SRAM cell comprises of two cross coupled inverters connected to complementary bit lines via access transistors. The information to be stored is written via these access transistors and the information to be read is done by connecting the complementary bit lines to the sense amplifier. The Static Noise Margin (SNM) provides a metric for the stability of SRAM cell[18-21]. The SNM information can be derived for three different operations of the SRAM, called the READ, WRITE and HOLD operation. The SNM graph is plotted by deriving the VTC curve of the two inverters in the cell and these results in a two-lobed curve known as the butterfly curve. The largest possible square that can be embodied in this curve provides the stability information.

The conventional 6T SRAM design is widely used because of very less area consumption. However, it shows very low read stability and write stability and this in turn, seeks for design of a robust SRAM cell. The 8T SRAM cell however has two decoupled paths for read and write operation to be performed. This shows good read and write stability and hence proves to be a better option for designing the SRAM array. The 8T SRAM cell consists of two bit lines (BL and BLB) connected through the two NMOS access transistors and the node where bit is stored is connected to the gate of another transistors whose source is connected to ground. The drain of this transistor is connected to the source of another transistor and the control line for read operation is given to the gate terminal of this transistor known as the Read Word Line (RWL). The Read Bit Line (RBL) provides the read output and this line is precharged before being read. If bit 1 is written through BL, this makes the transistor N5 ON and when RWL is applied then transistor N6 switches ON, draining the charge stored in RWL giving a complementary output. This is shown in Fig. 1.

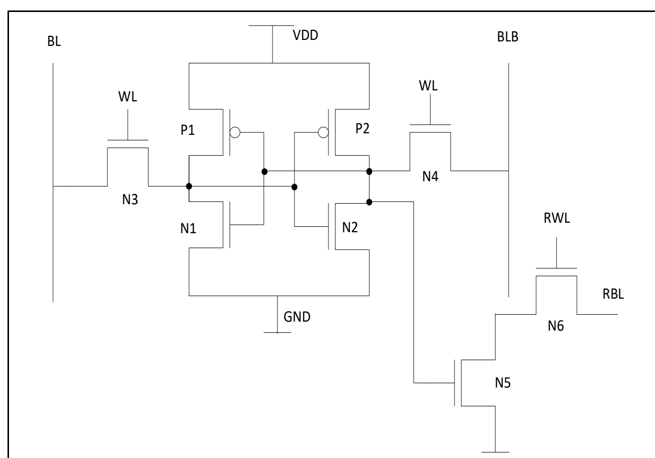

Fig. 1. Conventional 8T SRAM cell

The optimized 8T SRAM is used shown in Fig. 2. This makes use of pass transistors in the read path with the control lines RWL and RWLB connected to the gate of pass transistors. The SNM value is calculated for 6T, 8T and proposed 8T cell. The SNM is calculated for three different modes of operation of the SRAM cell. The proposed 8T SRAM shows significant improvement in terms of read and write stability. The read SNM is affected by ratio of the (W/L) of driver transistors to the access transistors this provides the Cell Ratio (CR). Similarly the write SNM is affected by the ratio of (W/L) of load transistors to the access transistors which provides Pull Up Ratio (PR).

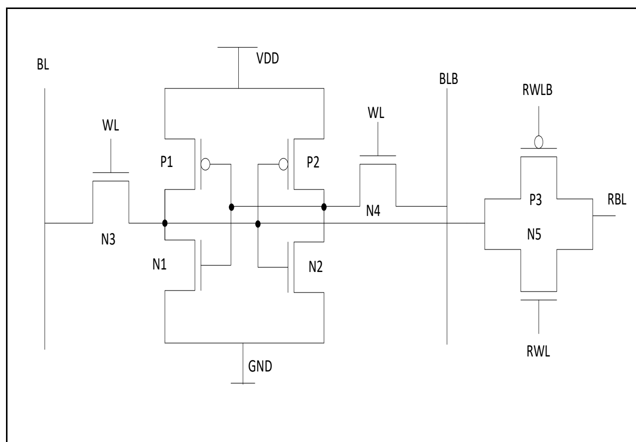

Fig. 2. Proposed 8T SRAM cell.

III. POWER REDCUTION TECHNIQUE

The design of low power SRAM is achieved by implementing different techniques, namely power gating and Multi Threshold CMOS (MTCMOS) technique. Power gating is achieved by placing a transistor in between the SRAM cell and V_{DD} or ground (gnd). Hence, this negates the direct V_{DD} and gnd path and creating a virtual V_{DD} and virtual gnd path. This implementation is shown in Fig. 3. The MTCMOS technique makes use of the sleep transistors of high threshold value which help in reducing the leakage power in the overall circuit. When the circuit is in HOLD mode, the sleep transistors acts a switch cutting off the power supply to the circuit. The implementation of this is shown in Fig. 4.

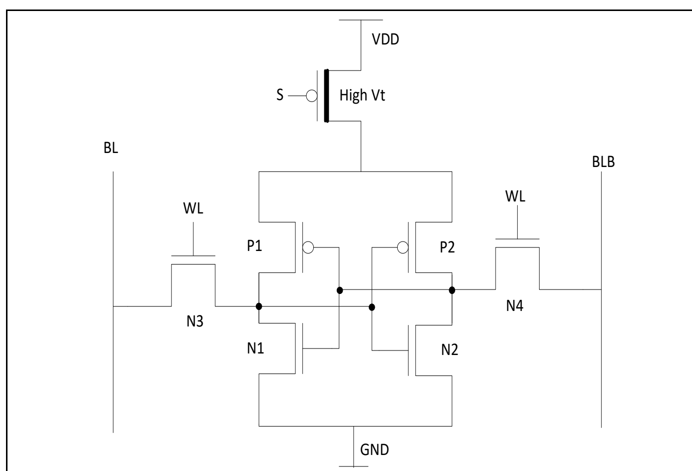

Fig. 3. Power gating implementation in 6T cell.

The comparison of these power reduction techniques can be observed from the Fig. 5. Power gating can be done by two ways, by placing a PMOS transistor between the memory cell and V_{DD} or by placing NMOS transistor between memory cell and ground. Hence, we can observe MTCMOS technique provides significant improvement in terms of power reduction in the circuit. The comparison of MTCMOS technique among 6T and proposed 8T SRAM in reducing power in write and read operation is shown in Fig. 6.

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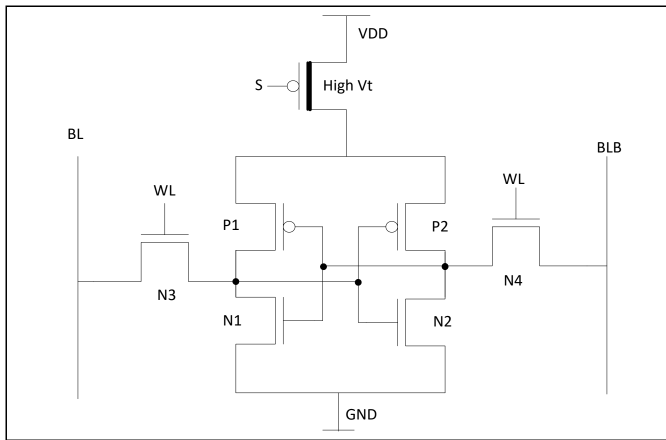

Fig. 4. MTCMOS implementation in 6T cell.

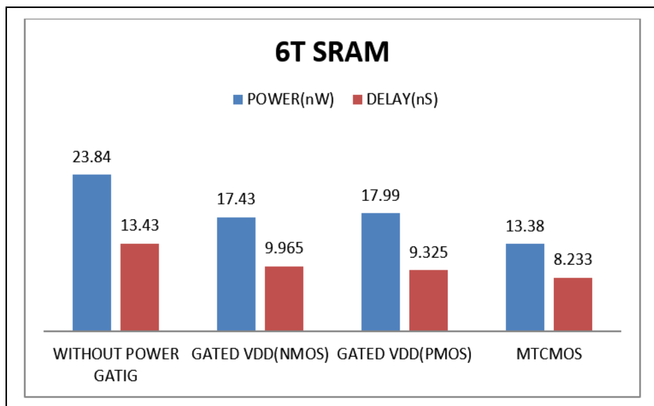

Fig. 5. Comparison of power reduction techniques.

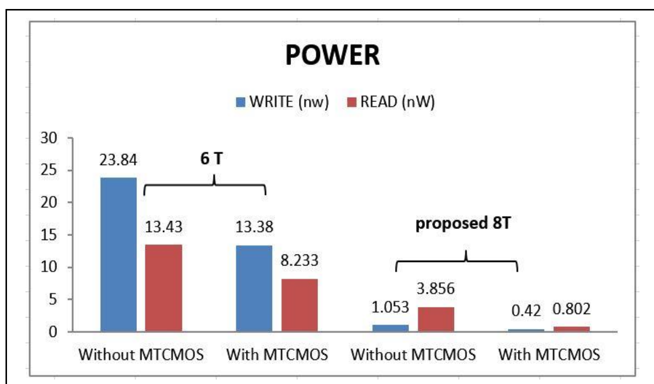

Fig. 6. Power reduction in 6T and proposed 8T cell.

IV. SRAM ARRAY

With the technological advancement taking place at a high pace, the need to have an efficient, reliable and high density memory in a SOC is the need of the hour. The requirement of the amount of memory and the performance depends on the type of application. Hence a memory array facilitates this need and proves to be very efficient in designing a high capacity memory. In the proposed design 4x8 memory array is designed and the power requirement is reduced with the help of MTCMOS technique discussed above. The SRAM array basically has a row decoder, write driver, precharge circuit, sense amplifier and the core memory cell.

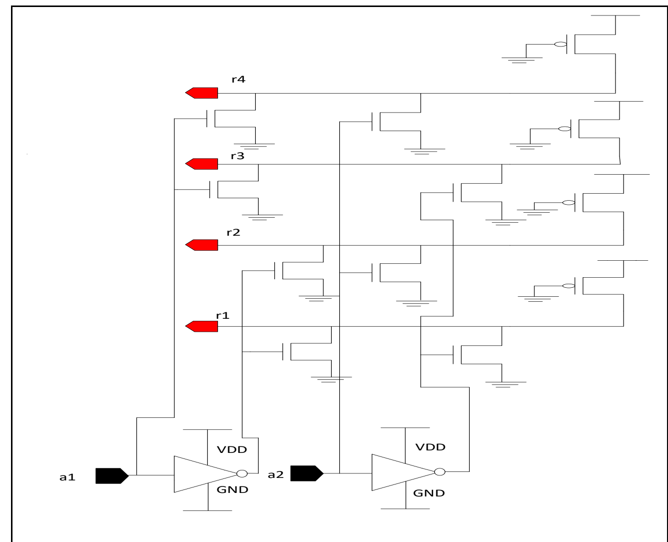

Fig. 7. 2:4 Row Decoder.

A. Row Decoder

The row decoder shown in Fig. 7 is a NOR based 2:4 decoder. The main aim is to select a word line depending on the inputs supplied to the decoder. The inputs to this are a1 and a2 and the outputs provide word line to each of the 4 rows namely r1, r2, r3 and r4.

B. Write Driver

Write driver is used to mainly provide the data to be written into the memory cell by discharging one of the bit lines below the write margin of the SRAM cell from the precharge level. The write driver is controlled by the Write Enable (WE) signal which discharges one of the bit lines to ground. The write driver is constructed by feeding input to the inverter and the output of whose is connected to the drain of one NMOS and to the input of another inverter and the output of the second inverter is connected to the drain of another NMOS transistor, whose source is given to Bit Line (BL). This is shown in Fig. 8.

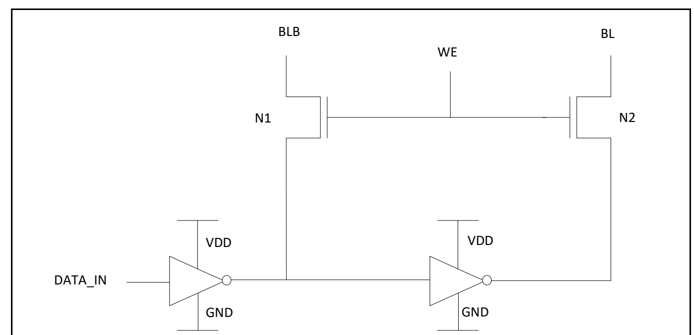

Fig. 8. Write Driver Circuit.

C. Precharge Circuit

The precharge circuit is mainly used to charge the RBL line to V_{DD} so as when the read operation is performed the difference between the precharge line and RBL is amplified and given as output to the sense amplifier. The schematic of the precharge circuit is shown in Fig. 9.

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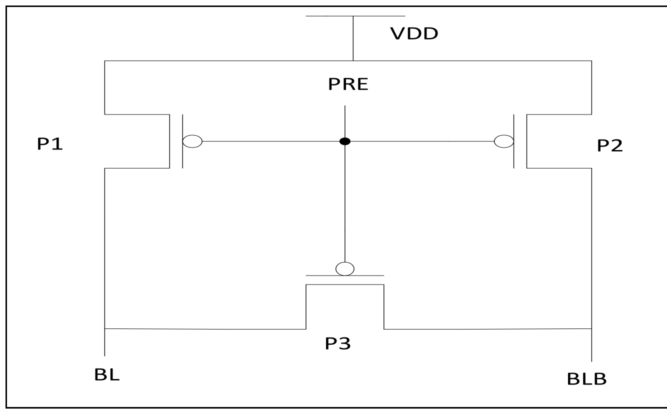

Fig. 9. Precharge Circuit.

D. Sense Amplifier

The main aim of sense amplifier is to sense a small differential voltage developed between the bit lines by the read-accessed cell and amplify it providing a faster read operation. The SRAM array designed in the work involves 8 sense amplifiers, 8 precharge circuit and 8 write drivers. The schematic of sense amplifier is shown in Fig. 10. However, the number of sense amplifiers used can be reduced by using column multiplexing. The sense amplifier is controlled by Sense Enable (SE) and is activated when read operation is to be performed.

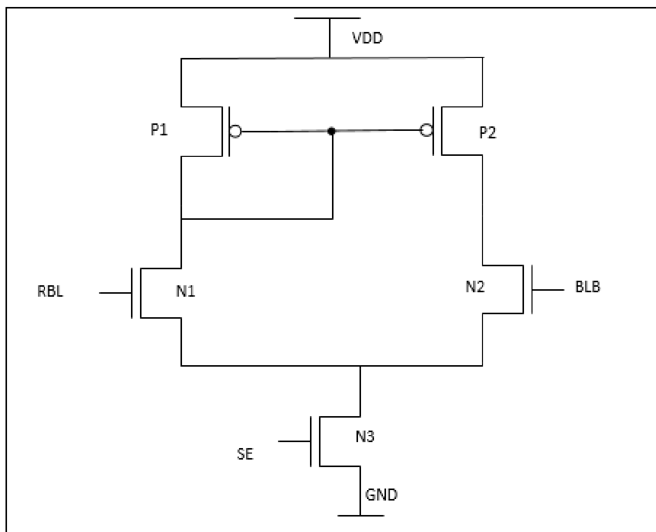

Fig. 10. Sense Amplifier Circuit.

V. RESULTS AND DISCUSSION

The row decoder is constructed and 4x8 memory cell array is designed and power usage is calculated for the design with and without MTCMOS technique incorporated and we observed the MTCMOS implementation provides 6.9 % reduction (from 1.3761 mW to 1.281 mW) in average power. This is considerably good number for such a small array and it can be effective in large density memory array.

The READ SNM calculated for 6T, 8T and proposed 8T design is shown in Fig. 11. Similarly the WRITE SNM is calculated and is shown in Fig. 12. We can observe the proposed design shows significant improvement in terms of both READ SNM and WRITE SNM ensuring good amount of reliability on the memory cell. The CR is fixed for the proposed design is 2.5 and the PR is 0.9.

The 4x8 SRAM array is constructed with the 8T SRAM cell and MTCMOS technique implemented, 2:4 decoder, write driver, precharge circuit and sense amplifier. The schematic of the array is shown in Fig. 13 and the simulation result is shown in Fig. 14. The entire circuit operates with 1.5573 mW power.

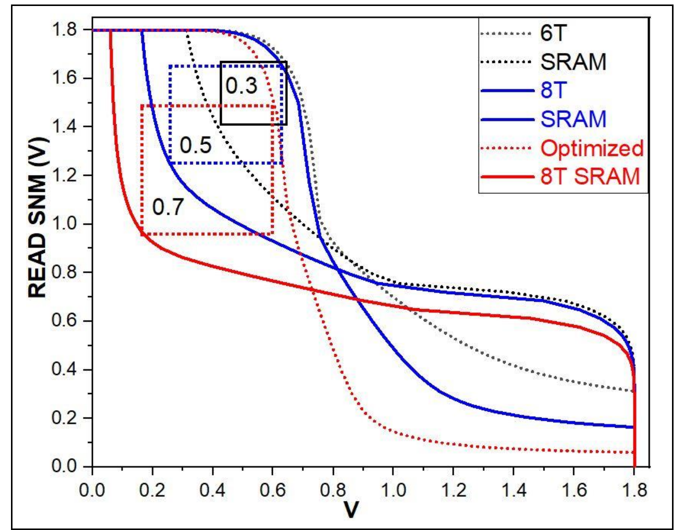

Fig. 11. READ SNM for 3 different SRAM structures.

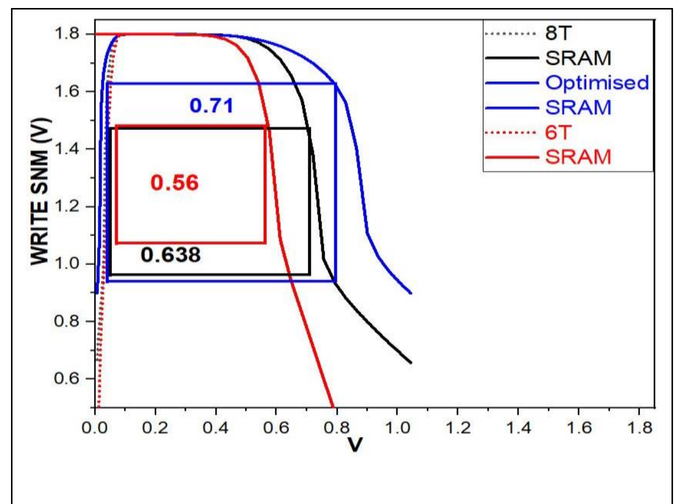

Fig. 12. WRITE SNM for 3 different SRAM structures

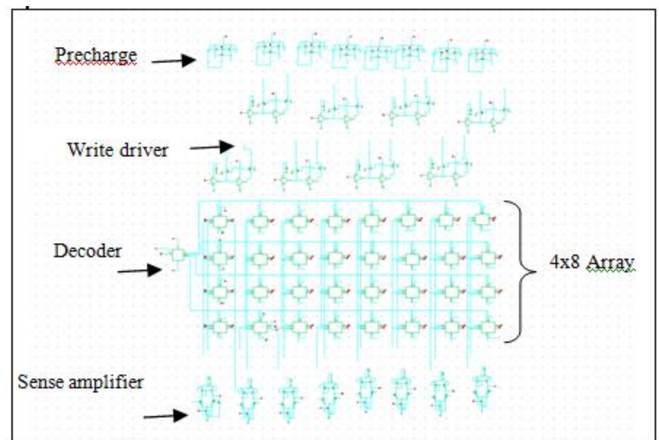

Fig. 13. Schematic of proposed 4x8 SRAM Array

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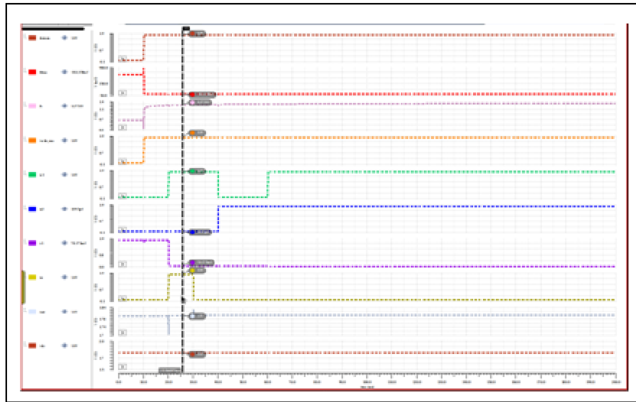

Fig. 14. Simulation result of the proposed 4x8 array

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