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A Design of Phase Locked Loop Based Frequency Synthesizer using 4/5 Prescaler Circuit

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Abstract*: In the arena of communication, The Phase Locked Loop plays an important role in maintaining the phase lock by comparing the output frequency with the input frequency. Because of its wide variety of application such as frequency synthesizers, tracking satellite, demodulation and telecommunication, it needs to operate with low power. The Phase Locked Loop based frequency synthesizer is designed and it uses swallow counter in order to acquire a series of continuous division by working together with dual modulus prescaler. When the static logic is used in the design, it operates with low power but increases delay. When it operates in dynamic logic it consumes more power but speed of operation increases as there is reduced delay. In order to attain both the advantages of static and dynamic logic, Dual Mode Logic method is proposed in the design. In Dual Mode Logic the circuit operates both in static and dynamic modes of operation. In static mode it saves power and in dynamic mode the performance increases. The simulation result shows that the suggested method yields better performance when compared with the CMOS logic for a technology of 0.25um,180nm

***Index Terms*: Dual Mode Logic, Phase Locked Loop, Phase Frequency Detector, Voltage Controlled Oscillator, Prescaler.**

I. INTRODUCTION

Frequency synthesizers [8,9] which is an application of Phase Locked Loop (PLL) is broadly applied in radio communication equipment. These frequency synthesizers select a user defined frequency from the single fixed frequency [1]. From the fundamental frequency, the frequency synthesizer obtains new set of frequencies by performing few mathematical arithmetic operations like addition, subtraction, multiplication etc., the group of crystal resonators in a multichannel radio receiver is replaced by the frequency synthesizers. A crystal oscillator is used to provide reference frequency whereas the frequency synthesizer produces different frequencies which is of low cost also can be controlled by digital circuits. The required output signals are obtained from frequency multiplication, division and mixing operations. In most wireless applications like radio chipsets, cellular phones the PLL based frequency synthesizers are commonly applied circuit.

There are several different types of categories of synthesizer. Each of them obviously has its own advantages and disadvantages. Here indirect method of frequency synthesizer is used. Indirect frequency synthesis is based around phase locked loop technology. Here the output signal is generated indirectly. In other words, the final signal is generated by an oscillator that is controlled by other signals. In this way the signals used in creating the output are indirectly replicated by the output oscillator, thereby giving the name to this technique. The frequency synthesizer can be implemented in two ways. A frequency mixer is placed in between the Voltage Controlled Oscillator (VCO) and Phase detector in an analog frequency synthesizer. For proper operation, an external signal is applied to one end of the mixer but the range of VCO is maintained so that the loop should not get into unstable condition. In digital frequency synthesizer, a digital divider is added in the loop between VCO and the Phase Detector. VCO frequency will be divided by the division ratio of divider and changing the division ratio, the output frequency can be changed. This makes synthesizer programmable. Switching speed is fast, but it is limited to low frequencies due to digital circuits.

II. COMPONENTS OF FREQUENCY SYNTHESIZER

A. Block Diagram

PLL based frequency synthesizer is given in Fig. 1, it comprises of a Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Voltage Controlled Oscillator (VCO) and a programmable divider blocks. PLL design based on Dual mode logic [11] shows the advantages of its operation both in static and dynamic mode thereby reducing the power dissipation, The phase detector compares the output frequency of programmable divider to reference signal (Fref). If there is any frequency difference, it generates an output voltage, which is proportional to the phase error of two signals. The charge pump converts a digital error pulse to an analog current and produces a single input to the loop filter. The loop filter integrates error current to generate control voltage to VCO. Filtering operation of error voltage is performed by loop filter.

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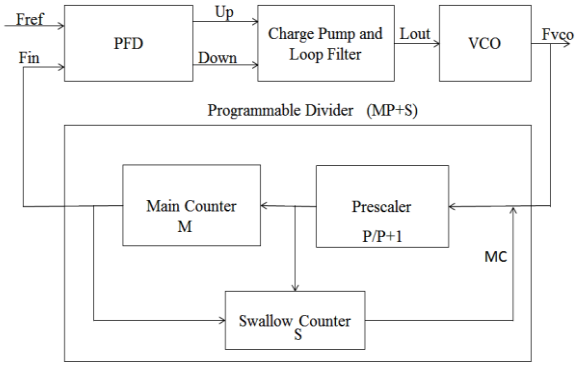

Fig. 1. Block Diagram of PLL Based Frequency Synthesizer

VCO output (Fvco) is divided down based on the division ratio of programmable divider. The output frequency of VCO is given by the equation

$$f_{vco} = \frac{f_{ref}}{N} \quad (1)$$

where N is the division ratio of programmable divider and is equal to MP+S. where M, P and S are the division ratio of main counter, program counter and swallow counter

B. Phase Frequency Detector (PFD)

The two D-type flip-flop (DFF) implemented in order to form PFD. The upper and lower DFFs generate UP and DOWN signals as shown in Fig. 2. The generated UP and DOWN signals are given as input to the charge pump. When external input Fref arrives first at the upper DFF, the UP signal is generated to turn on the charge pump. When oscillator frequency Fin arrives at the lower DFF, DOWN signal is generated which connect the DOWN value to the charge pump. When both UP and DOWN are at logic high, NAND gate resets both DFFs to output logic 0. Thus the phase difference between the two signals are detected and used to turn on either the current sink or current source of the Charge Pump. Here the D value is always connected with Vdd. The PFD can even achieve lock when it is in off frequency and is known as Phase Frequency Detector.

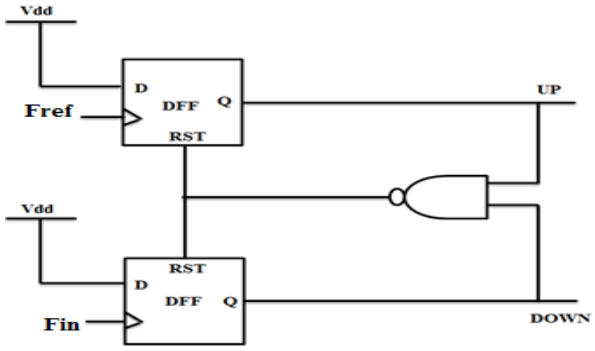

Fig. 2. Phase Frequency Detector

C. Charge Pump

A Charge Pump (CP) is provided with the input from the PFD. The UP and DOWN signals are given as input as shown in Fig. 3. The upper most transistors are connected with the source Vdd and lower most transistors are connected with ground. The inverted UP input is given to the PMOS so, that when the UP input is high the PMOS connects output with the source. Similarly when the DOWN signal is high the NMOS connects output with the ground. Charge pump circuit is used to combine both the outputs of the PFD and provide a single output which is fed to the input of the loop filter.

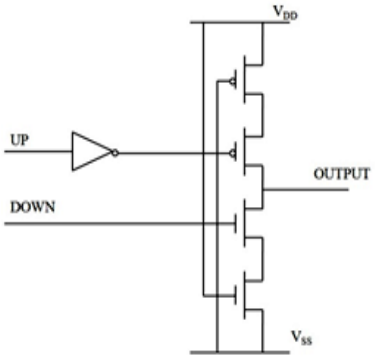

Fig. 3.Charge Pump

D. Loop Filter

The loop filter is typically a simple passive filter. Filters are frequently added after the charge pump to reduce the ripple. The purpose of the loop filter is to change the output signal of phase frequency detector to control voltage and as well as to filter out noise of high frequency value produced by the PFD. The loop filter used with this type of PFD is a simple RC low-pass filter. A low pass filter consists of a resistor and capacitor which passes low frequency signals and blocks the high frequency signal.

E. Voltage Controlled Oscillator

An electronic oscillator known as VCO, whose Oscillation frequency is controlled by a control voltage input. Here the instant value of oscillation frequency is regulated by the applied input voltage. When the control voltage increases VCO output frequency increases and is proportional to the control voltage [10]. Therefore, modulating signals applied to control input may cause frequency modulation (FM) or phase modulation (PM). In a voltage-controlled oscillator, a voltage input controls the resonant frequency. They generally require a relatively small area and can be more easily integrated with digital CMOS circuits, reducing cost. Also, they have a wider tuning range than LC oscillators, making them more robust over process variations The VCO is a useful circuit because its oscillation frequency can be set to a desired value. The equation for VCO is given by the equation 3.

$$f_{vco} = f_o + K_{vco} V_{ctrl} \quad (3)$$

f_o is the centre frequency of VCO. It is the frequency at which it oscillates with no external control. It is referred to as free running frequency. K_{vco} is the gain of the VCO that controls how much a change in control voltage that change VCO frequency. V_{ctrl} is the input voltage that makes VCO such an important and useful circuit.

F. Programmable Divider

The programmable divider is based on the pulse swallow topology and is used to carry out more than one division. The important components of programmable divider are main counter, prescaler and swallow counter.

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G.Dual Modulus Prescaler

In order to design a high speed frequency synthesizer, the design or circuit needs to have dual modulus or multi modulus divider that is of high speed. In the proposed design the dual modulus prescaler based programmable divider architecture is utilized. Using a standard prescaler, reduces the system resolution. but without loss of resolution a high speed can be addressed by using a dual-modulus prescaler which has the advantages of a standard prescaler. A dual-modulus prescaler is a counter whose division ratio can be switched from one value to another by an external control signal. It consists of two separate frequency divisors, namely P and P+1 and is used to carry out more than one division. The block diagram of prescaler is shown in Fig. 4. It performs either P bit division or P+1 bit division based on the control signal given by the swallow counter. Initially it will perform P+1 bit division and it changes with the control input. Here the prescaler is designed to perform either 5 or 4 bit division.

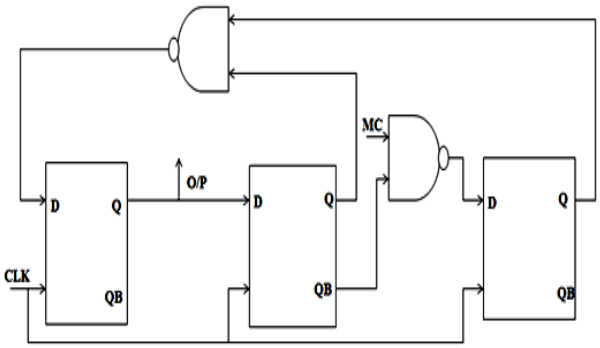

Fig. 4. Block Diagram of 4/5 Prescaler Circuit

Dual modulus prescaler consist of three D Flip-Flop (DFF) and two NAND gates, initially the first 2 DFF produce 4-bit division output. An extra clock period delay for divide by 5 is added by third DFF. The propagation delay through the Flip-flops and NAND gate decides the maximum operating frequency of prescaler. So DFF and NAND gates are used together to reduce the delay.

H. Swallow Counter

The programmable divider which is used in frequency synthesizers has three building blocks among them the swallow counter is given in Fig 5. The purpose of swallow counter is to control the dual modulus prescalar that is programmed to divide either by P or P+1.The aim of the pulse-swallow counter is to acquire a series of continuous division by working together with dual modulus prescaler. The swallow counter divides the prescaler output by a programmable ratio of S. The prescaler divides by P+1 until swallow counter is full. After (P+1)s pulses at input changes modulus control signal to P. The swallow counter receives the output obtained from the prescaler as input. For every single M input pulses, the main counter generates one output pulse. As the name the swallow counter, swallows 1 from P+1 of the dual modulus prescaler. In shallow counter design, five D flip-flops are linked in cascade method. Here output of one F-F is given as input to other F-F and NAND gate is connected with the controlling input.

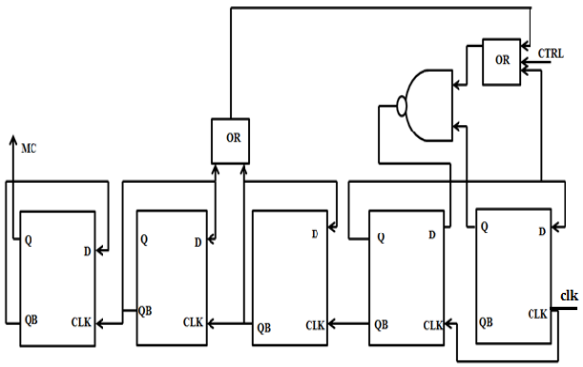

Fig. 5. Block Diagram of Swallow Counter

I. Main Counter

The main counter also performs the division operation as prescaler; it performs a fixed bit division. The prescaler output is given as the clock input to the main counter. Here the main counter is designed to perform fixed 20 bit division. The block diagram of main counter is shown in the Fig. 6. It uses five DFF and a NAND gates, the inverted output of the first DFF is given as clock to the next Flip-Flops. The divided output from the main counter is given as input to the VCO.

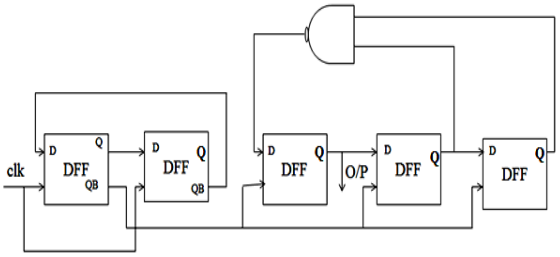

Fig. 6. Block Diagram of Main Counter

III. Simulation of PLL Based Frequency Synthesizer

All the individual blocks of PLL are integrated in order to obtain the complete frequency synthesizer. The simulation model of PLL based frequency synthesizer is shown in the Fig. 7. The output from the loop filter is given to the VCO and its output is given as feedback to the programmable divider and frequency division is carried out. The frequency divider output is given as reference clock input of the Phase Frequency Detector. Before giving the control voltage to the VCO, it oscillates with constant frequency. The division ratio is given by the equation

$$N=MP+S \qquad (4)$$

$$=20*4+16$$

$$=96$$

The programmable divider performs a total division of 96 bit based on the value of prescaler, main counter and swallow counter. This divided input is given as the feedback input to the Phase Frequency Detector.

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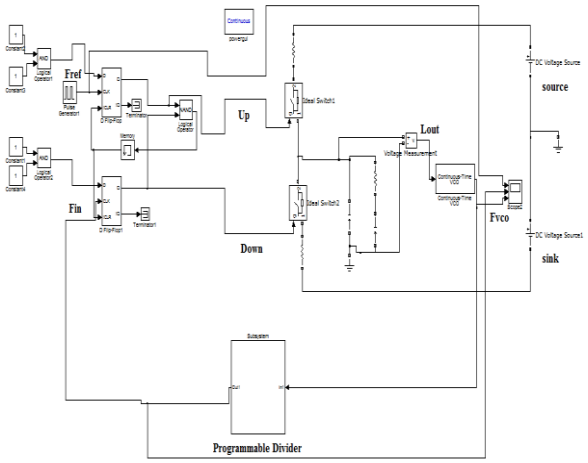

Fig. 7. Simulation Model of PLL Based Frequency Synthesizer

The output waveform of PLL based frequency synthesizer is shown in the Fig. 8. The first waveform corresponds to the input clock given externally and the second waveform corresponds to the feedback clock taken from the programmable divider. The final waveform is the output taken from the VCO. Time period of input signal is 3.5ms and is inversely proportional to the frequency. So, the input clock frequency Fref is calculated as 0.285 kHz and the output frequency of programmable divider is 20 kHz. On dividing the programmable divider value by the division ratio 96, the feedback frequency equals the input frequency.

The output waveform shows that VCO oscillates with high frequency when the input Fref is high. The oscillation decreases with the decrease in control voltage, when the Fref is low.

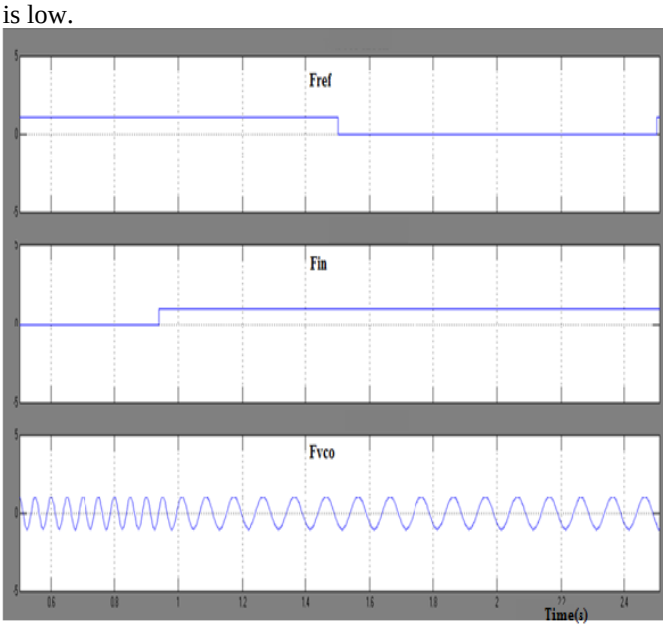

Fig. 8. Output Waveform of PLL Based Frequency Synthesizer

A.Hardware Implementation of PFD

The Spartan-3E family builds on the success of the earlier Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These Spartan-3E FPGA enhancements combined with advanced 90 nm process technology, deliver more functionality and bandwidth. The FPGA configuration is generally specified using a hardware description language (HDL). By using synthesis tools, the modeling, verification and implementation processes can be integrated. The major advantage of synthesis based designs is that the same hardware description language code can be used for verification and implementation. The Dual Mode Logic based PFD is designed using the Xilinx version 13.4 and is compared with the static logic PFD. The hardware implementation of these circuits is done using FPGA Spartan-3E kit.

B. DML Phase Frequency Detector

The DML (Dual Mode Logic) gates family was proposed in order to provide a very high level of energy-delay [3,4,5,6,7] optimization flexibility. DML allows changing between two operational modes at the gate level: static mode and dynamic mode. In the static mode, DML gates consume very low energy, with some performance degradation, as compared to standard CMOS gates. Alternatively, dynamic DML gates operation obtains very high performance at the expense of increased energy dissipation. Dual mode logic was used to allow switching between static and dynamic modes of operation. Frequency synthesizer is constructed using DML. Block of DML PFD circuit is given in Fig. 9.

The waveform of PFD is shown in the Fig. 10. The D input of both the flip-flops always stays at high value. Fref and Fin are represented by ‘a’ and ‘b’. Up and Down values are represented by ‘qa’ and ‘qb’. Set high represents the D value. Initially the qa output is in high impedance state represent by blue line, as the Fref value corresponds to zero. When both the inputs Fref and Fin are high, the output qa and qb are reset to 0. Then any one of the output goes high with raise in the equivalent input values.

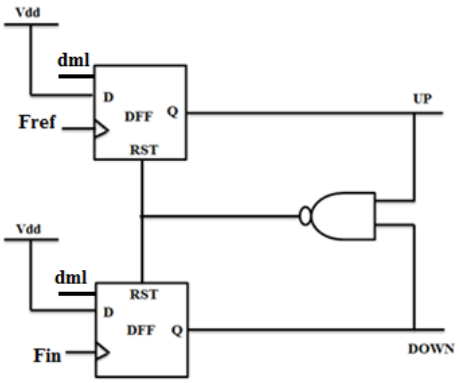

Fig. 9. DML PFD Circuit

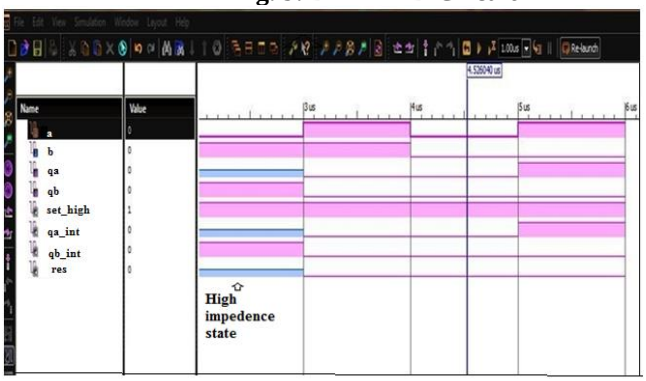

Fig. 10. Output Waveform of PFD

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The waveform of DML PFD is shown in the Fig. 11. The qa_int, qb_int represent the signals to the feedback NAND gate. DML clock is represented by dml; s and g represent the signal VDD and VSS of DML NAND. Set high represent the D value of the DFF. Here the DFF is replaced by DML DFF. Operation of DML PFD is same as normal PFD, when DML clock value is high and it goes to undefined state when the DML clock value is low. The undefined state is represented by green line.

Once the syntax is checked, post synthesis simulation is performed and the waveforms captured are shown in Fig. 11. The simulated codes have been synthesized for the selected target device as shown in Fig. 12 and the pin assigned is done for the corresponding switches and LED's through the user constraints option. After loading the program into the FPGA kit, the output can be verified with the successful implementation of the code. The power Value of PFD and DML PFD is calculate as 0.081mW. The power value remains same irrespective of the increase in no of transistors. The hardware implementation of the DML PFD for the synthesized circuit using FPGA kit is done.

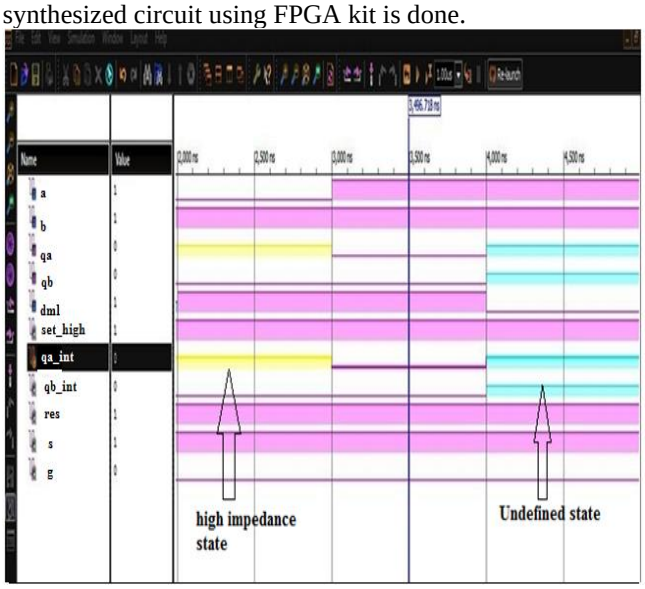

Fig. 11. Output Waveform of DML PFD

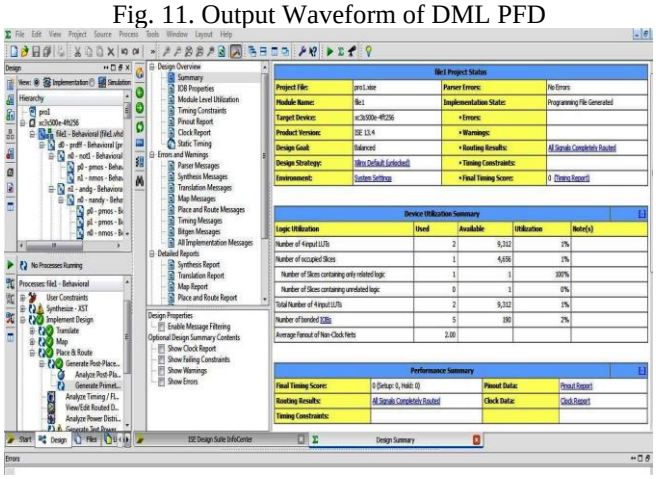

Fig. 12. Synthesis Report of DML PFD

C.Delay Comparison

The synthesis of NAND gate, DFF, PFD using the static CMOS logic [2] and DML logic is done using the Xilinx 13.4 tool and the delay comparison is done using the synthesizes results obtained during the execution of the code. The table shows the delay value of blocks in DML method is reduced by 20-30% when compared with the conventional logic. The DML method can reduce the overall delay of the frequency synthesizer circuit.

Table I. Delay Comparison

BLOCK	STATIC CMOS LOGIC	DML LOGIC
NAND GATE	6.557ns	6.209ns
D FLIP-FLOP	9.223ns	9.008ns
PFD	7.494ns	7.283ns

IV. CONCLUSION

The digital PLL using Dual Mode Logic is designed and simulated using the TANNER tool version 13.0 using 180nm, 0.25um and few technology files. The performance of different logics is compared and the result shows that Dual Mode Logic reduces the total power consumption by 2-3% in microwatt and also reduces the computational delay by 3%. Hence the total performance of the circuit improves. This frequency range renders the designed phase locked loop architecture that can be used as clock generator in microprocessors. It has been identified that substantial settling time enhancement is achieved by proper division of the swallow and main counter for 4/5 scaling techniques. This Dual mode PLL based Frequency synthesizer architecture provides a new pathway for high speed design of signal processing applications

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