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VLSI based Low Power Multiply Accumulate Unit Employing Kogge Stone Adder with Modified Pre-Processing and Post-Processing Stages

Rakesh S, K. S. Vijula Grace

Abstract*: The high demand of low power electronic devices necessitates the implementation of novel power management strategies in wide range of applications including signal processing in biomedical device applications. Digital hearing aid is such a biomedical device that uses a Digital Signal Processor (DSP) with a MAC unit and several filters for faster processing, better acoustic signal capture and better noise rejection. The device is designed to help patients having hearing impairment. The objective of this paper is to implement a Multiply Accumulate (MAC) unit based on a modified Kogge Stone adder (KSA) for a DSP module. The unit is designed using Verilog Hardware Description Language (HDL) and simulated and synthesized using Xilinx Vivado Design Suite 2015.2. The design is synthesized for Artix-7 series Field Programmable Gate Array (FPGA). The analysis showed that the proposed design has significant improvement in the power consumption and the figure of merit. The 16 bit design showed an improvement of 11.29% in the power consumption and 6.18% in the figure of merit.

Index Terms*: Digital signal processor, Kogge Stone adder, Modified Inequality detector, Multiply accumulate unit, Vivado design suite.

I. INTRODUCTION

The rapid technological advancement in the field of microelectronics supports the development of low power and portable biomedical devices. The VLSI engineers are always facing the challenge to design and implement power efficient modules. There is always a high demand for portable biomedical device designs which has lower power consumption. igital hearing aid is such a highly demanded portable low power biomedical device which uses a Digital Signal Processor (DSP) in it. Low power signal processor design can be incorporated into the hearing aid which will help the patients to have an efficient implantable or wearable hearing aid. The main unit in a DSP module is a Multiply Accumulate (MAC) unit. The MAC unit has a multiplier, an adder and an accumulator register as shown in Figure 1. The MAC unit performs multiplication and accumulation. The power consumed by DSP unit is mainly determined by the power consumption of the MAC unit. A low power MAC unit employed in a DSP module will reduce the overall power consumption of the module. The MAC unit may be used to design a filter that rejects noise and captures the required acoustic waves as in the case of a digital hearing aid. A design scheme is proposed here to reduce the power consumption of the MAC unit. A power efficient MAC unit will facilitate proper energy management in the DSP module.

A design scheme has been proposed here to reduce the power consumption of the MAC unit. The MAC unit is designed using a modified Kogge Stone Adder (KSA) in which the pre-processing stage and the post processing stage are modified. The Kogge Stone Adder with Modified Pre-processing and Post processing stages (KSA_MPPS) is used in the multiplier stage and the adder stage of the MAC unit. The coding is done using Verilog HDL in the tool Xilinx Vivado Design Suite 2015.2. It is synthesized for Artix-7 series Field Programmable Gate Array (FPGA).

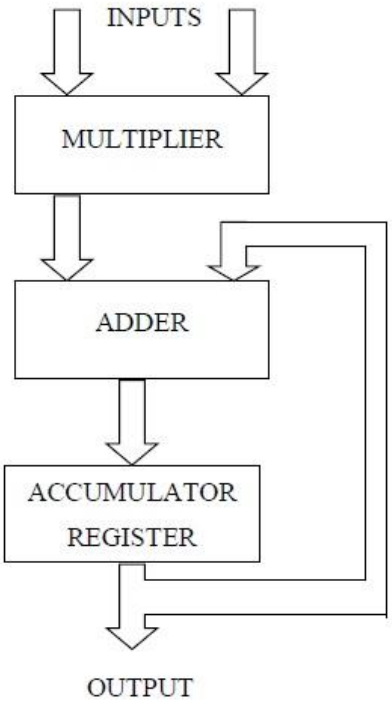

Fig. 1: General architecture of MAC unit

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***** Correspondence Author (s)
Rakesh S*, Department of Electronics and Communication Engineering, Noorul Islam Centre for Higher Education, Thuckalay, Tamil Nadu, India and Mangalam College of Engineering, Ettumanoor, Kerala, India.
K. S. Vijula Grace, Department of Electronics and Communication Engineering, Noorul Islam Centre for Higher Education, Thuckalay, Tamil Nadu, India.

The rest of the paper is organized as follows. In Section II, the literature review is explained in detail. Section III describes the methodology of the proposed scheme. The simulation results are discussed in Section IV and finally the concluding remarks are given in Section V.

II. LITERATURE REVIEW

There has been extensive research going on in the area of low power digital signal processing during the past two decades. Mohamed Asan Basiri et al. [1] introduced a different floating point MAC structure compared to the conventional one. He combined the multiplier and adder block and formed a new block called multiplier-accumulator block and used Wallace tree for multiply accumulation process. Tung Thanh Hoang et al. [2] proposed a two's complement MAC architecture which used a carry save adder as the final adder. The carry save adder contained 3:2 counters and it used shorter interconnects.

S Ahish et al. [3] developed a MAC unit with a partial product reduction block and the multiplier was implemented using Brent Kung adder. The design achieved better area, delay and power performance compared to the conventional multiplier employing Booth algorithm. Nithish Kumar V et al. [4] incorporated a modified carry select adder at the multiplier stage of the MAC unit to improve the area. A digital filter is then designed using the MAC unit which achieved significant reduction in area and power. Maroju Saikumar et al. [5] introduced four different MAC architectures which employed carry save adder at the adder stage and four different multipliers. The four different multipliers used in the design were Array Multiplier, Ripple Carry Multiplier with row bypass technique, Wallace Tree Multiplier and Dadda Multiplier.

Narendra C.P et al. [6] developed a partial product reduction stage using 29 compressors. Compressor architectures were also utilized in the carry propagation adder stage and accumulation stage. A. Abdelgawad [7] designed a merged architecture which combined the accumulation stage with the multiplier circuit. The speed and throughput of the MAC unit were increased and the area was decreased. Suryasnata Tripathy et al. [8] introduced a power efficient Vedic multiplier and realized using 45nm CMOS technology. He presented new design for 4-bit and 8-bit multipliers based on the URDHVA TIRYAKBHYAM (UT) sutra in Vedic Mathematics. The design was based on transmission gate logic and pass transistor logic. The design was realized using Cadence EDA tool with a 1V power supply by using several test inputs. The design showed improvement in speed, power consumed and chip area. The partial product generation unit designed using 5T AND gates helped to reduce the chip area. The UT sutra based design was responsible for the speed and power performance. S.Rakesh et al. [9] reviewed the design of different MAC unit architectures.

III. PROPOSED METHOD

In the proposed system a modified Kogge Stone adder (KSA) is used at the adder stage in the MAC architecture. The modification is done at the preprocessing and the post processing stages of the adder. The preprocessing and post processing stages consist of an inequality detector which performs exclusive OR operation. The inequality detector is designed here using a 4 transistor logic. Switch level modeling is used to design the logic. The logic used is similar to the Gate Diffusion Input (GDI) logic.

Kogge Stone adder is a type of Parallel Prefix adder which has $\log_2 N$ number of stages where N is the number of bits. It has low logic depth and hence has lesser computational delay [10]. The adder therefore performs faster. The fanout is also minimum for Kogge Stone adder [11-12].

Kogge Stone adder consists of a Propagate bit and Generate bit block (BGP) in the pre-processing stage, Group Generate and Propagate block (GGP) and Group Generate (GG) block in the carry computation stage and finally an inequality detector in the post processing stage for sum calculation.

BGP block generates the propagate bit

$$P_i = A_i \; xor \; B_i \tag{1}$$

where P_i is i^{th} Propagate bit, A_i is i^{th} A input, B_i is i^{th} B input, xor is 'xor' operation in digital.

and generate bit

$$G_i = A_i \; and \; B_i \tag{2}$$

where G_i is i^{th} Generate bit, A_i is i^{th} A input, B_i is i^{th} B input, and is 'and' operation in digital.

Figure 2 shows that GGP block generates

$$G = G_i + P_i . G_{previous} \tag{3}$$

$$P = P_i . P_{previous} \tag{4}$$

where G is Group Generate bit, P is Group Propagate bit, $G_{previous}$ is Generate bit from previous stage, $P_{previous}$ is Propagate bit from previous stage, + is 'or' operation in digital, . is 'and' operation in digital.

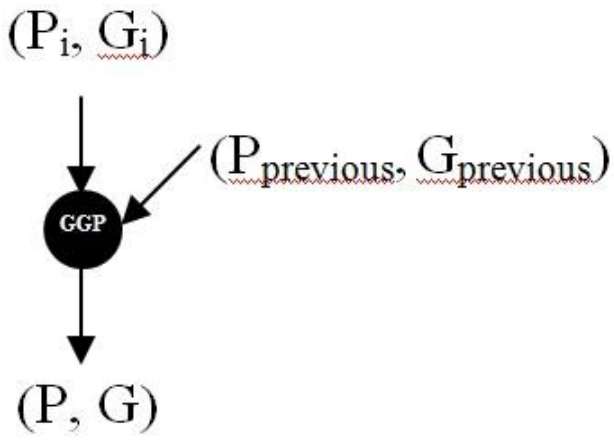

Fig. 2: Generation of Group Generate and Propagate bits

Figure 3 explains that GG block generates

$$G = G_i + P_i . G_{previous} \tag{5}$$

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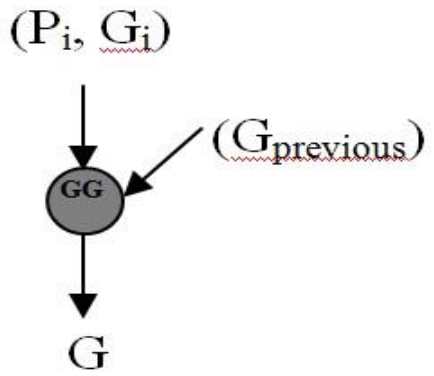

Fig. 3: Generation of Group Generate bit

Figure 4 clearly shows how the GGP block and GG blocks are used to compute the carry at different stages of KSA. The expressions for the generation of carry C_0 to C_7 are also given in (6) to (26).

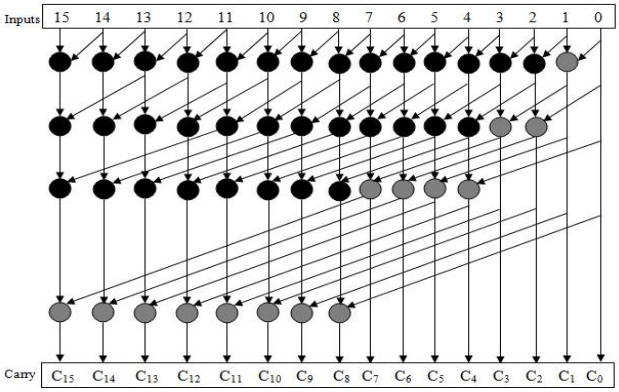

Fig. 4: Structure of a 16 bit Kogge Stone Adder

$$C_0 = G_0 + P_0\, C_{in} \quad (6)$$

$$C_1 = G_1 + P_1\, C_0 + P_1P_0\, C_{in} \quad (7)$$

$$C_1 = G_{1:0} + P_{1:0}\, C_{in} \quad (8)$$

$$C_2 = G_2 + P_2G_1 + P_2P_1C_0 = G_{2:1} + P_{2:1}C_0 \quad (9)$$

$$C_3 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0\, C_{in} \quad (10)$$

$$C_3 = G_3 + P_3G_2 + P_3P_2(G_1 + P_1G_0) + P_3P_2P_1P_0\, C_{in} \quad (11)$$

$$C_3 = G_{3:2} + P_{3:2}\, G_{1:0} + P_{3:2}\, P_{1:0}\, C_{in} \quad (12)$$

$$C_3 = G_{3:0} + P_{3:0}\, C_{in} \quad (13)$$

$$C_4 = G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1C_0 \quad (14)$$

$$C_4 = G_4 + P_4G_3 + P_4P_3(G_2 + P_2G_1) + P_4P_3P_2P_1C_0 \quad (15)$$

$$C_4 = G_{4:3} + P_{4:3}G_{2:1} + P_{4:3}P_{2:1}C_0 \quad (16)$$

$$C_4 = G_{4:1} + P_{4:1}C_0 \quad (17)$$

$$C_5 = G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4P_3G_2 + P_5P_4P_3P_2C_1 \quad (18)$$

$$C_5 = G_5 + P_5G_4 + P_5P_4(G_3 + P_3G_2) + P_5P_4P_3P_2C_1 \quad (19)$$

$$C_5 = G_{5:4} + P_{5:4}G_{3:2} + P_{5:4}P_{3:2}C_1 \quad (20)$$

$$C_5 = G_{5:2} + P_{5:2}C_1 \quad (21)$$

$$C_6 = G_6 + P_6G_5 + P_6P_5G_4 + P_6P_5P_4G_3 + P_6P_5P_4P_3G_2 + P_6P_5P_4P_3P_2C_1 \quad (22)$$

$$C_6 = G_6 + P_6G_5 + P_6P_5(G_4 + P_4G_3) + P_6P_5P_4P_3(G_2 + P_2C_1) \quad (23)$$

$$C_6 = G_{6:5} + P_{6:5}G_{4:3} + P_{6:5}P_{4:3}C_2 \quad (24)$$

$$C_6 = G_{6:3} + P_{6:3}C_2 \quad (25)$$

$$C_7 = G_{7:0} + P_{7:0}C_{in} \quad (26)$$

The carry bits are used to compute the final sum using the expression given in (27).

$$S_i = P_i\ xor\ C_{i-1} \quad (27)$$

Thus the pre-processing stage uses an inequality detector to compute the "Propagate bit,P_i" from the input bits A_i and B_i. The post processing block also uses an inequality detector to generate the final "sum bit, S_i". Inequality detector performs exclusive OR operation. It gives a high output when the inputs are unequal and hence the name inequality detector. The modified inequality detector is designed using the switch level modeling in Verilog HDL code. It is implemented using 4 MOS transistors out of which there are 2 PMOS transistors and 2 NMOS transistors. The conventional transistor implementation of the inequality detector needs 12 MOS transistors out of which 6 are NMOS transistors and 6 are PMOS transistors. The NAND gate architecture of realizing XOR function involves 16 transistors and the pass transistor logic used to implement the feedback element of the bit swapping linear feedback shift register in [13] requires either 6 or 7 transistors. Thus there is a reduction in the number of transistors in the circuit which reduces the power consumption appreciably and improves the power-delay product also. The improved XOR design can also be implemented in reversible circuits as the number of XOR logic in the output determines the hardware complexity of reversible circuits [14]. Figure 5 shows the circuit diagram of the modified inequality detector.

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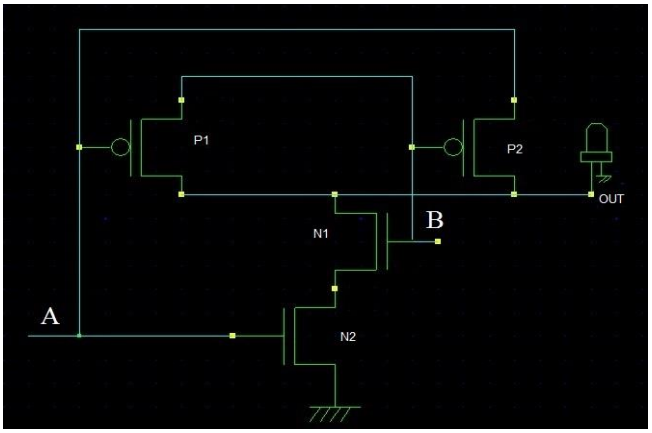

Fig. 5: Proposed Inequality detector design

The working of the proposed inequality detector is explained hereafter. When both A and B are zero, both pmos will be on and both nmos will be off. Hence the input of the pmos is transferred to the output. So output is pulled to zero. When AB=01, pmos P1 will be on and P2 will be off. Similarly nmos N1 will be on and N2 will be off. Hence the source voltage of P1 which is logic 1, is moved to the output. When AB=10, pmos P1 will be off and P2 will be on. Similarly nmos N1 will be off and N2 will be on. Here the source voltage of P2 will reach the output and hence the output becomes 1. When both the inputs are high AB=11, both pmos will be off and both nmos will be on. This will pull down the output to ground potential. Low swing can be caused at the output when A=0 and B=0. In that case we expect the output to be zero but due to the poor high to low transition characteristics of the pmos, the output will be $V_{Tp.}$ [15]. The proposed architecture of the multiply accumulate unit that can be used in a Digital Signal Processor is given in Figure 6. The design may be used for several biomedical applications, for example, in a digital hearing aid. The architecture employs a modified Vedic multiplier which uses a modified Kogge Stone adder to sum up the partial products. At the adder stage the modified Kogge Stone adder is incorporated to add the result of multiplication and the previous result stored in the accumulator register. The accumulation process is actually taking place at the adder stage. The final result is again stored in the register. The accumulator register is basically a parallel in parallel out shift register.

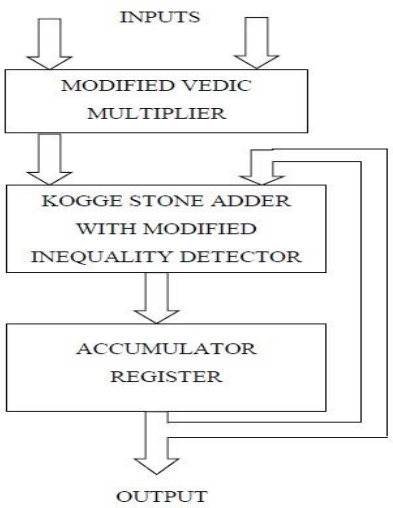

Fig. 6: Proposed MAC Architecture

IV. RESULTS AND DISCUSSION

The simulation result of the modified inequality detector and the proposed MAC unit is presented in Figure 7 and Figure 8 respectively. A comparison between the existing MAC design and the proposed design is given in Table 1. The comparison table clearly reveals that the proposed 16 bit MAC design contributes to a power saving of almost 11.29% compared to the conventional design. The figure of merit (FOM) which is the power-delay product of the device has also showed an improvement of 6.18%. Also the power reports generated are shown in Figure 9 and 10. Figure 11 and 12 presents a graphical comparison of onchip power and power-delay product of the 16 bit MAC units.

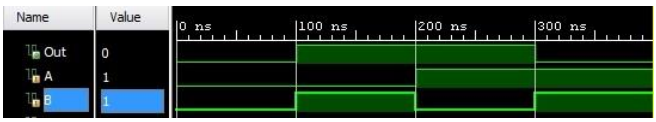

Fig. 7: Simulation result of modified inequality detector

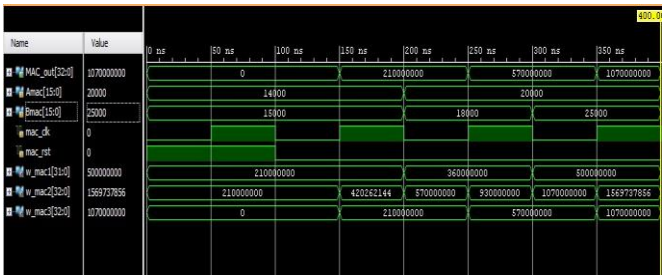

Fig. 8: Simulation result of 16 bit MAC unit with modified Kogge Stone adder

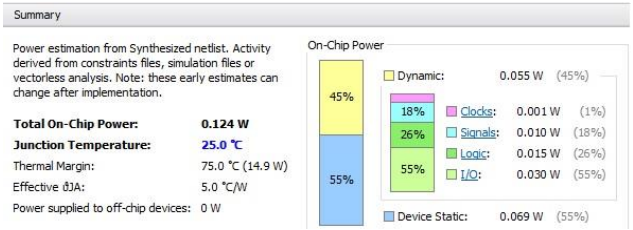

Fig. 9: Power report of 16 bit MAC unit with Kogge Stone adder

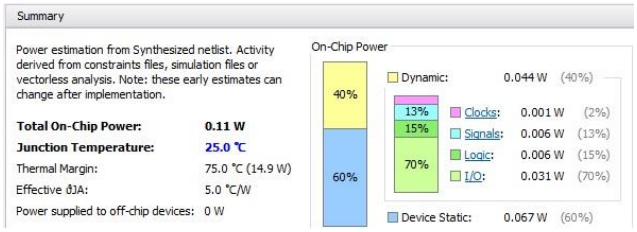

Fig. 10: Power report of 16 bit MAC unit with modified Kogge Stone adder

Table 1: Comparison of MAC Architectures

Architectures	On Chip Power (W)	Power Delay Product (nJ)
16 bit MAC using Kogge Stone adder	0.124	1.473

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Proposed 16 bit MAC using Modified Kogge Stone Adder (KSA_MPPS)	0.11	1.382

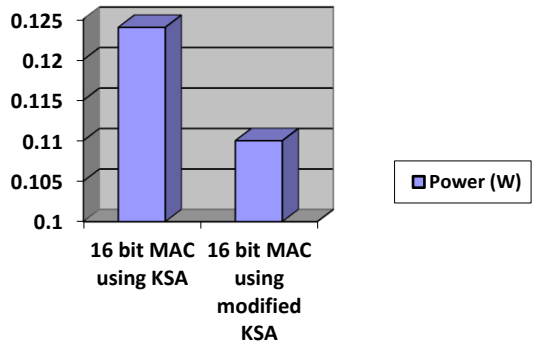

Fig. 11: Power comparison of 16 bit MAC architectures

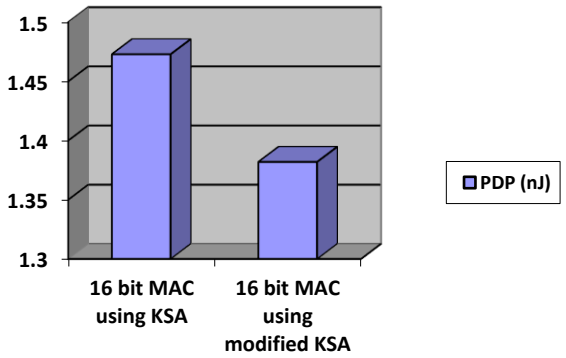

Fig. 12: PDP comparison of 16 bit MAC architectures

V. CONCLUSION

The proposed design of MAC unit for a Digital Signal Processor is found to be an optimized design in terms of power consumption and figure of merit. It is evident from the performance analysis that the 16 bit design showed an improvement of 11.29% in the power consumption and 6.18% in the figure of merit. The power efficient design can be utilized for many applications including biomedical devices like a digital hearing aid. In future work more focus may be applied to the high speed design part of the architecture.

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AUTHORS PROFILE

Rakesh S received B.Tech. degree in Electronics and Communication Engineering from Mahatma Gandhi University, Kottayam, Kerala, India in 2008. He obtained Masters in Engineering in VLSI Design from Anna University, Chennai, Tamil Nadu, India in 2013. He is currently a research scholar in Noorul Islam Centre for Higher Education, Thuckalay, Tamil Nadu, India. His research interests include Digital VLSI design, Low power VLSI design etc.

Dr. K. S. Vijula Grace received her B.E degree in Electronics and Communication Engineering from Madurai Kamraj University, Tamil Nadu, India in 1997. She obtained her Masters in Engineering in Power Electronics and Drives from Anna University, Chennai, Tamil Nadu, India in 2005. She received her Ph.D degree under the faculty of Information and Communication Technology from Anna University, Chennai, Tamil Nadu, India in 2015. Her research interests include Embedded systems, VLSI, Communication etc.