

Modeling of Nine Level Diode Clamped Multilevel Inverter Fed Induction Motor with front end Rectifier

A.Arther jain, T.Chandra sekar, B. Justus rabi, S.S. Darly

Abstract: A conventional Adjustable Speed Drive (ASD) with 2-level Pulse Width Modulation (PWM) inverters create high dv/dt and high-frequency common mode voltages which are destructive to the drive applications. It lessens the motor bearing life and directed Electro Magnetic Interference (EMI) decays the protection. The benefits of proposed AC-DC-AC system are minimal effort, little size, high productivity, and effortlessness. This paper introduces the nine level diode clamped multilevel inverter (DCMLI) fed induction motor . Hypothetical outcomes dependent on investigation are checked at first through PSIM reenactment and approved with a test model of 2.5kW.

Keywords: Diode clamped Multilevel Inverter, Induction motor, Front end Rectifier,

I. INTRODUCTION

In industry, ASD is utilized to control the speed of an induction motor with exactness up to 1% or above relying upon the control system. In all electric usage, 76% is utilized by the motor. 20% to 30% power utilization can be spared through ASD [17]. It has an improved system productivity, adaptability and hardware unwavering quality because of no moving parts. Presently, three-phase induction motor drives are works in various mechanical territories with a wide power go that can be started from a couple of 100W to several MW. The incredible advanced controllers are used in drives industry, which are responsible for the impression of control works inside minimal effort edges. ASD is more sensitive to their established mechanical system than the current environment system. The connection among ASD and its environment is in the two different ways: on the one side, the utilization of ASD conveys some unfriendly consequences for the earth as harmonics, untimely bearing disappointment, dielectric breakdown, clamor, vibration, etc. [12]. On the opposite side the impacts of the environment on the ASD that normally result in a glitch or a procedure shut down.

II. SYSTEM DESCRIPTION

The basic ASD structure for medium and low power equipment is an indirect converter [1]-[2].

Manuscript published on 30 June 2019.

* Correspondence Author (s)

A.Arther jain, Research scholar, Anna University, Chennai, Tamil Nadu
T.Chandrasekar, Associate professor , Shri Andal Algar College of Engineering , Mamandur, Tamil Nadu
B. Justus Rabi, Professor, Shri Andal Algar College of Engineering , Mamandur, Tamil Nadu
S.S. Darly .Assitant Professor, university college of Engineering, Tindivanam, Tamil Nadu

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license <http://creativecommons.org/licenses/by-nc-nd/4.0/>

IGBT-based power inverter is utilized which permits high switching frequency bringing about a high unique control of the present which is beyond the realm of imagination with lower switching frequency. Due to non-linear loads, harmonic currents and voltages are generated in the power distribution system [7]. If the sum of harmonic current increases above certain limits, harmonic distortion occurs and creates a type of pollution in the electric plant that can create problems.

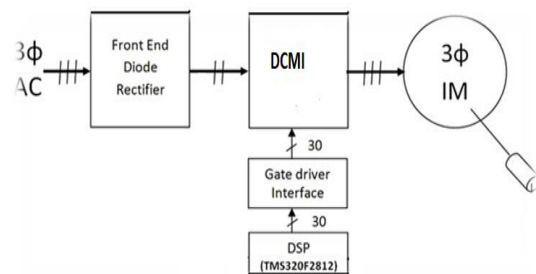


Fig 2.1 Multilevel inverter with front end rectifier

The nine-level diode clamped DC link inverter with front end rectifier is shown in Figure 2.1. DC link inverter is preferred for ASD application to produce desired voltage and frequencies from a constant AC input voltage. The circuit operation of six-pulse diode rectifier and MLI follows [13]-[14]. It has three legs. Each leg has two series connected diodes. Six diodes are divided into two groups. Upper groups, consisting of diodes are known as a positive group. It provides three pulses positive output at the point v_a . Lower group are known as the negative group. It provides three pulses negative output at the point v_b . The input voltages waveforms are exhibited in Figure 2.1. The phase voltages calculated by (2.1) and (2.2), two of the phase are associated with the load while one phase is detached in each point in time.

The THD of the input current is resolved to apply.

$$THD = \frac{\sqrt{I_{RMS}^2 - I_1^2}}{I_1} \quad (2.1)$$

$$THD = \frac{1}{3} \sqrt{\pi^2 - 9} = 31.08\% \quad (2.2)$$

The value of THD is viewed as high. The primary point of this work is to examination effective strategies to reduce the input current of THD in three-phase diode bridge rectifier. The NPC-MLI utilizes clamping diodes for level making and fell DC capacitors for keeping up DC-connect voltage.



Modeling of Nine Level Diode Clamped Multilevel Inverter Fed Induction Motor with front end Rectifier

The different parts of the 9-level NPC-MLI are examined, including the principle of working, inverter topology and commutation of device. In general, four cascaded DC capacitors split the DC input voltage of the inverter, by, giving a floating neutral point 'O' (NP).

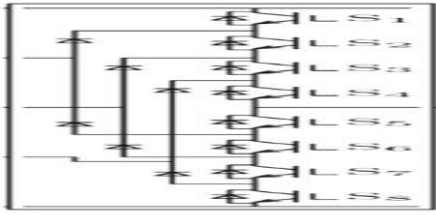


Fig 2.2 Phase A of Nine level DCMLI

Number of power electronic switches per/pole = $2(n - 1)$
 DC-link capacitors = $(n-1)$
 Number of clamping diodes per pole = $2(n - 2)$
 Voltage across each DC-link capacitor = $V_{dc}/(n-1)$
 Where, V_{dc} is the DC-link voltage, n is the level of the inverter. Fig(2.2) is showing that the simple diagram of a 9-level NPC-MLI. The leg "A" of an inverter is made out of four active switches S_1 to S_8 with the anti-parallel diodes. Practically, either the GCT or IGBT can be utilized as a switching device. On the inverter DC side, the DC-transport capacitor is part into four, giving a NP. The diodes associated with the neutral point, are the clamping diodes.

Table 2.1 Switching table for the 9-level NPC-MLI

Device switching Status of PhaseA				Inverter Terminal
$S_1 = S_5$	$S_2 = S_6$	$S_3 = S_7$	$S_4 = S_8$	Voltage (V_{AN})
1	1	1	1	$E_4 = V_{dc}$
0	1	1	1	$E_3 = 3V_{dc}/4$
0	0	1	1	$E_2 = V_{dc}/2$
0	0	0	1	$E_1 = V_{dc}/4$
0	0	0	0	$E_0 = 0$

It very well may be seen from Table 2.1 that switches S_{1A} and S_{3A} operate in a reciprocal way. With one is ON, the other must be OFF. Thus, S_{2A} and S_{4A} territory state pair too. The gate signal and switching state action, where vg_1 to vg_4 are the gate signals for S_{1A} to S_{4A} , individually. The gate signal can be produced by Space Vector Modulation (SVM), Carrier Based Pulse Width Modulation (CBPWM), or Selective Harmonic Elimination (SHE) schemes.

III. MODELING OF DCMLI FED INDUCTION MOTOR WITH FRONTEND RECTIFIER

The practical inverters waveforms are non-sinusoidal and contain higher magnitude harmonics with lower order. In the output of DC to AC inverters Harmonic are present in can be disposed of either by utilizing filter circuit or by utilizing PWM circuits. Utilization of filter has the inconveniences of bigger unit size, expanded the losses and subsequently the poor proficiency which results in greater expense for acknowledgment, though utilization of PWM systems lessens the channel prerequisites to least or zero, contingent on the kind of uses and the control method utilized for the age of terminating beats for the influence switches and relying on the sort of use. The harmonic can be

produced by either source or load side. Conventional two level high-frequency PWM inverters have a few issues related with high-frequency system, which delivers high dv/dt worry over the power switches [5]. While utilizing the specific control techniques to the MLI, the harmonics present in the output voltage are decreased essentially when contrasted with the ordinary high frequency PWM methods. Here the proposed SPWM strategy is used in PSIM, and the output waveforms were introduced for various levels. In the PSIM software, three phase Nine level diode clamped multilevel inverter fed induction motor (DCMLI) with front end rectifier is simulated .[17]. The sub-block consists of one arm of the nine level DCMLI, where all switches are connected in series with the parallel combination of clamping diodes. So the pulses generated for a positive arm is inverted and fed to the negative arm. PSIM induction motor simulation parameters fig 3.1.

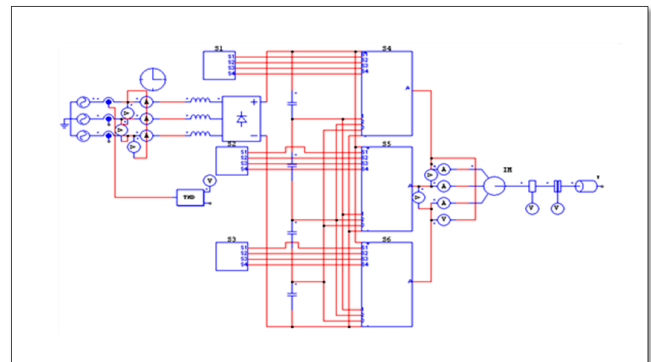


Fig 3.1 Simulation diagram for induction motor

Table 3.1 Induction motor simulation parameters

Parameters	Values
R_s (stator)	1.405
L_s (stator)	0.005839
R_r (rotor)	1.395
L_r (rotor)	0.005839
L_m (magnetizing)	0.1722
No of poles	4

The 415V, 50 Hz, AC is used to drive the motor through DC link inverter. The waveform shows per phase voltage waveform and phasor represent 120° displacement. Three phase supply voltage obtained from simulation.

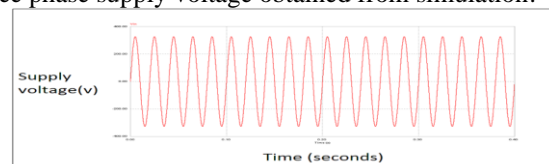


Fig 3.1 supply voltage 200v/div.Time:0.10s/div

A source current under front end rectifier operation. Front end rectifier used in many converter topologies to produce fixed DC output voltage from a fixed AC input voltage. The higher power handling capacity and reduced ripple

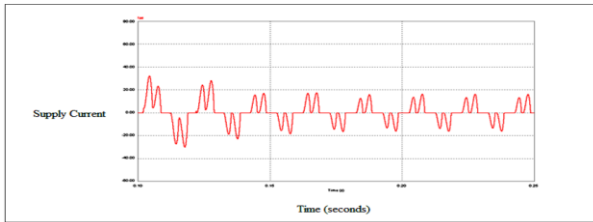


Fig 3.2 Source current 20A/div. Time: 0.15s/div

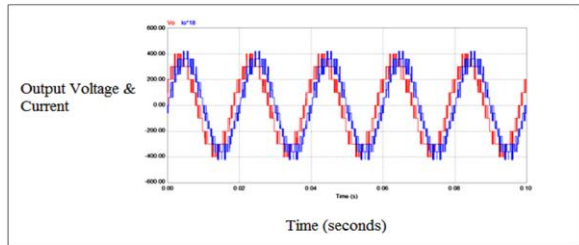


Fig 3.3 Output voltage and current V_o : 200V/div. I_o :200A/div(=18) Time:0.02s/div

The phase AC output voltage and current acquired from simulation are shown in Figure. 3.1. It demonstrates the output voltage, and current of nine level diode DCMI fed induction motor drive with active current injection is implemented with IGBTs switching elements and is examined with the three phase 440v squirrel cage induction motor . The nine levels produce THD about 9%. It is very low when compared with conventional two-level inverter used in adjustable speed drives. Figure 3.4 shows the value of supply current harmonics and p.f.

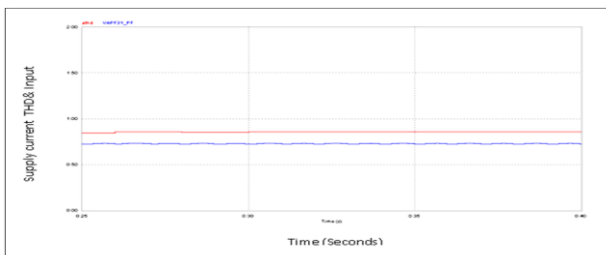


Fig.3.4 THD and PF;athd(THD): 0.2pu/div. $V_{APF31_PF}(PF)$:0.2pu/div. Time: 0.05s/div

Unity PF and 0% THD are desirable in DC link inverter. But the typical value of THD and PF of nine level DCMLI is around 85% and 0.73 respectively which is undesirable. It must be improved.

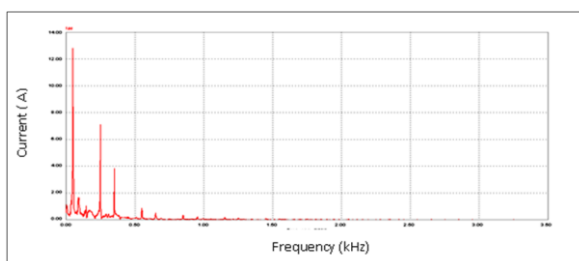


Fig 3.5 FFT spectrum 2.0A/div. Frequency: 0.5kHz/div

The Figure.3.5 gives the FFT spectrum of the supply current as obtained from simulation. It explains the order of harmonics. Waveform clearly shows that the presence of harmonic current. Especially odd order harmonics make an influence on the fundamental components.

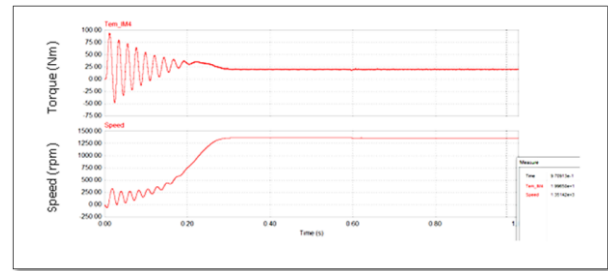


Fig 3.6 Torque and Speed at full load (Simulation) $T_{em_IM4}(Torque)$:25Nm/div. Speed: 250rpm/div

The mechanical characteristics of torque and speed of an induction motor obtained from simulation are shown in Fig3.6. The inverter fed induction motor has smooth speed – torque characteristics. The speed of an induction motor is around 1350 rpm, and it torque developed in the motor is 20 Nm. The torque pulsation is almost zero. The settling time of the given motor drive is about 0.28 sec.

IV. EXPERIMENTAL RESULTS

The power unit constructed with power processing unit and input supply unit. To confirm the performance of the simulated system, the nine-level DCMI fed induction motor drive is implemented with IGBTs as switching elements and is examined with the three phase 440 Volt squirrel cage induction motor coupled loading arrangements. In present day electric drives, elite control is required, which can be effectively accomplished utilizing progressed advanced processors. The components are chosen for the test model and specialized parameters of the AC motor is recorded in Table 4.1 An investigation of the AC-DC-AC converter is carried out in detail and dependent on the design, and test model of 2.5kW and output voltage of 540V is created. IGBT module IRGB4059D is utilized for HF inverter. The RHRP 30120 diodes are used in Front-end rectifier. The digital signal processor (TMS320F 2812) is used to create required gate pulses. The superior bipolar gate driver is worked by utilizing MOSFETs (IRF 510 and IRF 9510) with high speed. This has guaranteed better execution by staying away from false activating of the IGBTs amid their off state.

Table 4.1 Technical parameters of the AC motor

Parameters	Values	Parameters	Values
Rated Power	2.5Kw	Duty Cycle	S1
Rated Voltage	415V	No. of Poles	4
Rated Current	6A	Motor Type	Induction Motor



Modeling of Nine Level Diode Clamped Multilevel Inverter Fed Induction Motor with front end Rectifier

Rated Frequency	50Hz	Connection	Star
Rated Speed	1400RPM	No. of phases	Three Phase
R_s	3.69 Ω	L_s	0.26H

$L_s = 0.5mH$, $C_a = 1F$, $L_a = 290H$, $C_o = 50F$

In order to perform experimental work, various components such as Three phase rectifier module, Hall effect current sensor module, Three phase Nine level inverter, Three phase 3 HP induction motor and DSO are arranged to get results. The experimental arrangement is shown Fig 4.1

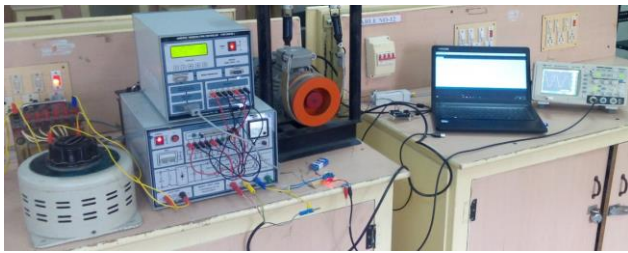


Fig 4.1 Experimental setup

For investigations a digital storage oscilloscope is used. To approve the hypothetical outcomes, a low power, three-stage, DCMLI model is developed. The inverter uses IRGB4059D (600V,8A) MOSFET as the switching devices. The reconfigurable MOSFET switches configured as the proposed Nine level diode clamped inverter with the current injection network. It uses IC PC817 in the interface circuit. The gate control signals are created by a separate unit, which is actualized on DSP processor TMS320F2812. For interfacing, an Atmel 8-bit AVR RISC microcontroller (ATmega16 L) is considered with the administrator and gives the changing occasions to DSP. The experiment is carried out to monitor the input voltage and current of three phase diode rectifier and the output voltage and current of DCMLI with and without current injection. Per phase readings of supply voltage and current.

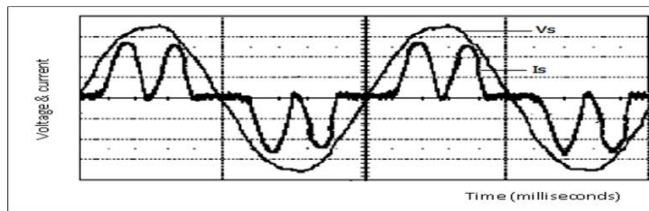


Fig5.1 Supply voltage (100V/div) and current (5A/div); x axis: 10ms/div

The supply voltage and current of phase A, from examination is appeared in Fig.5.1. It demonstrates the contorted information current.

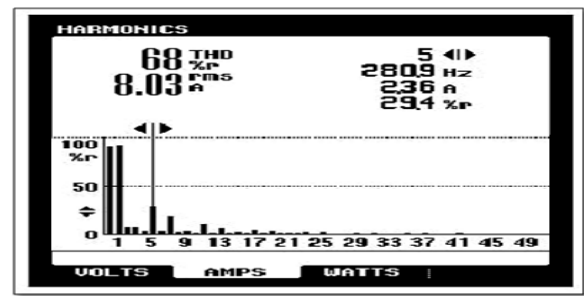


Fig 5.2 Input current harmonic spectrum scale: the input current, scale: Y axis 2A/div: X axis: 100 Hz/div

The FFT spectrum of the supply current without compensation is obtained from experiment is shown in Figure. 5.2

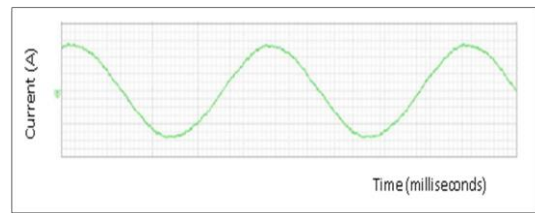


Fig 5.3 Multilevel Inverter per phase output current 5/div; Time 5ms/div

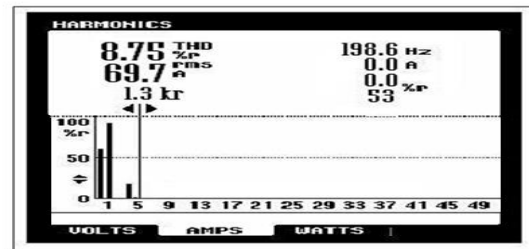


Fig 5.4 Output current harmonic spectrum, scale: output current, scale: Y hub 0.2pu/div: X hub: 200 Hz/div

The FFT spectrum of the output current is obtained from experiment is shown in Figure. 5.4. From the experiment, the observed parameters are tabulated in Table 5.1 and compared in graph.

The comparison between simulation and experiment result are compensation technique is Nine level inverter the output result of total harmonic distortion(THD) simulation result is 85% and the experimental result in total harmonic distortion is 68% then the power factor value is 0.8.

V. CONCLUSION

The detailed review was done on nine level MLI fed induction motor drive with a front-end rectifier. The performance was analyzed using PSIM simulation software. Various results are obtained, in which the value of THD and PF is 85% and 0.73 (lagging) respectively. The values fail to come to IEEE standards. Simulation results of MLI shows enhanced the harmonic profile of output voltage waveform. It is about 9%. The high-quality voltage used to drive the induction motor. It results in good torque-speed characteristics of the induction motor.

REFERENCES

1. J. Rodriguez, et., al., (2007) "Multilevel voltage-source- converter topologies for industrial medium-voltage drives", IEEE Trans. Ind. Electron. 54 (6) 2930-2945.
2. B.K. Bose, "Power electronics and motor drives recent progress and perspectives", IEEE Trans. on Ind. Electronics vol. 56 (2) (2009) pp581-588.
3. N. Vázquez, et., al., (2009) "Three-phase rectifier with active current injection and high efficiency", IEEE Trans. On Ind. Vol 56 (1) 110-118.
4. N. Mohan et., al., (1993), "Analysis of a new power electronics interface with approximately sinusoidal 3-phase utility currents and a regulated dc output", IEEE Tran on Power Delivery 8 (2) 540-546.
5. J.W. Kolar, et., pp (1999), "VIENNA rectifier II—A novel single-stage high-frequency isolated three-phase PWM rectifier system", IEEE Trans. Ind. Electron. Vol 46 (4) pp 674-691.
6. M. Malinowski, M. Jasinski, M. Kazmierkowski, "Simple direct power control of three-phase PWM rectifier using space-vector modulation", IEEE Trans. Ind. Vol-51 (2) (2004) pg 447-454.
7. D. Alexa, et., al., (2004) "An analysis of three-phase rectifiers with near-sinusoidal input currents", IEEE Trans. Ind. vol 51 (4) pg 884-891.
8. G. Chen, K. Smedley, "Steady-state and dynamic study of one cycle-controlled three-phase power-factor correction", IEEE Trans. Ind. Electron. Vol. 52 (2) pg 355-362 (2005).
9. D. Alexa, A. Sirbu, A. Lazar, "Three-phase rectifier with near sinusoidal input currents and capacitors connected on the AC side", IEEE Trans. Ind. Pg 1612-1620 vol 52 (2) (2009).
10. G.A. Dhokane, H.M. Suryawanshi, "Harmonics elimination in three-phase AC system using current injection technique for AC-to-DC converter", Electric Power System Research Journal .Vol.79 (10) (2009) 1374-1383.
11. G.A. Dhokane, H.M. Suryawanshi, "Power quality enhancement of three-phase front-end rectifier of UPS system using current injection technique", EPQU Journal ,Vol.24 (2) (2008) 35-40.
12. S. Hansen, et., al., (1996) "An integrated single switch approach to improve harmonic performance of standard PWM adjustable-speed drive", IEEE Trans. Ind. vol(4) pg 1189-1196 .
13. W.B. Lawrance, W. Milczarski, "Harmonic current reduction in a three-phase diode rectifier", IEEE Trans. Ind. Electron., Vol. 36 (1992) 571-576.
14. S. Kim, et., al., (1999) "A new approach to improve power factor and reduce harmonics in a three-phase diode rectifier type utility interface", IEEE Trans. Ind. Appl. 30 (6) pg 1557-1563.
15. A.R. Prasad, P.D. Ziogas, "An active power factor correction technique for three-phase diode rectifiers", in: IEEE Power Electronics Specialists Conference, Milwaukee, 1989, pp. 58-66.
16. Chandrasekar, T. and Rabi, B. Justus, "A study and review of current injection techniques", International Journal of Technology and Engineering Science, 2013, pp.1008-1003.
17. Chandrasekar, T. and Rabi, B. Justus, "Harmonics Reduction in Three Phase System Using Current Injection Technique for Adjustable Speed Drive", Australian Journal of Basic and Applied Sciences, 2014, pg.132-137.