Design, Implementation and Verification of Image Compression in High Speed DWT Algorithm for VLSI Applications

M.K. Deepa, Amay Shiva Naik, Rashmi Priyadarshini

Abstract--- The proposed DWT architecture for Image Compression targets the high-Speed processing improvement of DWT algorithm as compared to the existing architectures. It mainly includes line buffers, PIPO and lifting blocks. The methodology of using lifting scheme was to make architecture in a non-separable fashion and also to compute DWT algorithm at different resolutions. The RTL design will be coded via Verilog & synthesized using Xilinx ISE and vivardo tools, targeted on Spartan-6. The proposed architecture is scalable which can be parameterized for any size N(32,64,128,…..512). By the performance observation in the proposed architecture in terms of operating frequency for 128X128 image is 322.316 MHz implemented on spartan6 (xc6vhx565t-2ff1923) of FPGA board whereas it was seen in other architectures the maximum operating frequency was 254 MHz

Keywords--- Proposed Architecture for DWT Algorithm, 2-D Image Compression, Verilog, QuestaSim, Xilinx ISE.

1. INTRODUCTION

The concept of transfer speed plays a vital role in data transmission which justify the need for compression for its improvement which in turn means to reduce the bandwidth of the data.

Among the all the transforms it is seen that DWT gives best results for image compression due to its multi-resolution feature i.e. frequency & time both domains can be included simultaneously.

The deriving of filter bank coefficients for the DWT algorithm can be performed in two ways.

One way is the old convolution methodology and the other is lifting scheme.

The proposed architecture is mainly targeting the speed improvement thus going for the lifting scheme methodology as it involves acceleration as well reduction of computational calculations required for the algorithm.

The proposed algorithm gives operating frequency of 322.316 MHz which is implemented on spartan6 (xc6vhx565t-2ff1923) of FPGA board which in turn shows the improvement as compared to previously proposed architectures.

The following figure 1 shows the results of different architectures implanted for similar application.

References	Architecture Content
Sugreev Kaur and Rajesh Mehra, "High Speed and Area Efficient 2D DWT Processor based Image Compression", Signal & Image Processing: An International Journal (SIPU)	Sugreev Kaur et al, proposed pipelined partially serial architecture to enhance the speed along with optimal utilization and resources available on target FPGA. This design can operate at **maximum frequency 231 MHz** in Spartan 3 FPGA by consuming power of 117mW at 28 degree/c junction temperature
Naseer M, Basheer and Mustafa Mushtak Mohammed, "Design and FPGA Implementation of a Lifting Scheme 2D DWT Architecture", International Journal of Recent Technology and Engineering (IJRTE)	Naseer et al , proposed architecture based on lifting scheme approach, using the (5/3) wavelet filter, which reduces the hardware complexity and size of the on-chip memory. This architecture consists of a control unit, a processor unit, two on-chip internal memories to speed up system operations, and an on- board off-chip external memory (Intel strata parallel NOR flash PROM). It operates at **maximum speed of 62.767 MHz** on Spartan 3E FPGA
Li Bao Feng, Dou Yong and ShaoQiang, "Deeply Parallel Architecture for Lifting based 2D DWT in JPEG 2000", The Sixth IEEE InternationalConference on Computer and Information Technology	Li Bao-Feng et al, proposed a parallel architecture for 2D DWT with two rows and two columns processors. It takes 3N+2 buffers to store intermediate data and operates at **maximum of 145.54MHz** on Altera Stratix II FPGA.

Figure 1: Previously Proposed Architectures

2. PROPOSEDARCHITECTURE

In the VLSI domain the ability of signal analysis decides the popularity of the tool, the DWT has already made the mark about its effectiveness.

The efficiency of the design is completely dependent upon the deciding of filter coefficients. The filter implementation is done via poly-phase structure using distributive arithmetic (DA) technique.

The LUT architecture in turn implements DA. The RTL design was targeted on to Xilinx Spartan3A and Spartan6 DSP.

Revised Version Manuscript Received on 14 February, 2019.

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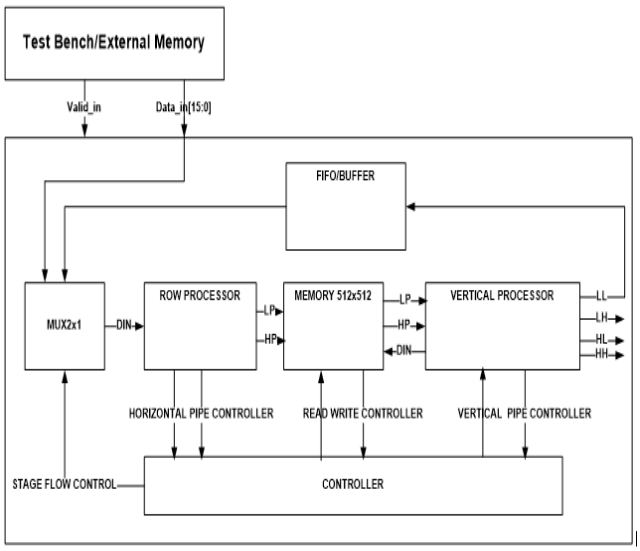

Figure 2: DWT Proposed architecture

Wavelet Transforms on images

Input image for compression: 512x512 grayscale image

If we look at the architecture figure the image is itself taken in the form of input data. An image in terms of numbers is the log file which is in turn acts as the datain. Both the processor has built-in filters one high pass and the other is low pass. The filters will generate outputs based on the frequency selection on their ends. The outputs from the row processor is forwarded to the vertical processor which also consist of both filters low pass and high pass who generate four outputs namely low-pass-low-pass, low-pass-high-pass, high-pass-low-pass & high-pass-high-pass. The aim of compressing the data lend us the concept to only take low-pass-low-pass output end for consideration. The output ends from vertical justify the first level of decomposition which is shown in figure 3.

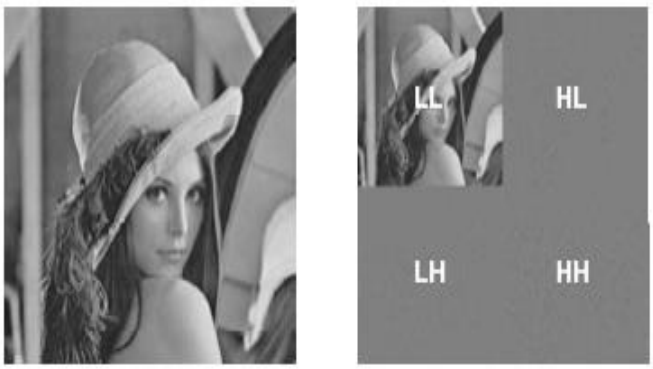

Figure 3: Base Image and its first level Decomposition

Top Level Architecture of DWT

Memory block

The whole scenario is being expertise by the controller from the beginning of the data in to the output ends. The intermediate output end generated by the row processor requires some amount of memory storage, thus a dual port ram block is taken to serve that purpose. The memory block is divided in two halves to store even and odd samples which are generated via address manipulation. Read & write operation are driven via controller.

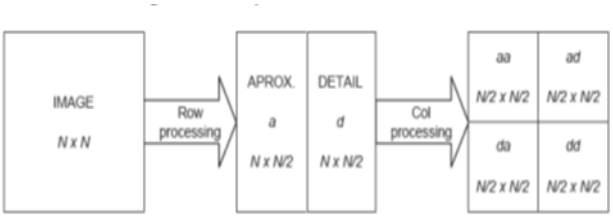

Figure 4: Image Decomposition Architecture

Poly phase structure of the input sample

By using poly-phase structure we intend to improve the efficiency i.e. by utilizing parallelism. In the end we need to split input samples into odd & even which can be realized as per the derived odd &even coefficients of the filter. Below figure illustrates poly-phase structure.

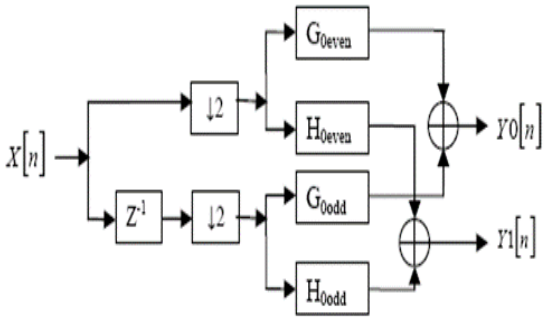

Figure 5: Poly-Phase decomposition structure

Choosing the effective coefficients will improve the DWT design. We use the filter design tool for deriving the coefficients values, since the values are in decimals, we need to use either floating point or fixed point to covert them into data which can be simulated i.e. in binary, hexa- decimal format etc. By comparison floating point is slower because of its complexity & hardware requirements thus we use fixed point instead. Fixed point is just multiplying 2^N where n is fixed by the user and the decimals are converted into needed data same at the receiving end previous values can be retrieved back. Below figures shows some filter coefficients derived by the tool.

Low Pass Filters				High Pass Filters			
Taps	Even phase G_{0even}	Taps	Odd phase G_{0odd}	Taps	Even phase H_{0even}	Taps	Odd phase H_{0odd}
4	0.60294	3.5	0.26686	2.4	1.11150	3	-0.59127
2.6	-0.07822	1.7	-0.01686	0.6	-0.05754	1.5	0.09127
0.8	0.02674						

Figure 6: Filter coefficient table

Micro architecture of DA

Adder Tree Implementation of DA

Computations are inherently bit-serial. For a B-bit input, it takes B clock cycles to cipher one output. Thus, this serial distributed arithmetic (SDA) filter encompasses a low output. The speed will be inflated by partitioning the input words into smaller words and process them in parallel.

Because the similarity will increase, the output will increase proportionately, and then will the quantity of LUTs needed.

Filters are often designed specified many bits of the input are processed during a clock amount. Partitioning the input word into M sub-words needs M-times as several memory LUTs and this will increase the storage necessities. But currently a brand-new output is computed each B/M clock cycles rather than every B cycle. a completely parallel district attorney (PDA) filter is achieved by factorization the input into single bit sub-words that achieves most speed. a brand-new output is computed each clock cycle. This methodology provides exceptionally superior, however comes at the expense of multiplied FPGA resources. Figure nine shows a parallel district attorney design for Associate in Nursing N-tap filter with 4-bit inputs.

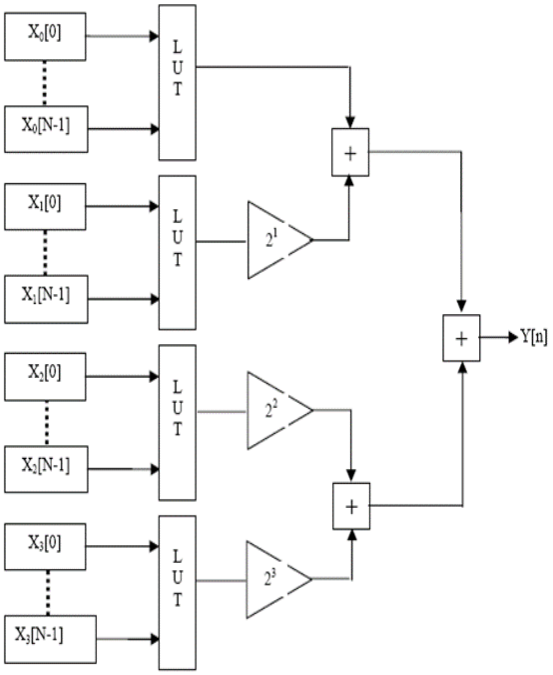

Figure 9: Adder Tree and parallel Implementation of DA

Row& Column processing Structure

The processing unit consist of two blocks mainly to store high-pass & low-pass samples separately, the coefficients linked within the filters are even & odd values which help in distinguishing odd & even output ends at the processing unit. The memory storage is for the storing row output ends so that it can be passed on later, the whole methodology is directed by the controller. The row unit generate two output ends. After the row processing its output ends are passed to the column processing unit which also comprises of similar structure as row processing unit. The column unit generates four outputs end among which low-pass-low-pass is preferred output for decomposition. Together completion from row to column unit will signify first level of decomposition. Figure 10 & 11 shows the architecture of row & column unit resp.

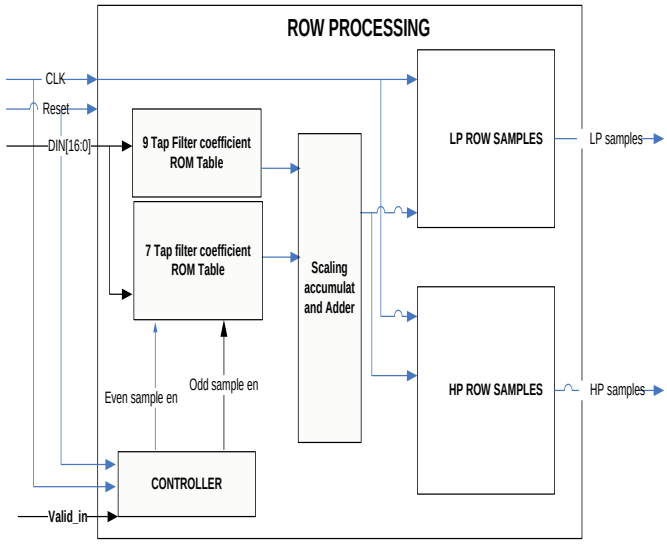

Figure 10: Micro-architecture of row processing

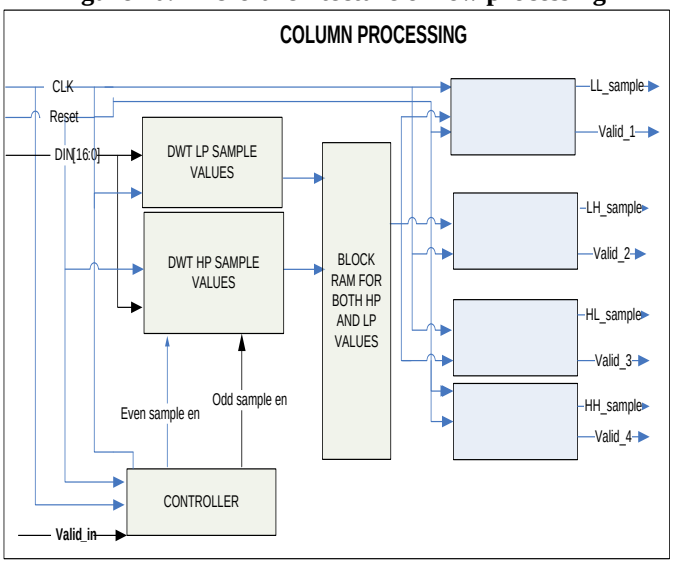

Figure 11: Column processing unit

Pin Description of Top Module

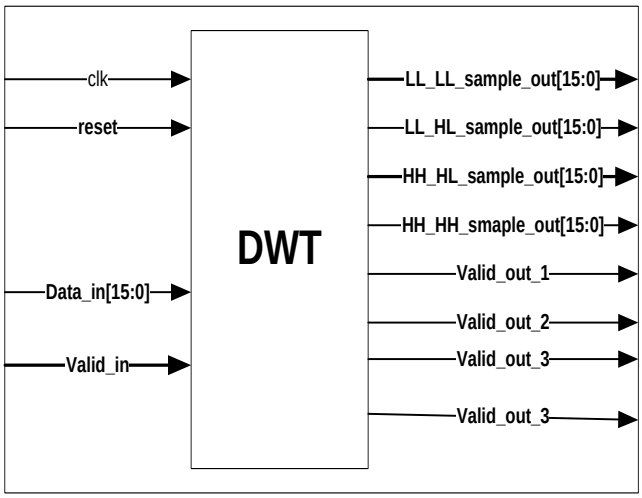

Figure 1: Pin Diagram of Top Module

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RESULTS AND DISCUSSIONS

Simulation Wave Form of Filtered Values

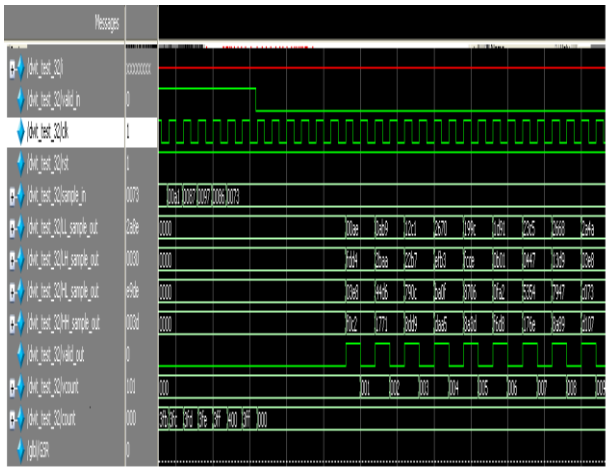

Figure 2: Simulation Wave form of DWT Top Module

RTL simulated values Imported and plotted in MATLAB

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1091	70480	0%
Number of Slice LUTs	2737	35240	0%
Number of fully used LUT-FF pairs	914	2914	31%
Number of bonded IOBs	84	720	11%
Number of Block RAM/FIFO	8	912	0%
Number of BUFG/BUFGCTRL/BUFHCEs	1	248	0%

Fig. 14: Device utilization summary for 128x128

The proposed architecture is synthesized on Xilinx FPGA target device using spartan6 (xc6vhx565t-2ff1923).The Modelsim simulation results and MATLAB validation plots are shown above figure 13. A separate Matlab verification code is written enabling it to read image and covert the image pixel to a text-based log-file which is feed into the testbench for the Verilog codeand alsoto read the Verilog output to display the compressed image results. display the images.

3. CONCLUSION

The Code developed for the proposed DWT design was a parameterized one which supports 32x32, 64x64, 128x128, 256x256, 512x512 and it can be scaled even higher, the synthesis was carried out on Xilinx ISE which resulted an operating maximum frequency of 322.316MHz for 128x128 image and 297.60Mhz for a 512x512 image which is the improvement over the previously obtained results as shown in the reference table of figure 1.

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