Energy Efficient Instruction Register for Green Communication

Shah Md Tanvir Siddiquee, Keshav Kumar, Bishwajeet Pandey, Abhishek Kumar

Abstract - Our work represents the interfacing of instruction register with FPGA. In this work we have taken three different FPGA of Virtex family that are Virtex 4, Virtex 5 and Virtex 6 and have observed the power variation of instruction register with this three FPGA. This experiment is done on a Xilinx 14.1 ISE design suite. And the power of instruction register with three FPGA is analyzed with an X Power tool. All the other chips power which is implanted on instruction register counts zero in total, dynamic and quiescent power consumption. In this experiment, only one LUT flip flop pair is used. On comparing the power of instruction register with the three FPGA of Virtex family, we concluded that 90 nm Virtex-4 FPGA requires the least power among all the three FPGA..

Keywords— Instruction register, FPGA, Virtex-4, Virtex-5, Virtex-6, Power analysis.

1. INTRODUCTION

Greenhouse gases are getting dangerous day by day for the world's population. Not only that these gases plays a drastic role in the disturbance of green communication. As we know green communication is the need of future generations. To fulfil the demands of our future generation we must have to ensure that we should develop such devices that will consume low power as much as possible [1-2]. Instruction register is the part of Central Processing Unit (CPU) which is used to hold the data instruction and also execute the data which is sent to the CPU from the sender end [3]. As for green communication it is necessary that this instruction register should consume least amount of power for operation. In our work we have tried to do the same by interfacing the instruction register with three FPGA of Virtex family. The RTL schematic and detailed RTL schematic of instruction register is shown in Fig. 1 and 2. And the technology schematic is shown in Fig. 3 respectively. In the interfacing of instruction register, number of slice LUTs used is one, number of fully used LUT-FF pairs is zero, number of bonded IOBs is five and number of BUFGs is one. Fig. 4 shows how instruction register executes data within CPU.

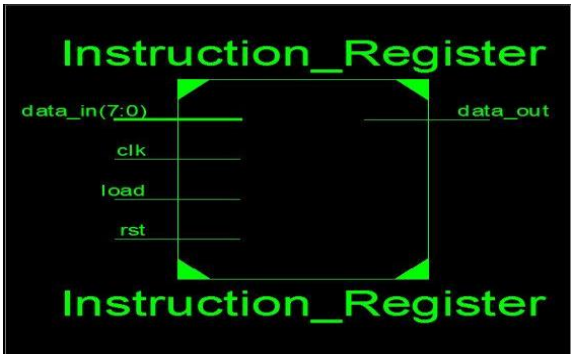

Figure 1. RTL Schematic of Instruction register

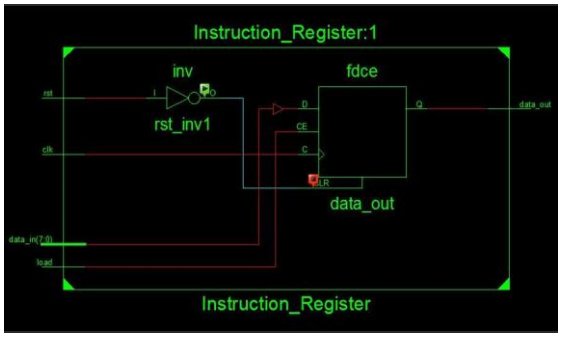

Figure 2. Detailed RTL Schematic of Instruction register

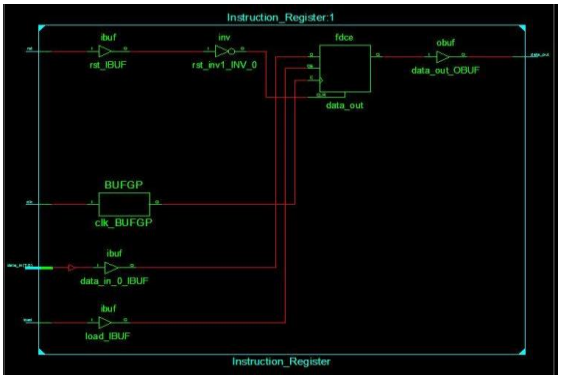

Figure 3. Technology Schematic of Instruction register

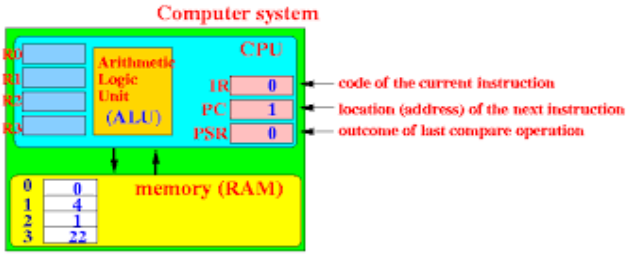

Figure 4. Execution of data by instruction register

Revised Manuscript Received on December 22, 2018.

Shah Md Tanvir Siddiquee, Daffodil International University, Bangladesh.(E-Mail: tanvir.cse@diu.edu.bd)

Keshav Kumar, Chitkara University Institute of Engineering and Technology, Chitkara University, Punjab, India (E-Mail: keshav.kumar@chitkara.edu.in)

Bishwajeet Pandey, Center of Energy Excellence, Gyancity Research Lab, Motihari, India.(E-Mail: gyancity@gyancity.com)

Abhishek Kumar, Center of Energy Excellence, Gyancity Research Lab, Motihari, India.(E-Mail: abhishek@gyancity.com)

2. RELATED WORK

M. I. Heywood et. al. [4] proposed an idea regarding register based genetic programming FPGAs. With the use of FPGA authors have tried to implement linearly structure genetic program. S. M. Trimberger in [5] have tried to work on designing a microprocessor which can be reprogrammed. Author has used FPGA, which can make the use of internal buses for execution of instruction data. M. J. Wirthlin et. al. [6] developed a DISC (Dynamic Instruction Set Computers) to back up demand driven set modification. Authors used FPGA for executing DISC instructions. M. B. Gokhale et. al. [7] implemented RISC FPGA implementation. This work allows programmer to control over the mapping of data and to correlate between conventional processor and configurable logic. B. Pandey et. al. [8] designed a FIR filter using FPGA for green communication. Authors used Kintex ultra scale FPGA to study the power consumption of FIR filter by changing its IO standards. R. Sharma et. al. [9] focused on a solution to find an operating condition for RAM so that it consumes the least amount of power. The different frequencies at which this experiment is performed lies in the range of 0.6 GHz to 1.5 GHz on Xilinx 12.1 simulator. K. Kalia et. al. [10] designed a power efficient RAM using 28nm FPGA for spacecraft. In this work authors work on IO standards of FPGA to study the power consumption of RAM.

3. EXPERIMENTAL SECTION

We have used the Xilinx 14.1 ISE design suit to interface the instruction register with FPGA. The power deviation with three FPGA of Virtex family is analysed using X Power analyser tool. The code of instruction register is written in Verilog hardware description language.

4. POWER ANALYSIS & RESULTS

In this work we are observing the dynamic power, quiescent power and total power variation of Virtex 4, Virtex 5 and Virtex 6 FPGA.

A. Power analysis of Virtex 4 FPGA

The dynamic power, quiescent power and total power consumed by Virtex 4 FPGA are 0.004W, 0.166W and 0.171W respectively. The power table of Virtex 4 FPGA is shown in table 1. Signal, IOs power are zero for Virtex 4 FPGA and the clock power is same as dynamic power that is 0.004W.

Table 1. Power Analysis of Virtex 4 FPGA

On chips power	Power in Watts (W)
Dynamic Power	0.004
Quiescent Power	0.166
Total Power	0.171

B. Power analysis of Virtex 5 FPGA

In case of Virtex 5 FPGA, dynamic power consumption is zero (0.000W). Total power is same as quiescent power that is 0.321W. The power chart of Virtex 5 FPGA is shown in table 2. All the other on chips power which are fabricated on instruction register are zero.

Table 2. Power Analysis of Virtex 5 FPGA

On chips power	Power in Watts (W)
Dynamic Power	0.000
Quiescent Power	0.321
Total Power	0.321

C. Power analysis of Virtex 6 FPGA

Table 3. Represents the power analysis of Virtex 6 FPGA. For Virtex 6 FPGA total power and quiescent power are same as 1.293W and the dynamic power consumption is 0.000W. Signal, IOs, clock power are zero for Virtex 6 FPGA.

Table 3. Power Analysis of Virtex 6 FPGA.

On chips power	Power in Watts (W)
Dynamic Power	0.000
Quiescent Power	1.293
Total Power	1.293

D. Power analysis of Virtex 4 FPGA v/s Virtex 5 FPGA v/s Virtex 6 FPGA

On comparing all the three Virtex 4 FPGA, Virtex 5 FPGA and Virtex 6 FPGA, we observed that Virtex 5 and Virtex 6 FPGA consumes 0.000 W of power and Virtex 4 FPGA consumes 0.004 W power. For the quiescent power and total power, Virtex 4 FPGA utilizes the least amount of power among Virtex 5 and Virtex 6 FPGA. The power comparison of three FPGA is shown in figure 5.

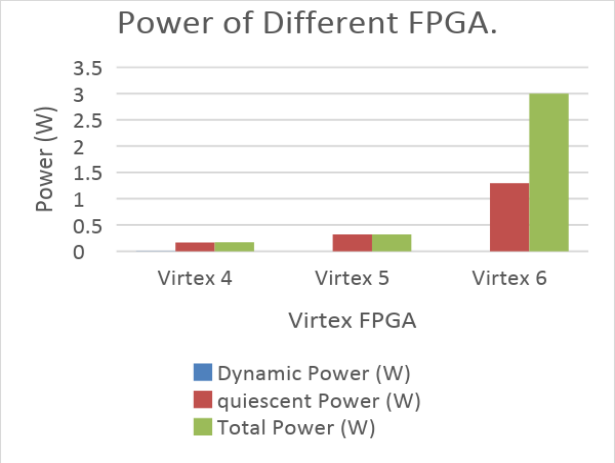

Figure 5. Power of Different FPGAs

5. CONCLUSION

In our work, we have interfaced the instruction register with three FPGA of Virtex family that are Virtex 4, Virtex 5 and Virtex 6 FPGA and observed the power variation of instruction register on FPGA. We came to conclusion that Virtex 4 FPGA is the most power efficient device among the group. The percentage variation of total power of Virtex 4 FPGA from Virtex 5 and Virtex 6 FPGA are 46.728% and 86.77% respectively. The power analysing process is done on X power analyser tool in Xilinx ISE Design Suit. The module in which the code of instruction register is written is Verilog HDL (Hardware Description Language).

6. FUTURE SCOPE

In this work we have interfaced the instruction register with Virtex 4, Virtex 5 and Virtex 6 FPGA. Not only these three FPGAs but we can implement the instruction register with Spartan, Kintex, Airtex, and Cyclone FPGAs also and can analyse the power consumption with these FPGAs. We can also implement other register and other electronics design with FPGA that can help in promoting green communication.

REFERENCES

1. D. Nandy, "Energy Crisis of India: In Search of New Alternatives", Journal of Business & Financial Affairs, 5:224. doi: 10.4172/2167-0234.1000224, 2016
2. Yongpeng Wu, Fuhui Zhou, Zan Li, Shunqing Zhang, Zheng Chu, and Wolfgang H. Gerstacker, "Green Communication and Networking", Wireless Communications and Mobile Computing, Volume 2018, www.hindawi.com/journals/wcmc/2018/1921353/
3. Instruction register, https://en.wikipedia.org/wiki/Instruction_register, Last Accessed on 9th April 2019
4. M. I. Heywood, and A. N. Z. Heywood. "Register based genetic programming on FPGA computing platforms." In European Conference on Genetic Programming, pp. 44-59. Springer, Berlin, Heidelberg, 2000.
5. S. M. Trimberger "Reprogrammable instruction set accelerator." U.S. Patent 5,737,631, issued April 7, 1998.
6. M. J. Wirthlin, and B. L. Hutchings. "DISC: The dynamic instruction set computer." In Field Programmable Gate Arrays (FPGAs) for Fast Board Development and Reconfigurable Computing, vol. 2607, pp. 92-104. International Society for Optics and Photonics, 1995.
7. M. B. Gokhale, J. M. Stone, and E. Gomersall. "Co-synthesis to a hybrid RISC/FPGA architecture." In Field-Programmable Custom Computing Technology: Architectures, Tools, and Applications, pp. 39-54. Springer, Boston, MA, 2000.
8. B. Pandey, N. Pandey, A. Kaur, D.M. A. Hussain, B. Das, and G. S. Tomar. "Scaling of Output Load in Energy Efficient FIR Filter for Green Communication on Ultra-Scale FPGA." Wireless Personal Communications (2018): 1-14.
9. R. Sharma, B. Pandey, and V. Sharma. "Analysis of frequency effect on variegated RAM styles and other parameters using 40 nm FPGA." In To Be Send To a Conference. 2018.
10. K. Kalia, B. Pandey, and D. M. A. Hussain. "SSTL based thermal and power efficient RAM design on 28nm FPGA for spacecraft." In 2016 International Conference on Smart Grid and Clean Energy Technologies (ICSGCE), pp. 313-317. IEEE, 2016

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication