Implementation of CMOS SRAM Cells in 7, 8, 10 and12-Transistor Topologies and their Performance Comparison

T. Santosh Kumar, Suman Lata Tripathi

ABSTRACT--- Memory is the important part of most of the electronic systems but the major problem with the design of memories is performance of devices i.e. speed and power dissipation. In this paper performance for read, write operations of SRAM cells based on different configurations are compared, specifically in each cell design the static-noise-margin (SNM) is calculated by observing butterfly characteristic curves. According to the result analysis the 7T SRAM cell in 45nm CMOS technology has less power dissipation and power delay product since it uses single bit for both read and write operations. The total circuitry is designed and simulated by using Cadence virtuoso and spectre respectively.

Keywords: CMOS, Power Product Delay, SRAM, SNM.

1. INTRODUCTION

Usage of SRAM based cache memories has increased over years for portable devices, mobile phones and all kinds of multimedia devices to attain high speed. Low power and high speed performance is the major puzzling task for Integrated circuit design in Nano scale technologies as VLSI chips are in demand in mobile communications and computing Devices. Since there is a wide spread use of battery powered smart devices, Nano medical devices, low power process has turned out to be a serious problem with system on chip design (SOC).In order to analyze an SOC we can consider a low power SRAM because it occupies the major portion of area in the SoC, it really disturbs the over-all power of SOC. Depending on how frequently we access the SRAM cell the power consumption varies largely. If we use a SRAM cell at high frequencies it consumes much power but at the same time if we use it at a slower speed in applications with moderately clocked microprocessors it consumes almost negligible power. There are many techniques for managing power in SRAM based memory structures. The adverse effect of variations in the threshold voltage (Vth) becomes substantial at low operating voltages as SRAM cell is vastly susceptible to the differences in Vth. For a low power procedure in a conservative 6T SRAM cell a lot of adjustment is required between READ and WRITE operations to obtain required stability.

In this paper diverse SRAM cell Formations (6T, 7T, 8T, and 9T) are conferred in Part 2. Part 3 provides performance assessment in terms of Speed and power dissipation for the designed SRAM structures. And the conclusion is provided in section 4.

2. SRAM CELL DESIGN

A. 7T, 8T, 10T, 12T Cell Design

From the figure 1 we can observe that the 7T SRAM-cell schematic which is utmost usually used SRAM cell structure. It has a stumpy fixed power indulgence. However, There is a problem existing with this SRAM- cell structure, ie., lack of potential stability. During the read operation at a node V1 of NMOS (N1) touches the beginning voltage(Vth) of NMOS N2, it will be turned on and pull down the voltage at node V2 to “0” this results PMOS (P1) is turned on and pull up the voltage ant node V1 due to positive feedback mechanism.

A new architecture of an 8T SRAM implementation was suggested [1], to decrease problem during the read operation, for which the data retaining component and the data output component should separate by using separate read/write bit and read/write word gesture lines. In turn, the cell employment offers a read-interrupt-free operation. However, this implementation uses eight transistors, which results in a cell area increase of 30% in contrast to the conservative 7T-cell design.

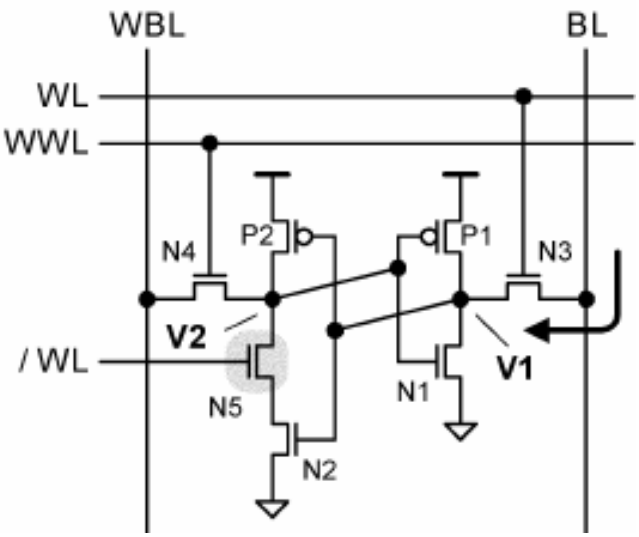

Fig1:7T SRAM schematic

Revised Manuscript Received on December 22, 2018.

T. Santosh Kumar, Assistant Professor, Dept. Of ECE, CMR Institute of Technology, Hyderabad, Telangana, INDIA.

Dr. Suman Lata Tripathi Associate Professor, Dept. Of ECE, Lovely professional University, Punjab, INDIA.

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

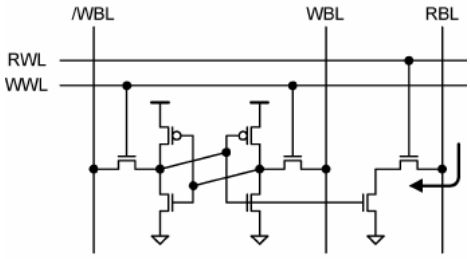

Fig2:8T SRAM -Cell schematic

The 7T cell design [2] also employs dispersed read and write signal lines but uses only one extra NMOS transistor to achieve read-disturb-free operation, thus increasing the cell area by 13%. NMOS transistor, whose gate is controlled by signal WL, is additional between node V2 and NMOS transistor, to the 7T-cell design as seen in Fig. 1.

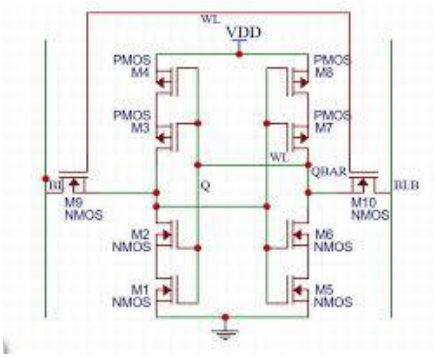

Fig3:10T SRAM -Cell schematic

Whereas the cell is being accessed, WL is set to "0" to turn off NMOS transistor. In the case of a "0" read, even if the voltage at node V1 reaches the Vth of NMOS transistor N2, node V2 cannot be pulled down to "0" and thus preserving the stored data. During data retention period, WL is set to "1", and the cell operates in the similar process as the 6T-cell circuit.

A 10T SRAM cell in figure3 has a read buffer on each side to improve the read performance and also write buffer on each side to progress the write performance apart from that it has six main body transistors which make its functionality similar to that of a 6T SRAM cell.

Further to improve the steadiness of the SRAM device a 12T transistor SRAM is proposed as shown in figure4 with one transistor on the top and the other in the bottom connected to Vdd and Gnd respectively.

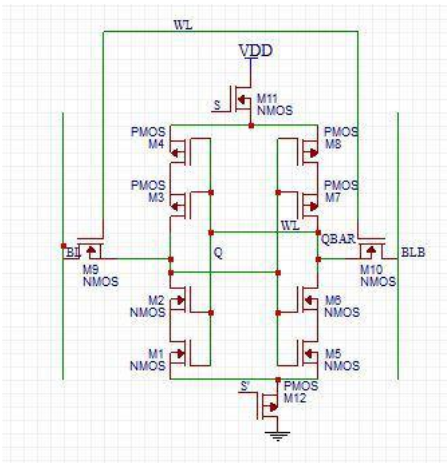

Fig4:12T SRAM -Cell schematic

Table1: Performance comparison of 7, 8, 10 and 12-Transistor topologies

S.No	Bit cell	SNM	Power consumption	Supply voltage
1	7T	290mv	20nw	1V
2	8T	310mV	25nw	1V
3	10T	330mV	30nw	1V
4	12T	340mV	33nw	1V

Table1 shows the comparison of various presentation metrics related to static noise margin, power dissipation and supply voltage of different topologies.

3. C.STATIC-NOISE-MARGIN (SNM)

The SNM is used to measure the SRAM cell steadiness. It is the extreme value of a dc disturbance that can be accepted by the cell before changing states [3]. Graphically, the SNM is characterized by the major square box that can be tailored in the butterfly characteristic curves of the SRAM cell [3]. The three designs in above figure were simulated such that all transistors are minimum-sized devices to achieve minimum cell area. During the read operation, the SNM is much smaller for the 6T design because the characteristic curves are tainted by the voltage separator among the access transistors (N3 and N4) and the drive transistors (N1 and N2). Without the read-disturb, the characteristic curves of the 8T design is that of two cross fixed inverters, which provide a larger SNM (Fig.6). Figure 5 shows the characteristic curves for the 7T design during its retention period and read access period. For a "0" read, the SNM for the 7T design is much larger than that for the 6T design, and thus improving the stability of the SRAM cell. Yet, if a time limit is set (word line is only active for a finite amount of time), the SNM actually increases as VDD decreases. This is since at a minor VDD, the cell current drawn from the bit line is smaller during a "0" read, so the charge stored onto the parasitic capacitance at node V1 is less, thus a lower voltage at node V1 is touched after a short amount of time, which means more static noise voltage can be tolerated before the cell change state. Here, SNM is the largest Vn that causes a state change in the cell after 400ps. Note that SNM is affected by the device ratio between the access transistors (N3 and N4) and the drive transistors (N1 and N2). Finally, figures below demonstrates that device mismatch degrades the SNM. Here, mismatch is introduced to the drive transistor N1. (1% mismatch is equivalent to WN1 = 0.99Wmin). In practice, process induced variations is not only limited to device geometry mismatch but also includes threshold voltage variability, which is not modeled in the simulations of this project. Therefore, SNM degradation can be more severe in reality

4. RESULT ANALYSIS:

Static noise margin with help of butterfly curves

Figures 5 demonstrates the values for VDD of 1 V for different number of transistor SRAM cells using butterfly

curves for static noise margin (SNM). As detected, SNM of the 7T bit-cell is lowest among all bit-cells owing to stronger influence of bit line voltage on the voltage level of the storage node. The lowest SNM (290mV) indicates that the 7T cell can flip the state in case of an existence of a slight noise on the storage node.

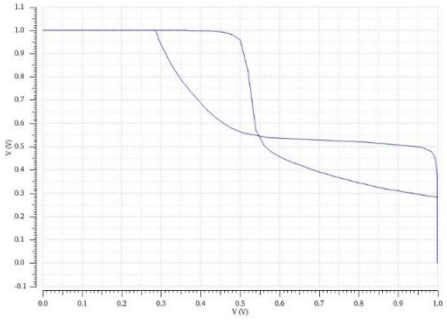

Fig5:7T SNM 290mv

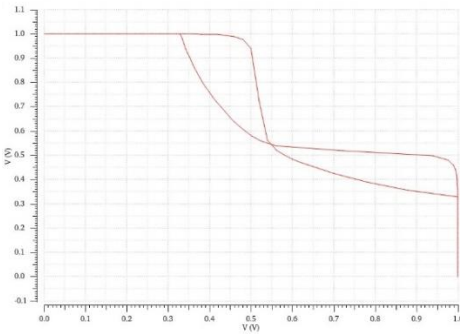

Fig6:8T SNM 310mv

From the figure 6 we can observe that the SNM of the 8T SRAM cell is 6.89 % (310 mV) greater than that of the 7T cell is shown in figure 6 [5].

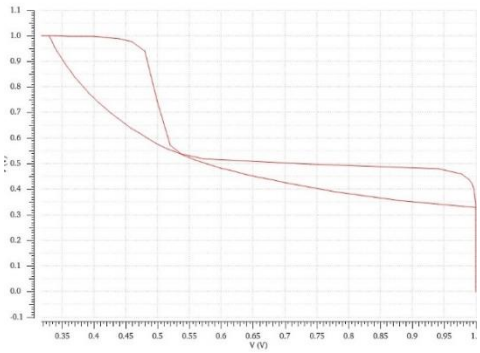

Fig7:10T 330mv

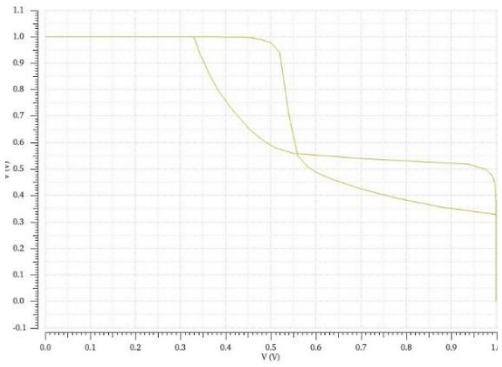

Fig8:12T 340mv

And SNM of the 10T SRAM bit-cell is 13.78 % (330mV) higher than that of the 7T bit-cell is observed from the figure 7. As a result, the 12T bit-cell validates the major SNM of 340 mV, which is 17.2 % higher as related with that of the 7T SRAM bit-cell.

5. CONCLUSION:

Designed four SRAM cell topologies of 7T, 8T, 10T and 12T stability performances have been presented. The speed of SRAM cell is increased based on the process technologies continue to advance, but devices will be more vulnerable to gaps, which damage the static-noise margin of SRAM cells. Due to performance concerns, the dual port designs that shows read disturb-free feature such as that seen in the 7T and 8T cell implementation might become more practical in the future SRAM cell implementation. And further if the technology is scaled beyond 45nm in order to increase the performance, performance of the device in terms of speed and power dissipation can be achieved by replacing CMOS with FinFET devices and also by applying different power reduction techniques.

REFERENCES:

1 L.Chang “SRAM cell Design for Stable 32nm Node and Beyond, “Symp.VLSI Tech.Dig., page.292-293, Jun., 2005.
2 “Low-Vdd Static-Noise-Margin-Free for Read SRAM Cell in High-Speed Applications,” JSSC, page.113-121, Jan., 2006. K.Takeda.
3 B. H. Calhoun, J. F. Ryan, S. Khanna, M. Putic, and J. Lach, “Flexible circuits and architectures for ultralow power,” Proc. IEEE, vol. 98, no. 2, pp.267–282, Feb.2010.
4 L. Chang., “An 8T-SRAM variability tolerance and low-voltage operation in high-performance caches,” IEEE, vol. 43, no. 4, page. 956–963, Apr. 2008.
5 Salahuddin, S., Jiao, H. and Chan, M. (2015), “Eight-FinFET fully differential SRAM cell with enhanced read and write voltage margins”, IEEE Transactions on Electron Devices, Vol. 62No. 6, pp. 2014-2021.
6 Chuang, S. Mukhopadhyay, J.-J. Kim, K. Kim, “A High-performance SRAM using CMOS: Design challenges and techniques,” in Proc. IEEE International Workshop Memory Technol., Design, Test., Dec. 2007, pp. 4–12.
7 J. Samandari-Rad, M.Guthaus, and R. Hughey, “Defying the inconsistency issues in the performance of next-generation SRAM design to optimize and expect the speed and yield,” IEEE Access, volume 2, page. 577–601, May 2014.
8 A High Density, Low leakage, 5T SRAM for embedded caches by Invagar Carlson, StefanAndersson, SreedharNatarajan, AtilaAvandpour IEEE 2004.
9 Sayeed Ahmad Mohit, Naushad Alam, and Mohmmad, Hasan, Senior Member, IEEE. Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell.
10 A. Fekietal., “10T SRAM bit cell with read, write selection,” Solid- State Electron., vol. 106, no. 4, page. 1–11, 2015.
11 Y.-W. Chiu, “A 40 nm bit-interleaving 12T sub threshold SRAM with data-aware write-assist,” IEEE Trans. Circuits Syst. I, Reg. Papers, volume. 61, no. 9, page. 2578-2585, Sep. 2014.
12 M.-H. Tu, J.-Y.Lin, M.-C.Tsai, S.-J.Jou, “Single ended sub threshold SRAM with asymmetrical write and read-assist,” *IEEE Transactions. Circuits*System.I, Reg. Papers,