Low Power and High Speed Synchronous Carry Generate Adder using Modified Gate Diffusion Input Technique

P.Kishore, S.Rajendra Prasad, Y.Chalapathi Rao

ABSTRACT--- Low power and high performance designs drew major focus in digital VLSI. In low-voltage and low-power applications, optimization of power dissipation and propagation delay of logic circuits is an important issue. Now a days, most of the high performance processors are built with arithmetic logic units in which the adders and multipliers are key components. The efficiency of these processors will be measured in terms of power dissipation, speed of operation. So, in order to develop low power and high performance processors, it is necessary to design the multipliers and adder circuits with required speed and power dissipation. This paper concentrates on design of a synchronous carry generate adder,generally called carry Look-ahead adder with low power dissipation and less propagation delay. The proposed design is implemented using a Modified Gate Diffusion Input technique in mentor graphics tools at 90nm technology.

Keywords-Power dissipation, Propagation delay, GDI technique, Carry Look-ahead adder.

I. INTRODUCTION

Years ago, the density of fabricated transistors in an IC and operating frequency were sufficiently low. In the era of high speed requirements, the levels of integration in an IC had a tremendous rise and more number of transistors with high speed and lesser physical dimensions are being integrated into an IC. This resulted in a constant rise in the operating frequency and the processing capacity per IC, which in turn increased the power dissipation.

Gordon Moore predicted in his first law that the no. of transistors in a IC will be doubled for 18 months. In spite of the exact numbers, it is observed that the growth rate of transistors on an IC is much higher than the predicted. The growth rate followed Moore's prediction up to 1980s and thereafter, there is huge difference between the predicted and the actual transistor count. VLSI technology failed to fill this gap with the existing fabrication limitations on silicon substrate. Later, Ultra Large Scale Integration (ULSI) technology was evolved to cater to the current day requirements which resulted in increased cost per IC [6]. Hence the design of high performance VLSI circuits with the existing requirements is one of the concentrated areas of the research.

Another factor that expresses the requirement for low power chips is the expanded interest of the market for portable electronic gadgets powered by batteries. The portable devices must be small in size, light in weight and more durable, without compromising with its required functionalities. Life of the battery is becoming a major product differentiator in many portable devices. It is also observed that the similar rapid changes are not experienced in batteries with respect to their physical dimensions and life time as compared to the electronic circuits[1]. So, it is necessary to design the portable systems with less power dissipation and high performance which in turn have long battery life.

It is also a difficult task to identify the suitable adder and multiplier circuit specific to certain operations initiated by the processor[2]. Hence, this has been considered as one of the issues in present work.

II. PROBLEM DEFINITION

In the development of adders and multipliers, a 1-bit full adder plays a major role as it is used as basic building block in designing complex adders and multipliers. In spite of large research going on to design an optimized high performance 1-bit adder cells, still there is a huge gap between present requirements to the available designs with respective to power dissipation, speed and area[3]. So, it is important to design an optimized 1-bit full adder cell which meets the requirements of the high performance adders and multipliers.

Designing such high performance logic circuits is a difficult task, as those circuits need to satisfy the low power dissipation and high speed with a reduced area. Due to the quadratic relationship between the power and speed, it is difficult to get low power and high speed simultaneously with most of the existing low power techniques. The existing techniques like CMOS logic, Transmission Gate and Pass Transistor logic etc., are not promising to find solution to above mentioned task. Therefore, to develop the logic designs without compromising the speed and power dissipation with less area is a major concern in VLSI research.

This paper proposes a synchronous carry generate adder which overcome the limitations of high performance circuits. Design of this adder requires the 2-input AND, OR and Ex-OR gates. All these sub-circuits are designed by

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using CMOS, Gate Diffusion Input(GDI) and Modified GDI techniques. Therefore,the performance of the proposed Synchronous carry generate adder is compared with the design using CMOS and GDItechniques. Introduction to GDI technique has been considered from author's publications.

III. MODIFIED GDI TECHNIQUE

In order to avoid the mentioned demerits of GDI technique[4], this this paper proposes a modification to existing GDI technique and named as Modified Gate Diffusion Input (MGDI) technique. The MGDI cell is developed from the GDI cell, with a proposed modification of substrates of PMOS and NMOS transistors are permanently connected to VDD and Ground (GND) respectively. The MGDI cell is shown in the Fig. 1. The generalized logic expression for the output of the MGDI logic cell is given in Eq.1.

$$D = P\bar{G} + NG \quad (1)$$

The operations derived by the MGDIcell are listed in the Table I. These operations are obtained based on Eq. 1. Here,SP and SN are representing the substrates of PMOS and NMOS transistors respectively,which are permanently connected to VDD and GND.

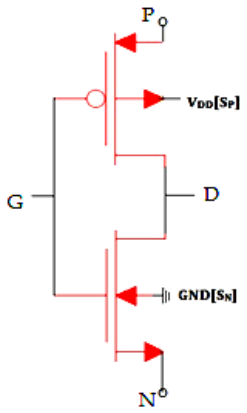

Fig. 1.Modified GDI cell

Table I. Functions implemented byusing MGDI cell

N	SN	P	SP	G	OUTPUT	FUNCTION
0	0	1	1	A	$\bar{A}$	NOT
B	0	0	1	A	AB	AND
B	0	A	1	A	A+B	OR
B	0	A	1	S	$A\bar{S}$+BS	2X1 Multiplexer

Table I., gives the list of functions obtained by the simple Modified GDI cell which is shown in Fig.1.The basic gates like Inverter, AND, OR and also the 2X1 multiplexer are implemented with only two transistors used by Modified GDI cell. MGDI cell has an advantage of reduced fabrication complexity as mentioned in GDI technique because the substrates are connected to VDD and GND terminals permanently. It also avoids the usage of debugging network to get the full output swing.

IV. PROPOSED SYNCHRONOUS CARRY GENERATE ADDER

The Carry Look-Ahead Adder (CLA) is also referred to as a synchronous carry generate adder in which carry outputs of the all stages are generated synchronously and are used to compute the sum output [5]. Basic property of this adder is to generate the carry outputs of all the stages in parallel. This decreases the overall propagation delay. In CPA, carry will be propagating all the stages, this is major concern with respect to speed.CLA aims at reducing this carry propagation delay and improves the overall speed. Carry propagation and carry generation are the main issues in addition process. This adder works on two boolean expressions on carry namely, carry generation and carry propagation, shown in Eq.4.8 and Eq.4.9 respectively.

$$G_i = A_i * B_i \quad (2)$$

$$P_i = A_i \oplus B_i \quad (3)$$

From the above expressions, it is noticed that carry generate and carry propagate signals depends only on the present inputs Ai and Bi. Accordingly, the sum and carry output expressions are shown in Eq. 4.and Eq.5.

$$C_{i+1} = G_i + P_i C_i \quad (4)$$

$$\text{Sum} = P_i \oplus C_i \quad (5)$$

These equations show that a carry is generated in the following cases.If both the inputs Ai and Bi are '1' , and If either Ai or Bi is equal to '1' and carry-in (Ci) is '1'. Let i=0, 1, 2, 3, ...n. The new carry equations can be obtained as follows:

$$C_1 = G_0 + C_0P_0$$

$$C_2 = G_1 + (G_0 + C_0P_0)P_1 \qquad C_3 = G_2 + (G_1 + C_1P_1)P_2$$

$$C_{n+1} = G_n + (G_{n-1} + C_{n-1}P_{n-1})P_n \quad (6)$$

From the Eq.6, it is noticed that all the carry signals are generated simultaneously, hence the name synchronous carry generate adder.

There are three stages to implement the CLA. First level generates the required propagate and generate signals. For 4-bit addition, four such sets will be generated and each set consisting with Ex-OR gate and an AND gates. Output signals of this level (Pi's &Gi's) will be valid after one gate delay. Second level consists of the Carry Look-Ahead (CLA) logic block which generates the carry signals (C1, C2, C3, and C4) as defined by the Eq. 6. It takes the carry propagate, carry generate and the initial carry(C0) signals as input and output signals of this level (C1, C2, C3, and C4) will be valid after three gate delays.Third level consists of four XOR gates (for 4-bit addition) which generate the sum signals (Si), (Si=Pi⊕Ci). Output signals of this level (S0, S1, S2, and S3) will be valid after four gate delays.

The CLA block for 4-bit addition is shown in Fig.2. By using this Carry Look-Ahead block, a 4-bit Carry Look-Ahead Adder can be constructed as shown in Fig.3.

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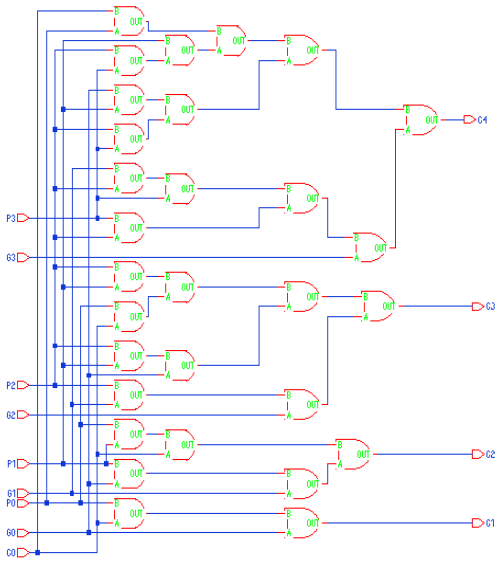

Fig. 2. Gate Level schematic of a 4-bit Carry Look-Ahead block

In this work, the design of the 8-bit and 16-bit Carry Look-Ahead Adder (CLA)s are proposed using CMOS, GDI, MGDI techniques. The required gates for this design are two input AND, OR and Ex-OR. The design of these gates using CMOS, GDI techniques have been discussed in author publication[6-9].Design of two input AND,OR,Ex-OR gates using the Modified GDI technique is carried out based on the input configurations listed in Table 1. These designs are shown in Fig.4,Fig.5,Fig.6.All the designs have low power dissipation,less propagation delay and required less number of transistors in compared with CMOS and GDI techniques. So, these design are being used in implementation in proposed adder.

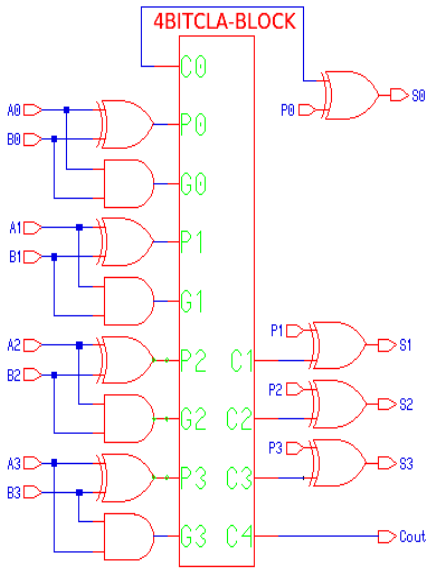

Fig. 3.Block diagram of a 4-bit Carry Look-Ahead Adder

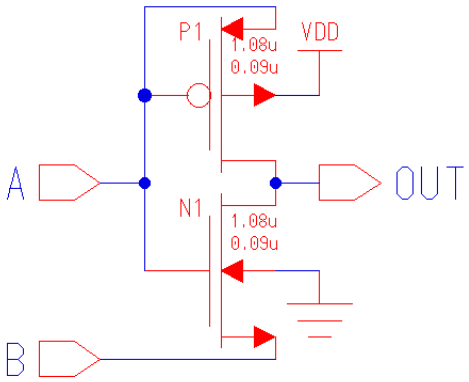

Fig.4.MGDI based two input AND gate

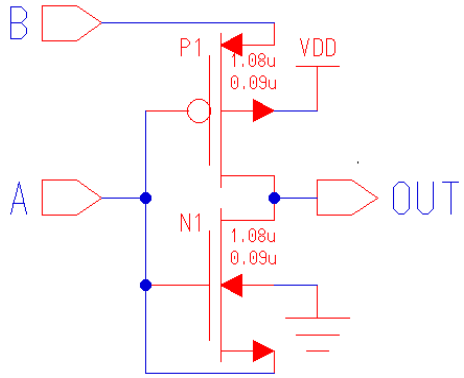

Fig. 5. MGDI based two input OR gate

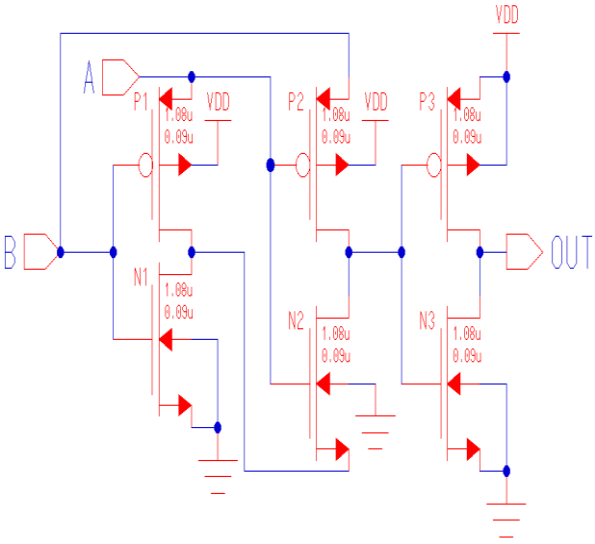

Fig. 6. MGDI based two input Ex-NOR gate

In designing of 8-bit CLA, an 8-bit input bit stream is required namely, A0 to A7 and B0 to B7 and a carry input signal(C_{in}). In this case, 8-Pis and 8-Gis are generated as per Eq.2 and Eq.3. The schematic of the 8-bit Carry Look-Ahead Adder is implemented as shown in the Fig.7. Here, It is cascaded with two 4-Bit CLAs which are designed as shown in Fig.3.

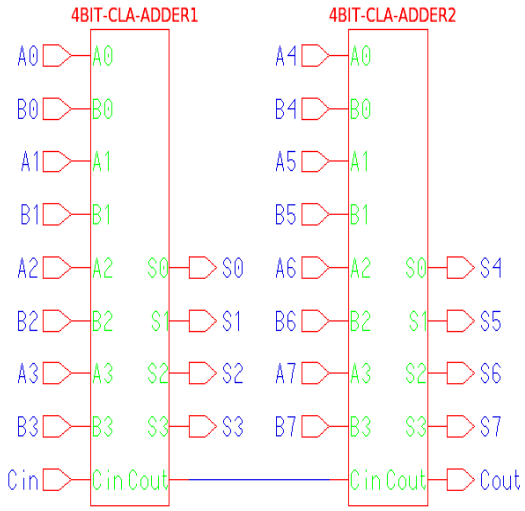

Fig. 7. 8-bit Carry Look-Ahead adder

To design the 16-bit CLA, two 8-bit Carry Look-Ahead Adders are required and are cascaded by giving the carry-out of the first 8-bit CLA to the carry-in of the second 8-bit CLA as shown in the Fig.8. 8-bit CLA is taken from Fig.7.

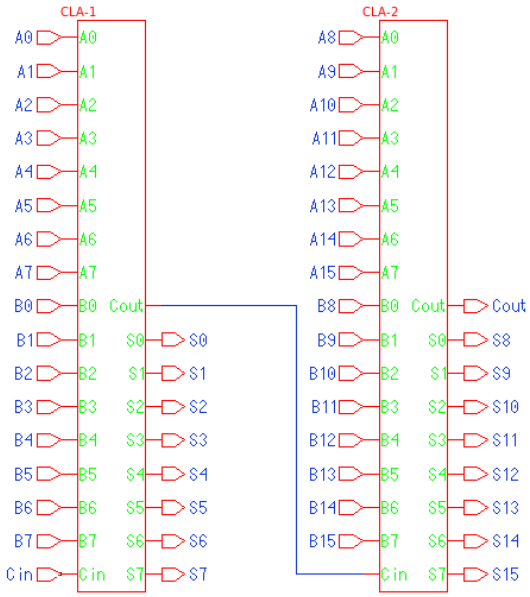

Fig.8. 16-bit Carry Look-Ahead adder

Block diagrams of 4-bit CLA, 8-bit CLA and 16-bit CLAs are represented in Fig.3,Fig.7,Fig.8.As the basic architecture is common in CMOS, GDI and MGDI technique, a common block diagrams are used to represent the three methods is shown to avoid the redundancy.

V. RESULTS

Initially, the designed 8-bit and 16-bit synchronous Carry Generate Adders are verified for functionality. Here, to avoid the redundancy functionalities of MGDI based architecture are represented. Later, power dissipation, Propagation delays and transistor count are compared with existing techniques. The output waveforms of MGDI based 8-bit CLA are shown in the Fig.9.Output results are verified for the following data.

A[7:0]=10111111,

B[7:0]=01111111 and initial carry input(C_{in})=‘0’.

For this input data sum and carry outputs are S[7:0]=00111110 and C_{out}=‘1’ respectively. For applying the above input data, Y1and Y2have been considered with logic ‘1’ and logic ‘0’ respectively. Y2 is connected to A6 and B7, and the remaining inputs are connected to Y1.

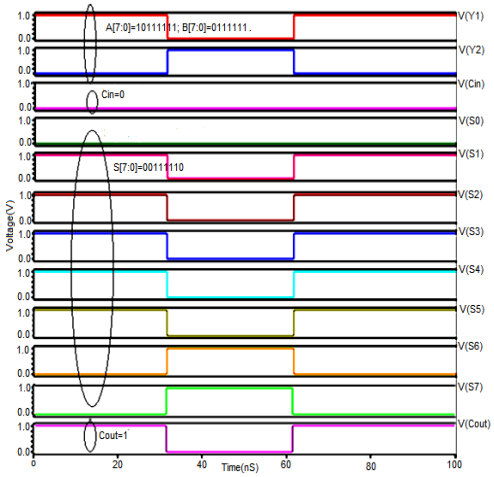

Fig.9. Simulation results of 8-bit CLA using MGDI technique

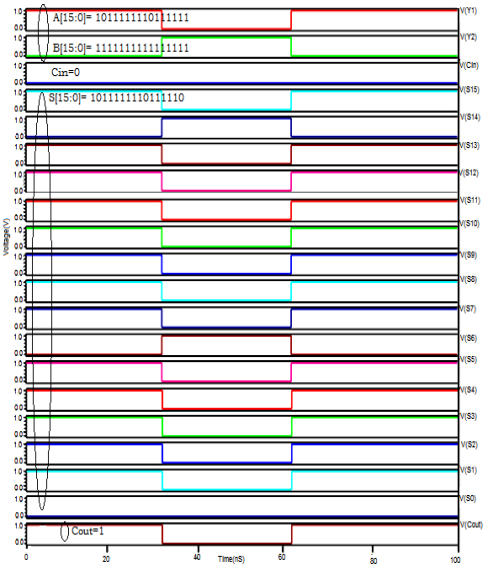

Fig.10. Simulation results of 16-bit CLA using MGDI technique

Simulation results of MGDI based 16-bit CLA is shown in Fig.10.and verified the functionality for the following example.

Inputs areA[15:0]= 1011111110111111,

B[15:0]= 1111111111111111 and C_{in}=0

Sum and carry outputs for the given inputs are

S[15:0]= 011111110111110 and

C_{out}=1 respectively.

Here, Y_1 and Y_2 are two binary inputs with logic ‘1’ and ‘0’ respectively and are applied to actual inputs A[15:0] and B[15:0].In this case, Y2 is connected to A6 and A14 ports and Y1 is connected to remaining all ports of A[15:0] and

B[15:0].For comparative analysis, each 8-bit module can be replaced by an 8-bit CMOS, GDI and MGDI CLAs and corresponding functionalities are verified through simulation results.The total power dissipation, propagation delay and the overall transistor count of the proposed designare tabulated in the Table II.

Table II .Power dissipation, Propagation delay and Transistor count of sychnronous Carry Generate Afder

Type of Adder	Parameter	CMOS	GDI	MGDI
8-bit CLA	Total Power Dissipation in pW	300X106	250.98	169.14
	Propagation Delay in ns	165	98	75.05
	Transistor Count	294	246	98
16-bit CLA	Total Power Dissipation in pW	600X106	305.09	289.06
	Propagation Delay in ns	330	190	170
	Transistor Count	588	492	196

VI. CONCLUSIONS

In this paper, the high performance adder called Synchronous Carry Generate Adder/Carry look-ahead adderis designed by using existing techniques(CMOS and GDI) and proposed MGDI technique. The functionalities of MGDI based designs have been verified. It is observed from the Table II. that MGDI based designs offers less power dissipation, high speed and require less no. of transistors. Hence, it is concluded that MGDI based adders can be used in high performance applications and can be used in the multipliers.

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