

# Design and Implementation of Low Power Energy Efficient Binary Coded Decimal Adder

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**Abstract:** A novel architecture for low power decimal addition using binary representation is presented in this paper. The proposed BCD adder uses Binary to Excess Six Converter (BESC) block for constant correction to adjust binary outputs exceeding 9 to correct decimal values and exploits the inherent advantage of reduced delay and switching, due to elimination of long carry propagation in second stage addition as in conventional design and switching OFF of the BESC block for decimal outputs less than 9. The proposed adder design is done using VHDL code and implemented in Altera Quartus board. The results demonstrate that the proposed decimal adder can lead to significant power savings and delay reduction compared to existing BCD adders which is realised in better power-delay product (PDP) performance. For example the PDP saving of the proposed BESC-BCD adder for a 1 digit and 2 digit addition implementations are 11.6% and 16.05% respectively, compared to the best of the designs used for comparison.

**Keywords:** Ripple Carry adder, Constant correction, Binary to Excess Six Conversion, Terahertz Optical Asymmetric Demultiplexer.

## I. INTRODUCTION AND RELATED WORK

The Computer systems were based on the decimal (base 10) numbering system rather than the binary numbering system in earlier days. These systems are popular for business/commercial applications. The decimal arithmetic overwhelms the binary arithmetic in money transactions. Therefore, the use of decimal arithmetic in business applications is specified by a large number of software systems [1].

The conversion between the string representation of a decimal number and its BCD representation is the significant feature of BCD representation over binary representation. The fixed and floating point binary

representations are not able to represent floating and fixed point binary representations. So this conversion plays a vital role when working with fractional values. The process of reading and writing in a BCD device and doing arithmetic operation is handled efficiently using BCD operators. The proposed architectures on decimal arithmetic include: A novel BCD adder by Behrooz shirazi et al., [2] using redundant BCD addition. The design involves simple conversion of a BCD number to redundant form, perform addition and reconvert the result back to BCD form. The extra conversion circuit used adds huge delay and increases complexity.

In another technique, Robert D.Kenny et al., [3] used non-speculative addition which have lesser delay. Adder for decimal addition proposed in [4] use speculative addition technique at the first stage. The proposed correction unit independent of the input operands is the significant feature. The feature of the design is that it has a regular structure and the design of correction unit is independent of the number of input operands

Some researches use reversible logic for the design of BCD adders [4][5][6]. The reversible logic adders provides less power dissipation and less speed. In a pioneer work on BCD addition, Sreehari Veeramachaneni et al., [7] added correction bits using multiplexer. The use of multiplexers for constant correction reduces delay compared to the state of art approaches.

Alp Arslan Bayrakci & Ahmet Akkas [8] proposed a BCD adder using analyzer circuit for carry generation. The reduced number of gates in the critical path of correction circuit reduces the total delay of the circuit. Anshwal Singh et al., [9] proposed an architecture for binary coded decimal addition using prefix block, correction block and PG block. Since the correction circuit is embedded within the pre-computing blocks the design complexity is less compared to the BCD adder in [10]. Gayen et al., [11] proposed a novel design for decimal (BCD) adder using Terahertz Optical Asymmetric Demultiplexer (TOAD).

Chetan Kumar et al., [12] proposed architecture for decimal arithmetic which can also perform binary addition. The circuit has high speed but it shows low performance for multi-bit operands. In a pioneer work, Sundaresan et al., [13] used Carry Look Ahead (CLA) addition for the first stage, carry network for second stage and correction logic for third stage.

**Manuscript published on 30 December 2018.**

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The architecture in [13] demonstrates better delay reduction compared to the architecture in [12], however the first stage CLA adder increases hardware complexity. A two stage correction free adder for BCD addition is proposed by Osama Al-khaleel et al., in [14]. In stage 1, the MSB three bits of a four bit BCD number are added. In second stage the result from stage 1 is added with the LSB. Since the circuit doesn't have any extra circuit for constant correction the latency is very less compared to the previous approaches. Shuli GAO Et Al. [15] implemented a new architecture of BCD adder using 6-input LUTs and fast carry chains. The proposed design demonstrates better critical path delay reduction however the circuit is prone to more power dissipation. Vijeyakumar et al, [16] proposed a new architecture for BCD addition using flag bit generation. The architecture uses flag bit computation and flag inversion logic to generate the decimal equivalent for outputs exceeding 9. The speed of the architecture is high due to use of Carry Select Adder (CSLA) [17] and CSK adder [18] for first stage addition, however it is prone to high power dissipation.

The main idea of this work is to reduce power and latency in BCD addition by using BESC instead of 4-bit Ripple Carry Adder (RCA) as in conventional design for the correction constant addition for decimal outputs exceeding 9. The main advantage derived is realization of BESC with lesser number gates compared to a 4 bit RCA. The output of first stage adders and BESC block are passed through a multiplexer. The multiplexer select signal produced by control logic generates 1 for sum values exceeding 9 and 0 for other values. The other sections of the paper are organized as follows. The conventional BCD adder is discussed in Section 2. Section 3 discusses about the design of proposed low power and energy efficient BESC- BCD adder. Section 4 presents the BESC logic and its detailed structure. The area and delay evaluation of the proposed and conventional decimal designs are discussed in section 5. The experimental result of the proposed adder is discussed in section 6. The implementation detail of the proposed design for a 2 digit addition is discussed in section 7. Section 8 gives a brief conclusion of the work done.

**II. Overview of BCD Addition**

The two decimal digits addition in BCD along with a possible carry from previous least significant digits produces a result of 19. The equivalent representation for the sum in the range 0 to 19 in binary is 0000 to 10011 and in BCD is 0000 to 1 1001 (MSB 1 is carry and next four LSBs is BCD digit sum) and is shown in Table 1. It is seen from Table 1, that for the binary sum equal to or less than 1001 the corresponding BCD digit is the same. The result is invalid BCD when the binary sum exceeds 1001 and needs correction. The binary sum is converted to correct digit by addition of 6(0110)<sub>2</sub> and a carry [19]. Based on the above methodology, the architecture of a 1digit BCD adder [19] is shown in Fig 1.

The input digits in binary are A (A<sub>3</sub>A<sub>2</sub>A<sub>1</sub>A<sub>0</sub>) and B(B<sub>3</sub>B<sub>2</sub>B<sub>1</sub>B<sub>0</sub>). S<sub>3</sub>' S<sub>2</sub>'S<sub>1</sub>'S<sub>0</sub>' are the sum outputs of the first stage 4 bit adder. The carry output C<sub>N</sub> shown in Equation (1) will be one for sum exceeding 9 or else it will be 0. When C<sub>N</sub> is 1, a correction constant 0110(6) will be added with S<sub>3</sub>'S<sub>2</sub>'S<sub>1</sub>'S<sub>0</sub>' by the second stage adder to produce the

decimal adjusted output S<sub>3</sub>S<sub>2</sub>S<sub>1</sub>S<sub>0</sub> and its realisation is shown in Equation (2)-Equation(5)

$$C_N = C_{OUT} + S'_3 S'_2 + S'_3 S'_1 \tag{1}$$

$$S_0 = S'_0 \tag{2}$$

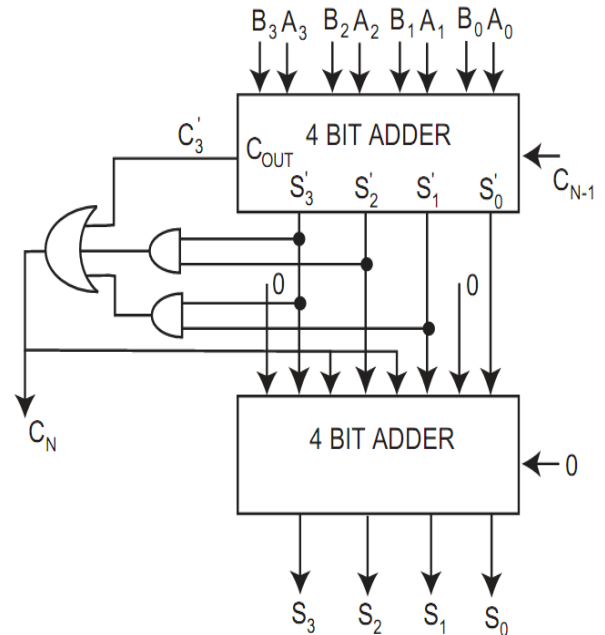
$$S_1 = S'_1 \oplus C_N \oplus C_1 \tag{3}$$

$$S_2 = S'_2 \oplus C_N \oplus C_2 \tag{4}$$

$$S_3 = S'_3 \oplus C_3 \tag{5}$$

**Table 1 Binary and BCD equivalent representation for possible outputs of decimal addition**

Decimal output	Binary Equivalent	BCD Equivalent
0	0000	0000
1	0001	0001
	-	-
9	1001	1001
10	1010	1 0000
	-	-
15	1111	1 0101
16	1 0000	1 0110
17	1 0001	1 0111
18	1 0010	1 1000
19	1 0011	1 1001



**Fig .1 Block diagram of Conventional BCD Adder**

**III. PROPOSED BESC-BCD ADDERS**

The structure of the proposed BCD adder using BESC for constant correction addition is shown in Fig 2. In addition to the BESC unit, the proposed design consists of a 4 bit RCA, Carry generator and four 2:1 multiplexer (mux). The schematic of Carry generator is shown in Fig.3 .



When the output from first stage 4 bit RCA exceeds 9, Carry generator produces 1. The Carry generator output is used as the control/select signal for the four 2:1 multiplexer group (shown as 8:4 mux in Fig.2). One input to the four 2:1 mux are the output bits of first stage adder ( $S_3S_2S_1S_0$ ) and the other input is the BESC output ( $M_3M_2M_1M_0$ ). The mux selects either of the inputs based on the control signal from Carry generator ( $C_{out}$ ) to produce the output ( $O_3O_2O_1O_0$ ) with  $C_{out}$  being the carry out bit. The main feature of the proposed decimal adder is the BESC unit which shows significant reduction in delay and switching due to elimination of carry propagation in second pair of RCA as in conventional design.

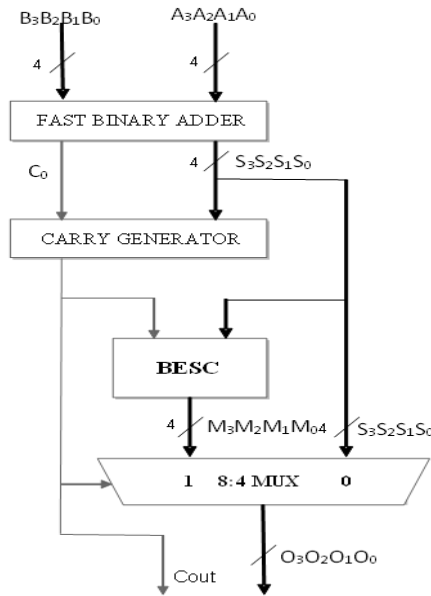


Fig.2 Block diagram of proposed BESC-BCD Adder

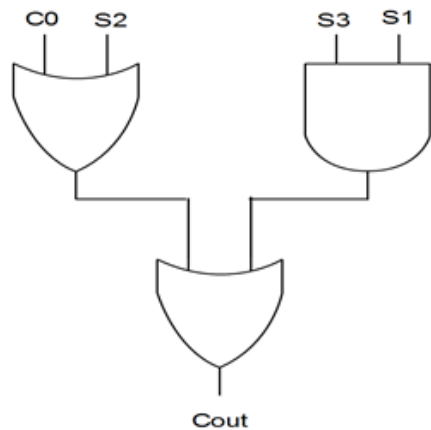


Fig.3 Schematic of Carry generator

IV. BESC

As stated in section 1, the objective of the work is to introduce BESC instead of a separate RCA for adding correction constant (0110: 6) to

Adjust outputs exceeding 9 to correct decimal. A 4 bit BESC is used to replace 4 bit RCA for correction constant addition. The logic table which realises the binary to excess six conversions is shown in Table 2 and its schematic in Fig 4.

Table 2 Logic Table for Binary to Excess 6 Conversion

C <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	M <sub>3</sub>	M <sub>2</sub>	M <sub>1</sub>	M <sub>0</sub>
0	0	0	0	0	X	X	X	X
0	0	0	0	1	X	X	X	X
0	0	0	1	0	X	X	X	X
		-			X	X	X	X
		-			0	0	0	0
0	1	0	0	1	0	0	0	1
0	1	0	1	0	0	0	1	0
0	1	0	1	1	0	0	1	1
0	1	1	0	0	0	1	0	0
0	1	1	0	1	0	1	0	1
0	1	1	1	0	0	1	1	0
0	1	1	1	1	0	1	1	1
1	0	0	0	1	1	0	0	0
1	0	0	0	1	1	0	0	1
1	0	0	1	0	X	X	X	X
1	0	0	1	1	0	0	0	0

X – represents don't care state

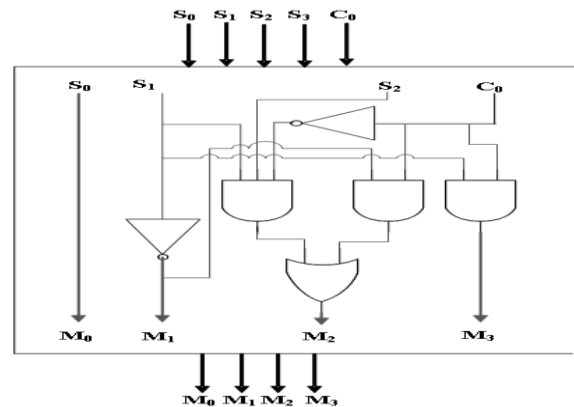


Fig 4. Schematic of BESC

The logic equations that define the output of BESC are shown as in Equation (6) to Equation(9).(Note the symbols - NOT, + OR, & AND)

$$M_0 = \overline{S_0} \tag{6}$$

$$M_1 = \overline{S_1} \tag{7}$$

$$M_2 = C_0 \& S_1 \& S_2 + C_0 \& S_1 \tag{8}$$

$$M_3 = C_0 \& S_1 \tag{9}$$

V. AREAS AND DELAY EVALUATION OF PROPOSED BESC-BCD ADDER AND CONVENTIONAL BCD ADDER

Area and delay evaluation of the proposed and conventional designs are done based on their equivalent NAND implementation. The NAND implementation of basic elements viz., Full Adder (FA), NOT, AND and OR gates used in the proposed and conventional BCD adder designs are shown in Fig 5.

We assume the delay of NAND gate to be 1 unit and area equal to 1 count.



The gates in parallel between dotted lines perform parallel operation and we use only one gate delay in these cases for calculation of worst case delay of circuit/element. Based on the above approach, the delay and area of the individual elements that make up the proposed design is shown in Table 3.

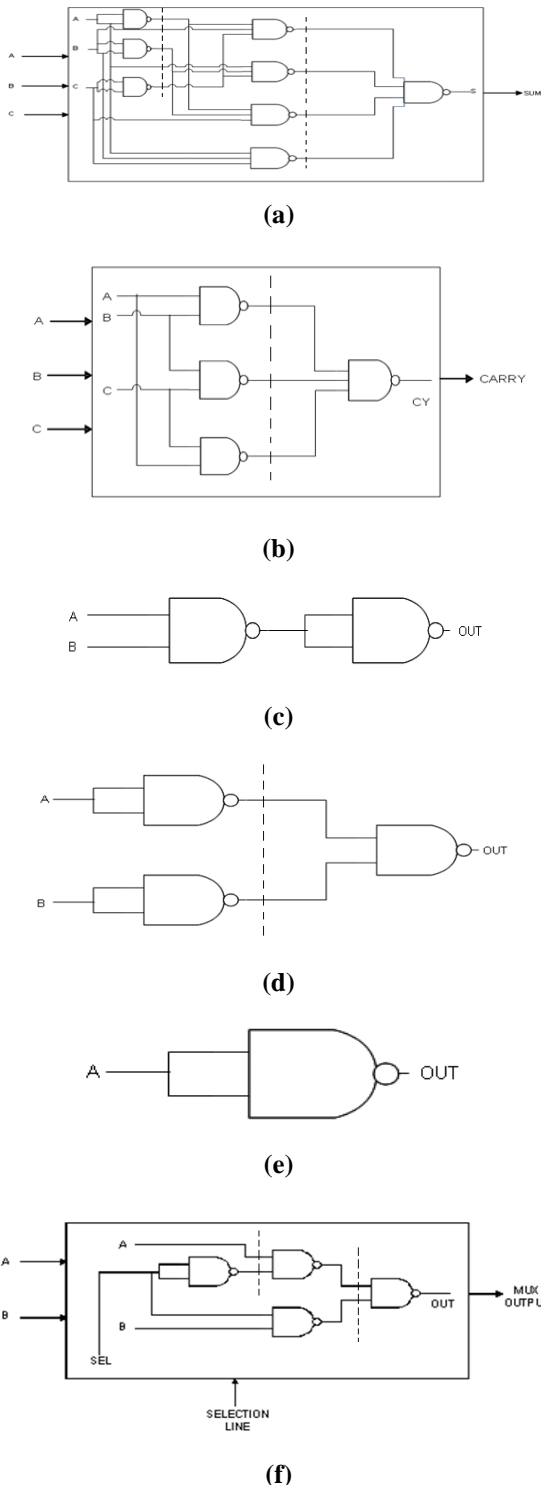


Fig .5 NAND implementation of (a) Full adder sum (b) Full adder carry (c) NOT logic (d) AND logic (e) OR logic (f) 2:1 Mux

Table 3 Area and delay of basic elements of BCD adder implemented using NAND logic

Element	Area	Worst case delay
Full adder	Sum:8 + Carry:4 =12	3

NOT	1	1
AND	2	2
OR	3	2
2:1 Mux	4	3

The area count and worst case delay of the proposed and conventional BCD adder designs are calculated as follows. The worst case delay is found by counting the number of NAND gates in the critical path and the area is evaluated by counting the total number of NAND gates that make up the circuit.

(a) Area count evaluation

The steps that lead to the area count evaluation for the BCD adder designs shown in Fig 1 and Fig 2 are as follows. From Fig 1 it can be seen that 4 FA(1<sup>st</sup> stage adder) + 2 AND & 1 OR (Correction circuit) + 4 FA (2<sup>nd</sup> stage adder) make up the conventional BCD adder. Using Table 3 the NAND equivalent gate count of the decimal adder in Fig 1 is found to be (48 + 4 + 3 + 48) 103. Using a similar approach, the area count of the proposed BESC-BCD adder shown in Fig 2 is evaluated as 4 FA(1<sup>st</sup> stage adder) + 1 AND & 2 OR(Carry generator) + 2 NOT & 3 AND & 1 OR(BESC) + 16 NAND(4 – 2:1 mux) with corresponding NAND equivalent count being 83. The results of the evaluation are shown in Table 4. It is seen from Table 4 that the NAND equivalent circuit.

Table 4 Area count (in NAND equivalent) of the proposed BESC-BCD adder and Conventional design

Basic Blocks	Conventional design	Area count	BESC-BCD design	Area count
1st stage adder	4 FA	48	4 FA	48
Correction circuit / Carry generator	2 AND + 1 OR	7	1 AND + 2 OR	8
2nd stage adder	4 FA	48	-	-
BESC	-	-	2 NOT+3 AND + 1 OR	11
2:1 mux	-	-	4 NAND	16
<b>Total</b>		<b>103</b>		<b>83</b>

Table 5 Worst case delay estimates (in NAND equivalent) of Conventional and proposed BESC-BCD adders

Basic Blocks	Conventional design	NAND equivalent delay	BESC-BCD design	NAND equivalent delay
1st stage adder	4 FA	12	4 FA	12
Correction circuit/ Carry generator	1 AND + 1 OR	4	2 OR or (1 OR + 1 AND)	4
2nd stage adder	4 FA	12	-	-
BESC	-	-	1 NOT+1 AND + 1 OR	5
2:1 mux	-	-	3 NAND	3
<b>Total</b>		<b>28</b>		<b>24</b>

(b) Delay evaluation

We have evaluated the worst case delay of the proposed and conventional BCD adder designs as follows. The delay of conventional BCD adder shown in Fig 1 is 4 FA carry (1<sup>st</sup> stage addition) + 1 AND & 1 OR (correction circuit) + 4 FA carry (2<sup>nd</sup> stage addition). Based on the consideration of the delay values for individual elements (in NAND equivalent implementation) shown in Table 3, the worst case delay of conventional BCD adder is estimated to be (12 + 4 + 12) 28. Using a similar approach the delay of proposed BESC-BCD adder shown in Fig 2 is 4 FA carry(1<sup>st</sup> stage addition) + 1 AND/1 OR & 1 OR(Carry generator) + 1 NOT & 1 AND & 1 OR(BESC) + 3 NAND (2:1 Mux) with the corresponding NAND equivalent delay to be (12+4+5+3) 24. The results of the evaluation are shown in Table 5. It is seen from Table 5

that the delay of the proposed BESC-BCD adder decreases by 4 units compared to the conventional BCD adder.

VI. EXPERIMENTAL RESULTS

The proposed BESC-BCD adder is designed using VHDL and synthesized using Altera Quartus II with EP2C35F672C6 device. Conventional BCD adder [19], Correction free BCD adder [14], Carry skip BCD adder [20] and Flagged BCD adder [16] are used for comparison. The designs used for comparison are also described using VHDL and synthesized using Altera Quartus II with the same device. The area, delay and total power dissipation results of proposed and previous designs are shown in Table 6. It is seen from Table 6, that the proposed BESC-BCD adder has lower power dissipation and reduced delay

Table 6 Comparison of Area, Delay, Power dissipation and PDP of proposed BESC-BCD adder and state-of-the art designs

Parameters	Area (Number of LEs)	Delay (ns)	Static power dissipation (mW)	Total power dissipation (mW)	Energy dissipation-PDP (mW-ns)
<b>BCD Adders</b>					
Conventional design[3]	11	15.230	80.04	144.06	2194.03
Correction free[16]	29	13.326	80.05	147.02	1959.19
Carry skip[9]	15	17.100	80.02	138.36	2365.96
Flagged BCD-Using CSLA[20]	13	12.303	80.04	146.43	1800.7
Flagged BCD -Using CSK[20]	9	12.984	80.04	146.31	1899.1
Proposed-BESC BCD (RCA in 1 <sup>st</sup> stage)	11	11.815	80.01	134.75	1592.1
Proposed-BESC BCD (CSLA in 1 <sup>st</sup> stage)	13	11.657	80.01	137.32	1600.73
Proposed-BESC BCD (CSK in 1 <sup>st</sup> stage)	11	11.815	80.01	134.53	1589.47

Compared to all other architectures used for comparison, thanks to the BESC unit which realises constant correction addition with minimal switching and has fewer gates in the critical path. The energy dissipation represented as product of power and delay (PDP) of the Proposed BESC-BCD adder is 11.6% lower compared to the best of the previous designs used for comparison. The area of the proposed BCD adder represented in Logic Element (LE) count is low compared to Correction free [14] and Carry skip [20] BCD designs. However the proposed BESC-BCD adder show high LE count compared to the Flagged BCD design (with CSK in the first stage addition) [16].

shown in Fig 6. The carry out of the first digit adder (C<sub>out</sub>) is used as the carry input for 4 bit RCA in second digit addition. The performance parameters of 2 digit adder implemented with proposed BESC-BCD adder and other approaches are shown in Table 7. From the Altera Quartus II results, it is seen that 2 digit addition using proposed BESC-BCD adder designs exhibit lower delay and reduced total power dissipation compared to all other architectures used for comparison. The reduction in delay is due to realisation of second stage constant correction with 1 NOT+ 1 AND +1OR which eliminates the long carry propagation path as in Conventional BCD adder[19], Correction free[14], Carry skip[20] and Flagged BCD adder[16] designs. The better delay and power dissipation performance of the proposed BESC-BCD design demonstrates better PDP product of the proposed design compared to all other architectures used for comparison.

VII. Implementation of Proposed BCD-BESC Adder for Two Digit Addition

To determine the functionality of the proposed BCD adder an implementation in 2 digit addition is done and is



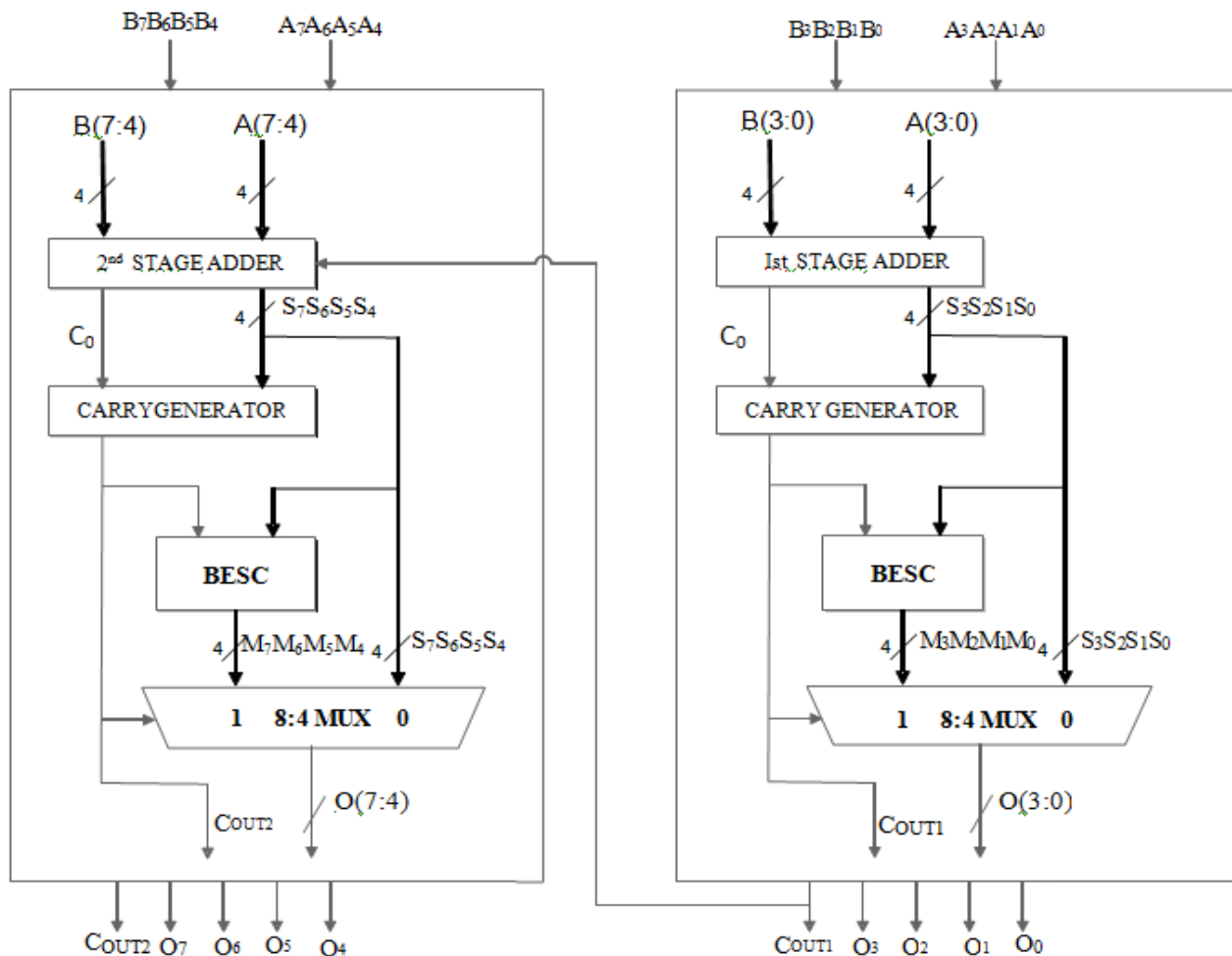


Fig 6 Block diagram of 2 digit adder implemented with proposed BESC-BCD adder

Table 7 Comparison of Area, Delay and Power dissipation and their products of proposed BESC-BCD adder and state-of the art designs for a two digit implementation

Parameters	Area (Number of LEs)	Delay (ns)	Static power dissipation (mW)	Total power dissipation (mW)	Energy dissipation (PDP) (mW-ns)
<b>BCD Adders</b>					
Conventional[3]	24	18.42	89.05	172	3167.38
Correction free [16]	58	16.33	89.34	173.06	2825.38
Carry skip[9]	32	21.12	91.56	174.27	3680.58
Flagged BCD-Using CSLA[20]	25	15.65	80.14	175.39	2744.85
Flagged BCD -Using CSK[20]	21	16.49	86.83	169.22	2791.11
Proposed-BESC BCD (RCA in 1 <sup>st</sup> stage)	21	14.52	80.09	158.75	2304.26
Proposed-BESC BCD (CSLA in 1 <sup>st</sup> stage)	26	14.2	80.10	163.66	2323.32

VIII. CONCLUSION

We have proposed a new adder for decimal addition using the concept of binary-excess six conversions for constant correction, to adjust outputs exceeding 9 to equivalent decimal. An extensive evaluation of area and worst-case delay of the proposed decimal adder with conventional design, fair better results which proves the novelty of the proposed methodology. The proposed BESC-BCD adder

overwhelms other previous designs in terms of power dissipation and delay performances. The potential benefits of reduced delay and power dissipation of our proposed BESC-BCD adder can be realized in fair PDP saving performance. This makes our design suitable for portable VLSI implementation.



Moreover, the proposed methodology for decimal addition can be easily extended to multi digits.

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