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Performance Analysis of Reconfigurable Heterogeneous Adder Architectures

S.Karthick, R.S.Valarmathy R.Nirmalkumar

Abstract: ***The computational problems are solved by adaptable fabrics. A reconfigurable fabric has attracted high priority as the complexity and throughput has increased. The problem related to a specific architecture can be effectively addressed by reconfigurable computing. Various adder structures like Carry Bypass (CBA), Carry Look-Ahead (CLA), Ripple Carry Adder (RCA) and Carry Select (CSLA) with reconfigurable architecture are designed for Field Programmable Gate Array (FPGA) application. Performance metrics like area speed and power consumption can be effectively optimized by reconfigurable architectures. More fine grained architecture with improved can be achieved using reconfiguration techniques. The proposed structures are coded in Verilog-HDL. These architectures are targeted for 65 nm technology node using Synopsis tool. The proposed technique can be extended for more complex designs with improved performance. An area reduction of 14% to 44% and power reduction of 18% to 54% has been achieved using proposed reconfigurable adder architectures.***

Keywords: Fabrics, Fine grained, Reconfiguration, Tradeoff

I. INTRODUCTION

Commonly algorithms can be executed with one of the two methods viz. ASIC's (Application Specific Integrated Circuits) and the microprocessors. Usually ASIC's are the hardware and these cannot be altered once the fabrication is done, but it has higher performance compared to the microprocessors. On the other-side, the microprocessor has the ability to alter the configuration at the cost of the timing. To overcome or to gain or to balance the flexibility and performance of the product, a new computing methodology called reconfigurable computing was developed, which has the ability to reconfigure the hardware even after fabrication. Reconfigurable computing is performed in reconfigurable devices. The performance lag between software and hardware can be effectively rectified using reconfigurable computing [1].

Reconfigurable computing has become one of the most attractive research areas for the researchers because of its reconfigurability by the end-user without any further fabrication costs and yielding the benefits similar to the ASIC's [2]. Reconfigurable solutions at the bit level operations form the basic building tiles and provides wide spectrum of applications ranging from control-dominant architectures to complicated (DSP) Digital Signal Processing applications.

The reconfigurability provides optimized energy and power efficiency in addition to flexibility and performance optimization. Targeting a specific application will improve power optimization as compared with designs for generic applications. From one of the study, the use of reconfigurable circuitry instead of software loops saves the energy by 35% to 70% with average speed of 3 to 7 times depending on the particular device used [3]. Heterogeneous adder architectures to obtain power optimization is proposed [4]. Researchers have utilized the different classifications of reconfigurable computing and developed several architectures. In [5], author has designed novel adder architecture for least latency using pipeline and parallel computing technique. A run-time reconfigurable architecture to facilitate the binary and BCD add/subtract is developed in [6].

The configurable instruction can be achieved using reconfigurable course-grained architecture [7]. Reusable, Modular and Scalable framework concepts are utilized in developing a high-end reconfigurable computer's and helps in providing more computing-throughput than DSP-based system [8]. In [9], the author has proposed a configurable computing machine (CCM) using Reconfigurable Computing Application Framework for interactive applications. A novel reconfigurable computing system based MorphoSys processor implementation is described in [10]. In this paper, the flexibility of reconfigurable architectures is explored and various combinations of adder variants are configured to achieve low power and less area for the implementation of design. Depends on the user defined specifications the proposed reconfigurable adder can be utilized for optimized design metrics like throughput, delay and power consumption. The paper is organized as follows. Various reconfigurable computing techniques and architectures are given in section 2. Existing and proposed architectures are illustrated section 3. The techniques used to implement the proposed techniques are explained in section 4. Section 5 describes results and conclusion is given in section 6.

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II. RECONFIGURABLE COMPUTING

By utilizing the reconfigurable fabrics the hardware and software are interlinked to achieve optimized performance. Even while the hardware is in running condition to ability to adapt to new designs is made possible by reconfigurable computing. The functional and system level visualization helps to improve the hardware and software co interface in an efficient manner. An differentiation can be made depends on coupling degree between processing and functional units. In a reconfigurable system single or multiple memories and processors will be made available.

Fig. 1(a) to 1(e) shows the example of coarse grained reconfigurable systems. Each of these classifications has their own benefits depending on their coupling mechanisms with processor. The most loosely bounded reconfigurable hardware may have infrequent communication between the hosts and is alike to that of the net workstations, where dispensation is extremely slow. An example is shown in Fig. 1(a). In Fig. 1(b) we can observe the attached processing unit similar to another processor in multiprocessor system where communication between the host and the reconfigurable fabric is the major overhead and these are useful when large chunks of data need to be computed. Reconfigurable fabric itself can behave like a co-processor and these doesn't need the constant supervision of the processor. An example is given in Fig. 1(c). As shown in Fig. 1(d), the reconfigurable fabric can be made as functional unit in the host processor and allow for the creation of custom instructions. Finally the processor can be made embedded in reconfigurable fabric as shown in the Fig. 1(e). Further differentiation can be made in fabrics based on structure complexity which can be subdivided in to course and fine grained architectures.

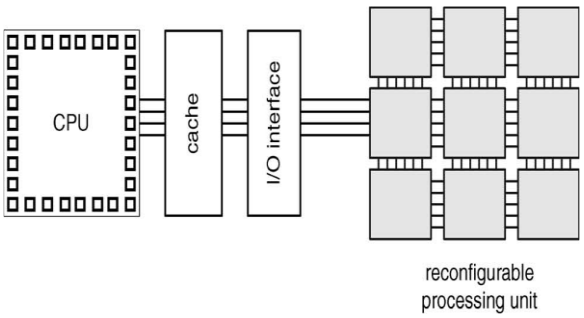

Figure 1(a)

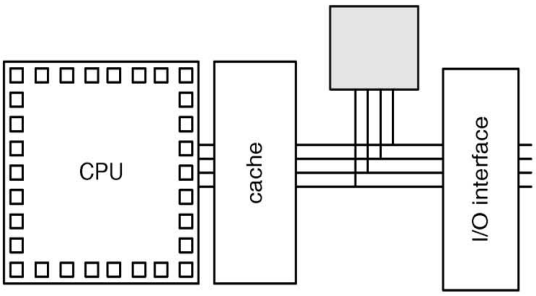

Figure 1(b)

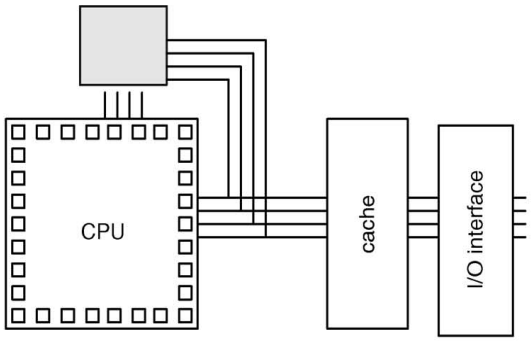

Figure 1(c)

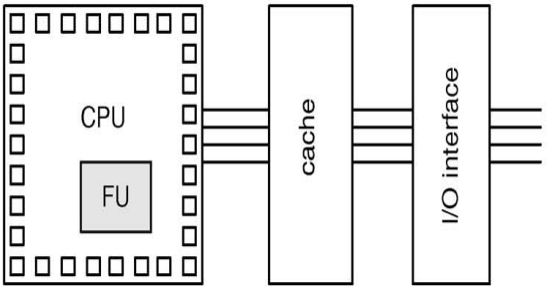

Figure 1(d)

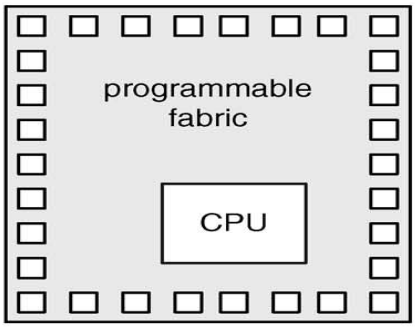

Figure 1(e)

Figure 1: Reconfigurable classification. (a) External stand alone processing unit [1, 4]. (b) Attached processing unit [1, 4]. (c) Co-processor [1, 4]. (d) Reconfigurable functional unit [1, 4]. (e) Processor embedded in reconfigurable fabric [7, 8]

III. ARCHITECTURE

Based on the demand and applications different adder combinations can be achieved. In this paper course grained structure is proposed. Different Adders like RCA, CLA, CSLA, CBA are combined to achieve reconfigurable designs. These adder variants are featured to form the combinations and result in the hybrid architectures for the applications that require variable performance. The reconfigurable architectures can be developed based on the requirements of the applications and their limitation with the design restriction. The performance limitation may be the low power, less area, high performance or the balanced constraints. The conventional architectures provide the better results with improvement in the above mentioned constraints. In this paper, proposed architectures create the space to emerge with new corners by providing the reduced power with same/reduced area and performance for the reconfigurable architectures.

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Several reconfigurable architectures have been designed and illustrated to provide better results. Different combinations of adder variants are designed to bring the reconfigurability between the architectures for the particular applications. These reconfigurable architectures can be utilized where the application needs ultra low power in terms of leakage, high performance, low area, and a balanced design quality metrics so that the trade-off is at acceptable value while improving the particular quality metrics. The conventional reconfigurable architectures are designed to be of 8 bit wide and are compared with same conceptualized reconfigurable adder architecture. The proposed architectures are different from the conventional reconfigurable architectures in the way they are being implemented. They are developed based on the concept of partitioning, where the 8 bit architecture is divided in to two 4 bit architectures without altering the functionality of the design. The sharing of adder logics is done instead of replicating the design which enhances performance. Distribution of logics among the adder variants reduces the quantity of area required for the design and contributes directly in reducing the power consumption of the design.

Different adder combinations are proposed in this paper.

Following Fig. 2 and Fig. 9 show the schematics of the conventional and the proposed reconfigurable architectures, captured after synthesis using the Synopsys DC synthesis tool. Fig. 2 to Fig. 9 show the architectures of the conventional and proposed reconfigurable adder architectures respectively. The conventional adder architectures consist of both variants with 8 bit width, whose outputs are multiplexed depending on the control signal of the multiplexer i.e. required adder variant.

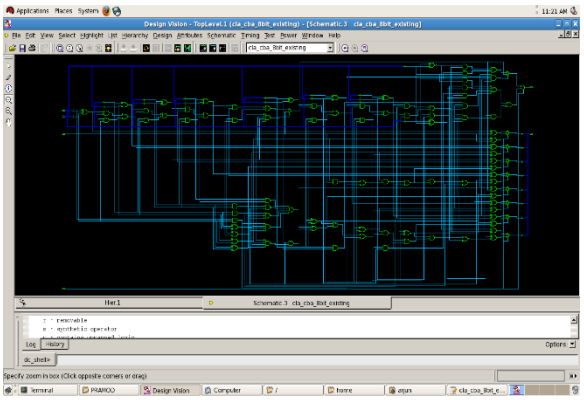

Figure 2: A conventional Carry Bypass- Carry Look-ahead reconfigurable adder architecture

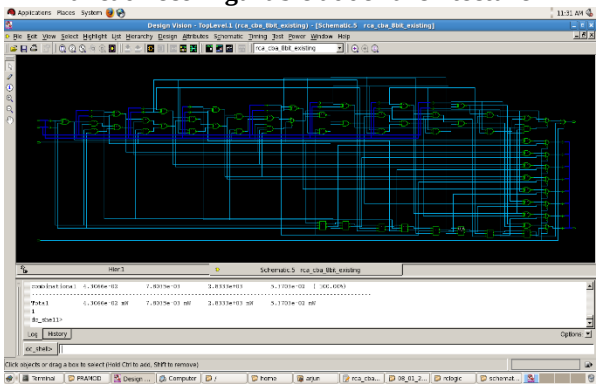

Figure 3: A conventional Ripple Carry - Carry Bypass reconfigurable adder architecture

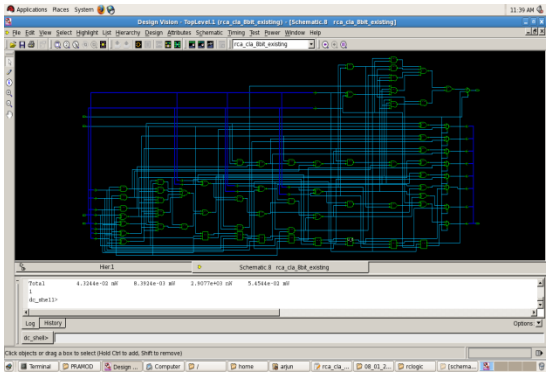

Figure 4: A conventional Ripple Carry - Carry Look-ahead reconfigurable adder architecture

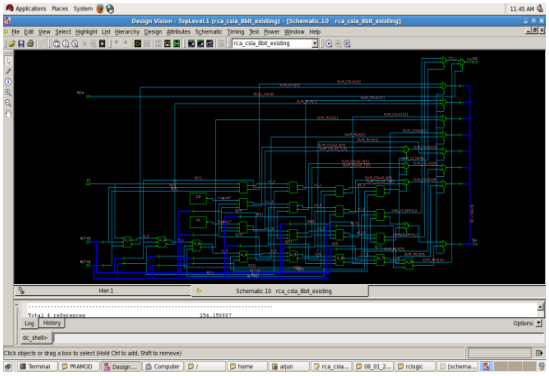

Figure 5: A conventional Ripple Carry - Carry Select reconfigurable adder architecture

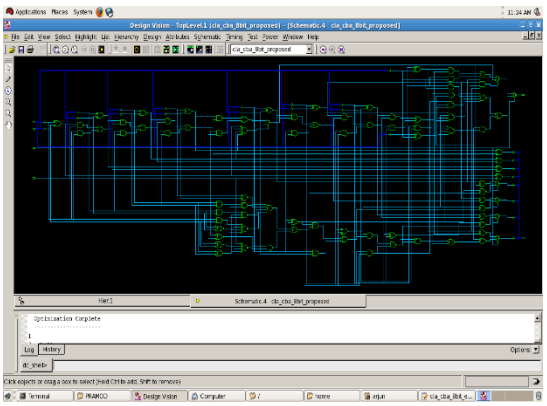

Figure 6: A proposed Carry Bypass- Carry Look-ahead reconfigurable adder architecture

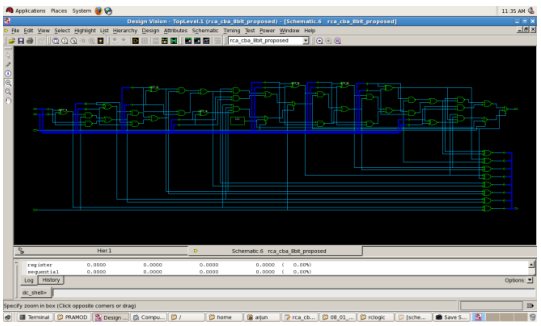

Figure 7: A proposed Ripple Carry - Carry Bypass reconfigurable adder architecture

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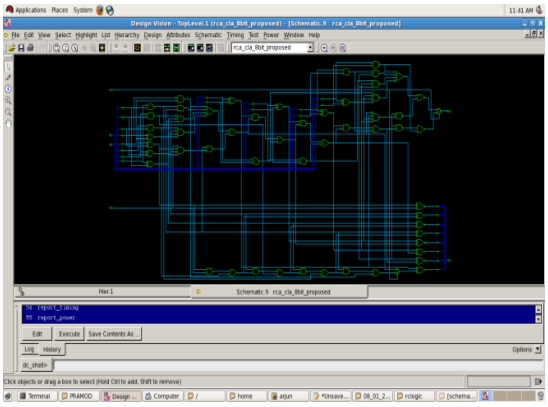

Figure 8: A proposed Ripple Carry - Carry Look-ahead reconfigurable adder architecture

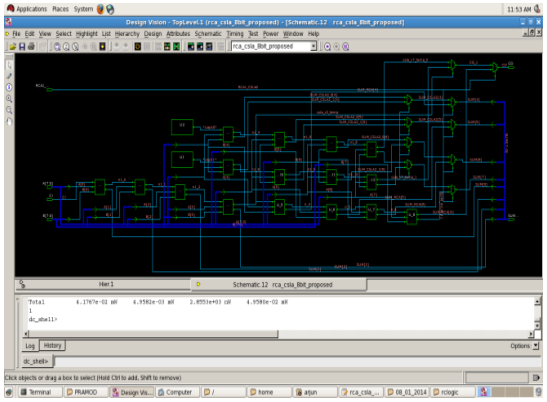

Figure 9: A proposed Ripple Carry - Carry Select reconfigurable adder architecture

But the proposed architecture uses the concepts of sharing and partitioning to arrive at the reconfigurability among the architectures. These designs utilizes reduced power and die area for the designs, while trade off with the performance and extra logic for some of the reconfigurable combinations.

IV. IMPLEMENTATION

The Synopsis tool is utilized for synthesis of existing and proposed reconfigurable designs. The functionality of the designs is verified using Mentor graphics waveform editor. Benchmarking of the proposed technique is done with standard ASIC. Fig.10 to Fig.12 illustrates steps involved in simulation and steps to obtain netlist.

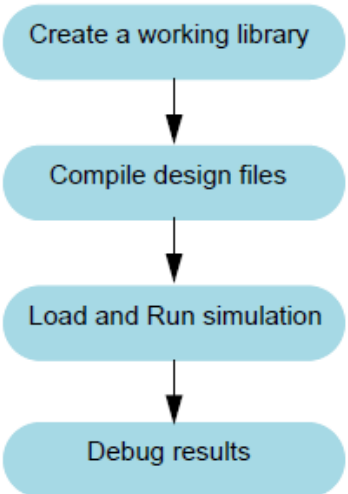

Figure 10: Steps for simulation

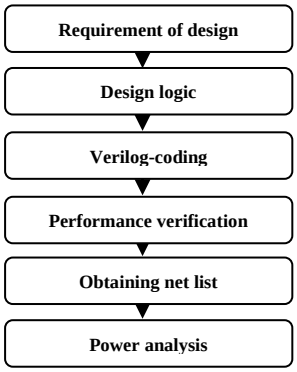

Figure 11: A Typical VLSI Synthesis Flow

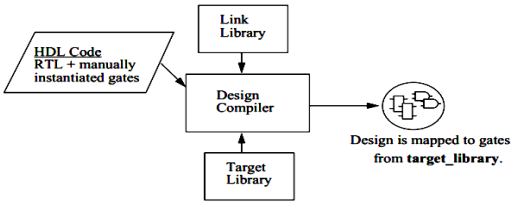

Figure 12: Steps to obtain net list

The tool used for functional verification is Modelsim. Working library is designed and the required design is uploaded in it. By activating the higher end model of the design simulator is loaded. The required results are debugged and verified.

V. RESULTS AND DISCUSSIONS

The tabulated results are obtained after the synthesis as per the above mentioned test set-up; are shown in Table I. The inputs are applied and the simulation is done targeting 65nm technological node. The performance metrics is enhanced by obtaining optimum design parameters.

Fig. 13 to Fig 18 shows the simulation results of all the proposed reconfigurable adder architectures. Table 1 to Table 3 evaluates the performance of existing and proposed designs. The novelty of the proposed design is reflected reduced area and power improvement mentioned in table III. If the hardware requirement is reduced the dynamic switching activity can be achieved. The switching activity reduction will enhance the power optimization. Hence the ideal architectures can be shared between adder architecture to obtain area and power reduction.

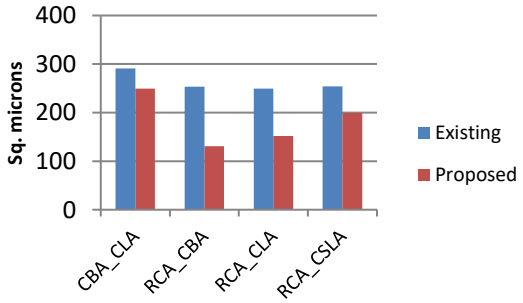

Figure 13: AREA consumed by the Existing and proposed reconfigurable adder architectures

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Figure 14: Performance chart of the Existing and proposed reconfigurable adder architectures

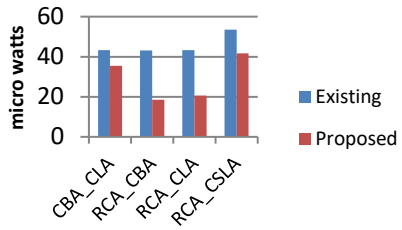

Figure 15: Internal Power of the Existing and proposed reconfigurable adder architectures

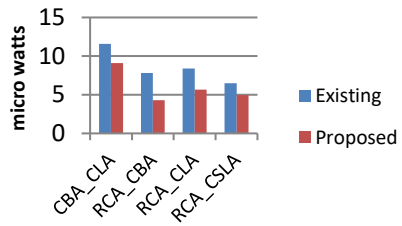

Figure 16: Switching Power of the Existing and proposed reconfigurable adder architectures

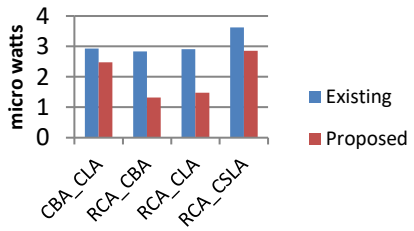

Figure 17: Leakage Power of the Existing and proposed reconfigurable adder architectures

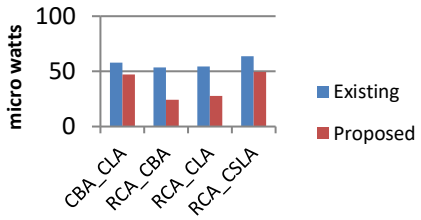

Figure 18: Total Power of the Existing and proposed reconfigurable adder architectures

Table 1: Evaluation of Conventional and Proposed Carry Bypass- Carry Look-ahead reconfigurable adder architecture

Parameters	Conventional	Proposed	% gain
Area (sq. microns)	290.88	249.12	14.35
Timing (ns)	1.16	1.10	5.17
Internal power (uW)	43.315	35.49	18.06
Switching power (uW)	11.585	9.101	21.44
Total Dynamic power (uW)	54.9	44.591	18.77
Leakage power (uW)	2.925	2.48	15.21
Total Power (uW)	57.825	47.071	18.59

Table 2: Comparison of Conventional and Proposed Ripple Carry - Carry Bypass reconfigurable adder architecture

Parameters	Conventional	Proposed	% gain
Area (sq. microns)	253.43	130.68	44.49
Timing (ns)	1.16	1.1	5.17
Internal power (uW)	43.065	18.591	56.83
Switching power (uW)	7.803	4.286	45.06
Total Dynamic power (uW)	50.869	22.877	55.02
Leakage power (uW)	2.833	1.3163	53.54
Total Power (uW)	53.702	24.194	54.94

Table 3: Comparison of Conventional and Proposed Ripple Carry - Carry Look-ahead reconfigurable adder architecture

Parameters	Conventional	Proposed	% gain
Area (sq. microns)	249.12	151.92	39.01
Timing (ns)	0.85	0.83	2.35
Internal power (uW)	43.2442	20.587	52.39
Switching power (uW)	8.3924	5.651	32.66
Total Dynamic power (uW)	51.6366	26.238	49.18
Leakage power (uW)	2.9077	1.476	49.21
Total Power (uW)	54.5443	27.715	49.18

VI. CONCLUSION

The proposed design uses various adder combinations to achieve reduced die area and power consumption. An area reduction of 14 to 44% and power reduction of 18 to 54% is achieved. Benchmarking and verification of the proposed technique is done with standard ASIC. Synopsis design tool is used to simulate and synthesis the existing and proposed design for 65nm technology. Multiplexing has been done in the proposed architecture which effectively utilizes the hardware and reduces area and power. These proposed techniques can be used in design constrained circuits. The proposed method addresses the design tradeoffs. More fine grained and improved design space can be achieved in the proposed techniques. These proposed design can be can be implemented for higher levels abstractions.

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