A Novel Eleven-Level Inverter Employing One Voltage Source and Reduced Components as High Frequency AC Power Source

D.Rajalakshmi, R.Mahalakshmi, K.Praveenraj

Abstract: ***This work is based on a multi-level inverter novel te chnique for multilevel output voltage. The implementation of this topology is built on capacitor switching method and the output levels count is calculated from the sum of capacitor switching cells. One DC voltage source or from solar panel is used and the capacitor voltage balancing problem can be avoided .This model can be enhanced with higher rating and also it has simple gate driver circuit due to reduced number of switches. Operating norm of this multilevel inverter and modulation techniques are also presented and performance of the inverter with existing technology is also discussed with proposed work. The proposed eleven level multilevel inverter is modeled using Matlab/simulink and results are presented, also compared with existing reduced level inverter topology.***

Key words: Multi level inverter, AC power source, simulation

I. INTRODUCTION

Most of the industrial applications and energy sources are renewable such as photovoltaic, wind, and fuel cells. Typical three-level inverters have difficulty to meet the requirements for sinusoidal waveforms and reduced distortion factor [1] .So for high power quality conditions multilevel inverters can be used as an alternative [2]. Approximate sinusoidal staircase output voltage waveforms, decreased change in voltage stresses and operation with low switching frequency stress are the important features of this multilevel inverter[3][4].

Multilevel inverters is receiving more attention because of the quality output. As a result different topologies which are classified into the 3 categories such as neutral point clamped, H-bridge cascade, flying capacitors and wide variety of control strategies are introduced. Such inverters are playing very major role.

For high quality ac power supplies and motor drives, some multilevel inverter topologies are introduced which cannot be qualified to the traditional system and mentioned 3 classifications [5]. A topology is proposed with multiple detached dc voltage sources are required still. Coupled-inductor technique is used in multilevel inverter. These structures are simplified but expansion is difficult to higher levels applications. But proposed multilevel topology can be extended [6].But the usage of excess number of active devices leads increased cost and component numbers in terms of gate driver circuits and the overall system. Also SC technique, a novel multilevel inverter topology can be connected to a multilevel DC-DC converter and a full bridge converter [7][8].

With the proposed topology, one DC voltage source is desired and other difficulties such as balancing of voltage, active switches count and complex gate driver circuits can be avoided. The key point of topology is the DC-DC conversion section which is calculated by the SC cells [9]. Each single SC cell consists of a capacitor, two diodes and an active switch. At the same time, the levels of output voltage of this inverter could be varied by employing different number of SC cells flexibly.

II. SYSTEM MODEL & CONTROL STRATEGY

The proposed eleven Level multi-level inverter block diagram is shown in Fig 1

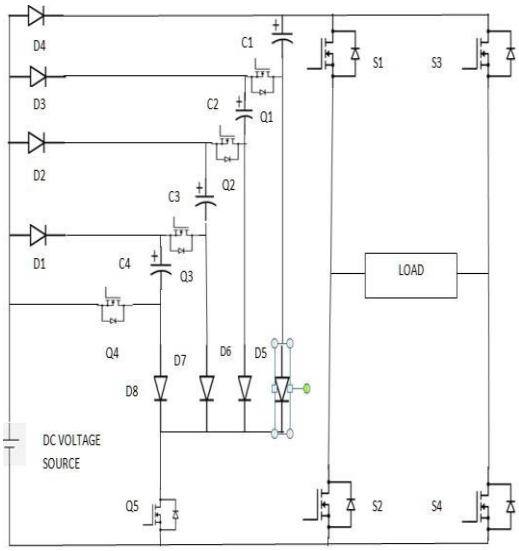

Fig 1. Proposed 11 level multi-level inverter

III. CIRCUIT DESCRIPTIONS AND STATE ANALYSIS

This inverter is developed with combination of full bridge inverter and a DC-DC multilevel converter. Here DC-DC converter consists of the 9 switches [10]-[12], it gives eleven voltage levels according to states of switches. On this multilevel inverter, based on the H bridge operation,

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a sum of eleven voltage stages can be formed, i.e. *0*, $\pm V_{in}$, $\pm 2V_{in}$,..., $\pm(n+1)V_{in}$.. The following assumptions have been made without loss of analysis of output.

--The switched capacitors value Ci are high enough and so that negligible voltage swells across them.

--Each switching device in this inverter are ideal, lead to negligible on-state-run voltage potential and resistance.

--The power source in input side V_{in} should be ideal, lead to constant and no sequence impedance.

A. *First Level Output*

When the switch *Q5* is switched on and Qi (*i=1, 2,3,4*) is switched off, at the same time diodes D1,D2,D3,D4 are conducting and the capacitance are charging (C1,C2,C3,C4). For the H bridge, switches *S1* and *S4* are switched on instantaneously *S2* and *S3* are maintained off state. The voltage V_{in} is from the input power connected to load directly.

B. *Second level output*

When the switch *Q1* is switched on Q_i (*i= 2,3,4,5*) is switched off, at the same time diodes D3,D4 are in conducting and the capacitances (C1,C2,C3,C4) are charging. For the H bridge, switches *S1* and *S4* are switched ON whereas *S2* and *S3* maintained as OFF state. The voltage V_{in} is from the input power directly connected to the load.

C. *Third level output*

When the switch *Q1* and Q2 are switched on and *Qi* (*i=3,4,5*) is in off then diodes D2,D3,D4 are in conduction state and the capacitance C3,C4 are charging. For the H bridge, switches *S1* and *S4* are switched on whereas *S2* and *S3* maintained in off state. The voltage V_{in} is produced by the input power feed the load directly.

D. *Fourth level output*

When the switch *Q1*,Q2 and Q3 are switched on and *Qi* (*i=4, 5*) are in off state then diodes D1,D2,D3,D4 are in conduction state and the capacitance C2,C3,C4 are charging. For the H bridge, switches *S1* and *S4* are switched on whereas *S2* and *S3* maintained in off state. The voltage V_{in} is developed by the input power feed the load directly.

E. *Fifth level output*

When the switch Q1,*Q2,Q3* and Q4 are switched on and *Q5 is in off* then diodes D1,D2,D3,D4 are conducting and the capacitances C1,C2,C3,C4 are charging. For the H-bridge, switches *S1* and *S4* are switched on whereas *S2* and *S3* are maintained as OFF state. The voltage V_{in} is developed by the input power directly connected to load. Fig. 2 to Fig.6 show the connection diagram of all levels.

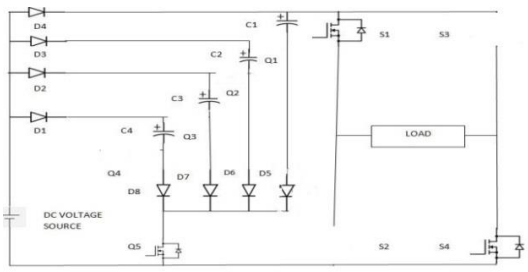

Fig 2. First level output

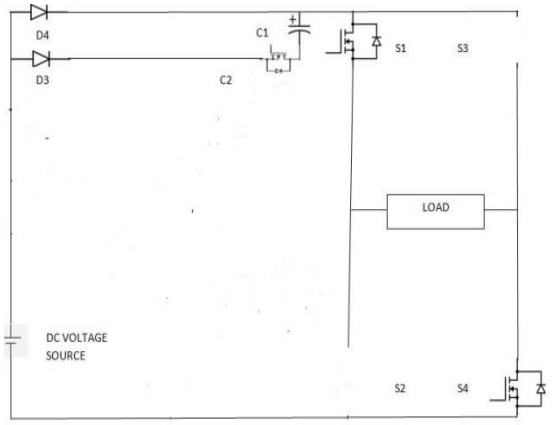

Fig 3. Second stage output

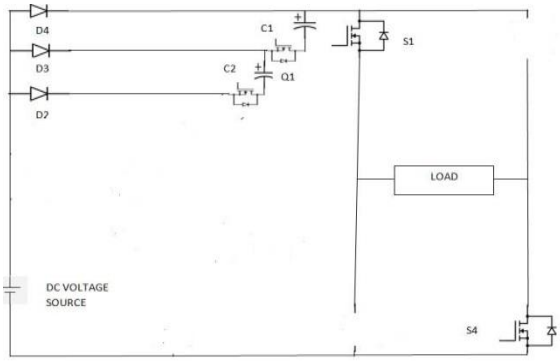

Fig 4. Third stage output

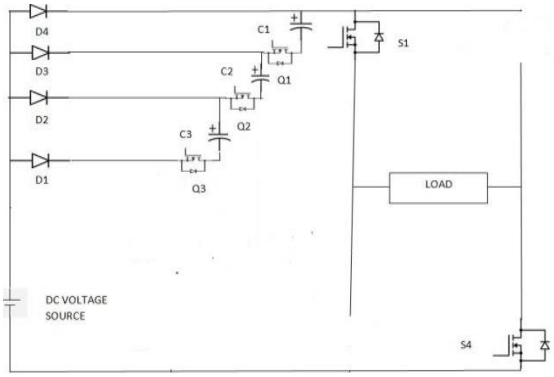

Fig 5. Fourth stage output

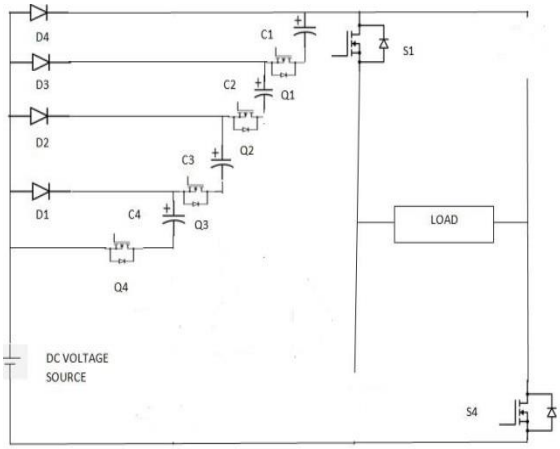

Fig 6. Fifth level output

Voltage level	S1	S2	S3	S4	Q1	Q2	Q3	Q4	Q0 or Q5
5Vdc	1	1	0	0	1	1	1	1	0
4Vdc	1	1	0	0	1	1	1	0	0
3Vdc	1	1	0	0	1	1	0	0	0
2Vdc	1	1	0	0	1	0	0	0	0
1Vdc	1	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1
-1Vdc	0	0	1	1	0	0	0	0	1
-2Vdc	0	0	1	1	1	0	0	0	0
-3Vdc	0	0	1	1	1	1	0	0	0
-4Vdc	0	0	1	1	1	1	1	0	0
-5Vdc	0	0	1	1	1	1	1	1	0

Table 1: Working States Combination For The Proposed Inverter

Table 1 explains the on and off conditions of the switches corresponding to the voltage level.

IV. MODULATION STRATEGIES

To produce the output voltage of multilevel inverters, different modulation strategies are used and it made output as close as possible to the sinusoidal waveform .It is shown in Fig. 7

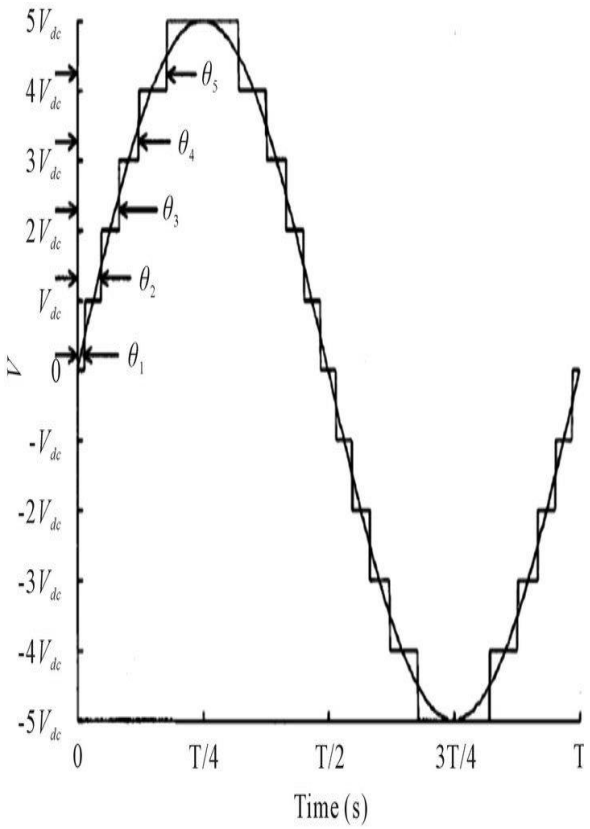

Fig 7 Eleven level output

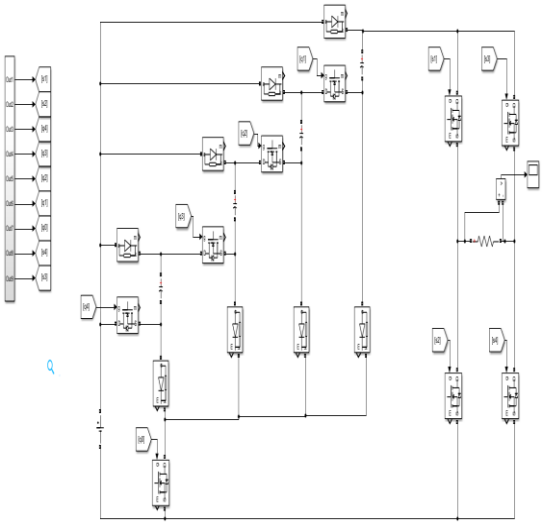

Fig 8 Pulses for inverter

MODES	U	Proposed	Existing
Component Parameters	Forward voltage drop across diodes (VD)	0.8V	0.3V
	On state resistance of switches (Ron)	1mΩ	4.8mΩ
Circuit Parameters	Capacitance value	4700µf	1000µf
	Input DC source (V_{dc})	30V	60V
	Output frequency (Fo)	50HZ	1KHZ
	Load impedance (ZL)	100Ω	32Ω

Table 1 Simulation parameters

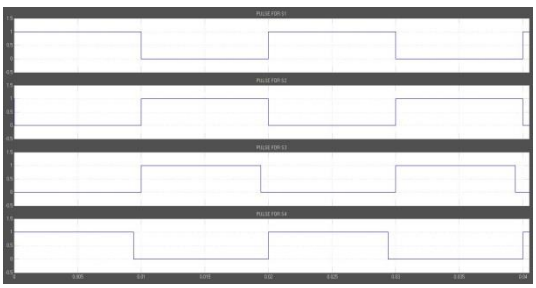

Fig 9 Pulses for Q1 to Q5

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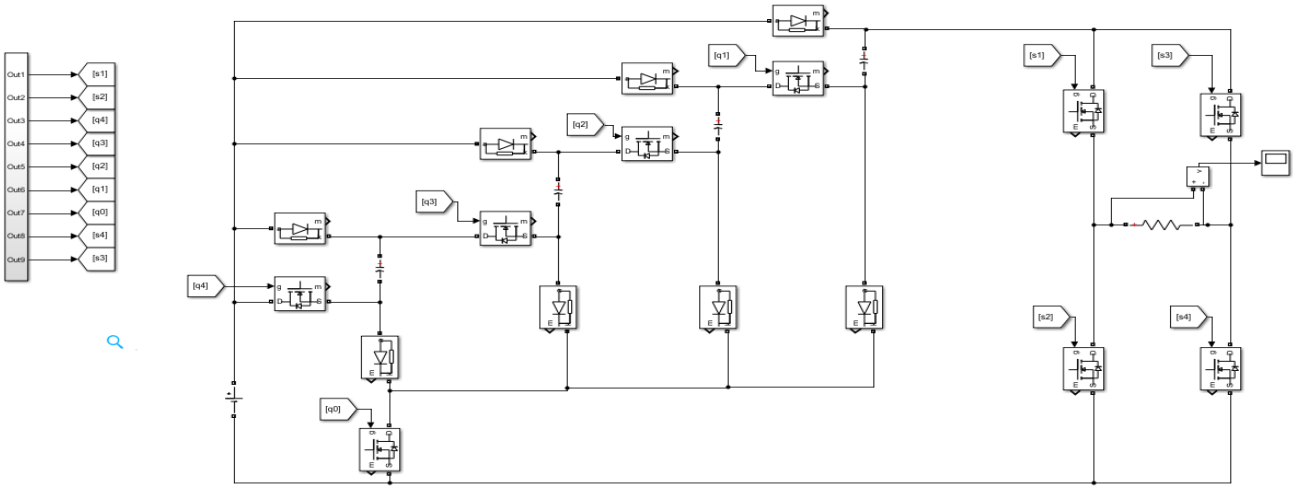

Fig. 10 Simulink model of novel eleven multi-level inverter with one AC source with reduced components.

The Fig 8 and 9 show the pulses given to inverter and switches Q1 to Q5. A converter topology with only voltage source, 9 switches and a flying capacitor was proposed [13]. It can produce output at a anticipated level such as 1/3Vdc when the normal frequency modulation strategy keeps the capacitor voltage with eleven levels exactly. A step-up multilevel topologies which is in series based on switched-capacitor (SC) techniques is proposed

V. SIMULATION MODEL

Fig. 10 shows the simulink model of novel eleven multi level inverter with one AC source with reduced components.

VI. RESULTS & DISCUSSIONS

The matlab model is constructed for existing nine level and proposed eleven level. The results are compared and specifications are shown in Table 2and in Table 1

PARAMETER	9 LEVEL INVERTER	11 LEVEL INVERTER
Peak voltage	124V	172V
Peak current	2.150A	1.175A
THD Value	9.78%	7.58%
Nsource	1	1
Ncap	2	4
Nswitch	9	9
Ndiode	2	8

Table 2 Comparison of proposed system

High frequency AC Source can be introduced, here 50 Hz standard frequency is used. It can also be implemented at low frequency and step level increased from nine levels to eleven levels with some modification in design and it leads to reduced harmonics

The input dc source with load through multilevel inverter with control technique has been supported using matlab/simulink.

The input DC voltage is shown in Fig.11.In this constant power supply is given by the help of DC sources. (solar or Batteries)

The voltage across the H-bridge is shown in Fig.12. The input voltages will be increased according to the requirements.

The five level in the output is observed. Output voltage of the multi-level inverter is shown in Fig.13. The load current is shown in Fig.14.

If the load is resistor, then the output voltage and current are in phase. Voltage and current RMS values obtained are 85.17 V and 2.66 A respectively. For series RL load (Ro = 24Ω, Lo = 3.2mH), thus the voltage leads current with an angle 40°, which is the impedance angle of the inductive load.

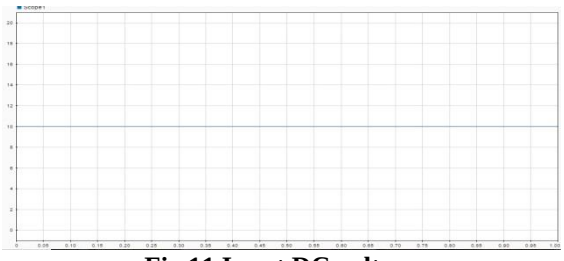

Fig 11 Input DC voltage

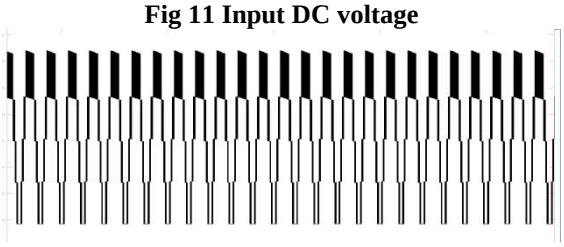

Fig 12 Output of H bridge inverter

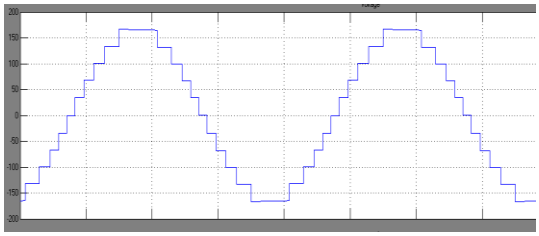

Fig13 Output voltage

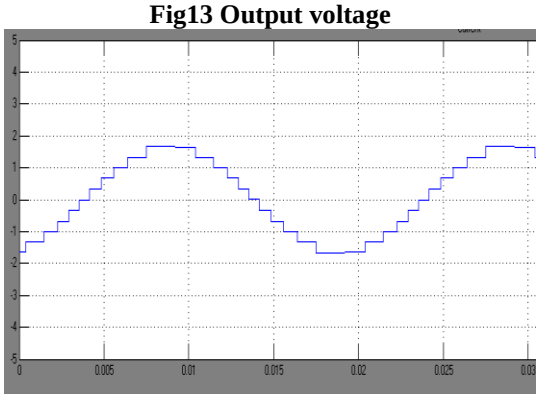

Fig 14 Output current

VII.ANALYSIS OF THD VALUE

Integral multiple of the fundamental frequency are the harmonics. When the current and voltage are distorted from sinusoidal waveforms it indicates the harmonics presence. [14].

Total harmonic distortion values five level inverters (>10%) and nine level (>5%) are found to be high [15]. So eleven level inverter is proposed to reduce the total harmonic distortion and to make the output voltage more sinusoida . Analysis of THD values are shown in the graph.

The number of level increases, THD can be reduced. In existing system THD is 9.78% and the proposed inverter THD is 7.58% FFT analysis is shown in Fig .15

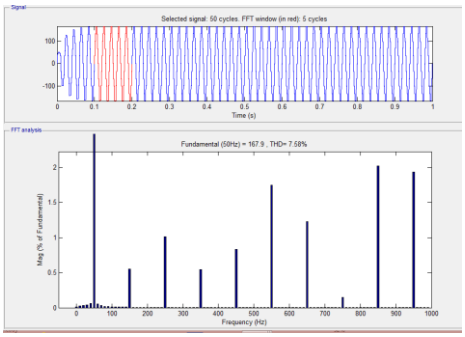

Fig 15 FFT analysis of output voltage

VIII.CONCLUSION AND FUTURE SCOPE

In this paper switched-capacitor step-up multilevel inverter which is consists of a multilevel DC-DC converter and full bridge is introduced. The DC-DC conversion contains multiple switched-capacitor cells. The output voltage level is varied flexibly by connecting numerous SC cells, It has been analyzed that this inverter gives eleven levels in the output using only 4 capacitors and 9 switches which are active devices. So it leads to the simple assembly and little cost of the gate driver circuits.

High switching and fundamental switching frequency modulation methods are discussed for this swapped capacitor multilevel inverter. The logic for Multi-carrier modulating circuit is designed and modelled for the inverter using Matlab. With analysis of THD the performance and operation of this eleven level inverter are verified. In future it is extended toe level of output further and it can also be verified using experimental setup.[17] The optimization algorithm will be also introduced to improve the output performance further.[16].It can also be verified with solar system with different load conditions.[18]

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