A Novel Eleven-Level Inverter Employing One Voltage Source and Reduced Components as High Frequency AC Power Source

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Abstract: This work is based on a multi-level inverter novel technique for multilevel output voltage. The implementation of this topology is built on capacitor switching method and the output levels count is calculated from the sum of capacitor switching cells. One DC voltage source or from solar panel is used and the capacitor voltage balancing problem can be avoided. This model can be enhanced with higher rating and also it has simple gate driver circuit due to reduced number of switches. Operating norm of this multilevel inverter and modulation techniques are also presented and performance of the inverter with existing technology is also discussed with proposed work. The proposed eleven level multilevel inverter is modeled using Matlab/Simulink and results are presented, also compared with existing reduced level inverter topology.

Key words: Multi level inverter, AC power source, simulation

I. INTRODUCTION

Most of the industrial applications and energy sources are renewable such as photovoltaic, wind, and fuel cells. Typical three-level inverters have difficulty to meet the requirements for sinusoidal waveforms and reduced distortion factor [1]. So for high power quality conditions multilevel inverters can be used as an alternative [2]. Approximate sinusoidal staircase output voltage waveforms, decreased change in voltage stresses and operation with low switching frequency stress are the important features of this multilevel inverter[3][4].

Multilevel inverters is receiving more attention because of the quality output. As a result different topologies which are classified into the 3 categories such as neutral point clamped, H-bridge cascade, flying capacitors and wide variety of control strategies are introduced. Such inverters are playing very major role.

For high quality ac power supplies and motor drives, some multilevel inverter topologies are introduced which cannot be qualified to the traditional system and mentioned 3 classifications [5]. A topology is proposed with multiple detached dc voltage sources are required still. Coupled-inductor technique is used in multilevel inverter. These structures are simplified but expansion is difficult to higher levels applications. But proposed multilevel topology can be extended [6]. But the usage of excess number of active devices leads increased cost and component numbers in terms of gate driver circuits and the overall system. Also SC technique, a novel multilevel inverter topology can be connected to a multilevel DC-DC converter and a full bridge converter [7][8].

With the proposed topology, one DC voltage source is desired and other difficulties such as balancing of voltage, active switches count and complex gate driver circuits can be avoided. The key point of topology is the DC-DC conversion section which is calculated by the SC cells [9]. Each single SC cell consists of a capacitor, two diodes and an active switch. At the same time, the levels of output voltage of this inverter could be varied by employing different number of SC cells flexibly.

II. SYSTEM MODEL & CONTROL STRATEGY

The proposed eleven Level multi-level inverter block diagram is shown in Fig 1.

![Fig 1. Proposed 11 level multi-level inverter](image_url)

III. CIRCUIT DESCRIPTIONS AND STATE ANALYSIS

This inverter is developed with combination of full bridge inverter and a DC-DC multilevel converter. Here DC-DC converter consists of the 9 switches [10]-[12], it gives eleven voltage levels according to states of switches. On this multilevel inverter, based on the H bridge operation,
a sum of eleven voltage stages can be formed, i.e. 0, ±V_{in},
±2V_{in}, ..., ±(n+1)V_{in}. The following assumptions have been
made without loss of analysis of output.

--The switched capacitors value C_i are high enough and
so that negligible voltage swells across them.

--Each switching device in this inverter are ideal, lead to
negligible on-state-run voltage potential and resistance.

--The power source in input side V_{in} should be ideal, lead
to constant and no sequence impedance.

A. First Level Output

When the switch Q_5 is switched on and Q_i (i=1, 2, 3, 4) is
switched off, at the same time diodes D_1, D_2, D_3, D_4 are
conducting and the capacitance are charging (C_1, C_2, C_3, C_4).
For the H bridge, switches S_1 and S_4 are switched on
instantaneously S_2 and S_3 are maintained off state. The
voltage V_{in} is from the input power connected to load
directly.

B. Second level output

When the switch Q_1 is switched on Q_i (i= 2, 3, 4, 5) is
switched off, at the same time diodes D_3, D_4 are in
conducting and the capacitance (C_1, C_2, C_3, C_4) are
charging. For the H bridge, switches S_1 and S_4 are switched ON
whereas S_2 and S_3 maintained as OFF state. The voltage V_{in} is from the input power directly connected to the load.

C. Third level output

When the switch Q_1 and Q_2 are switched on and Q_i
(i=3, 4, 5) is in off then diodes D_2, D_3, D_4 are in
conduction state and the capacitance C_3, C_4 are charging. For the H
bridge, switches S_1 and S_4 are switched on whereas S_2 and S_3 maintained in off state. The voltage V_{in} is produced by
the input power feed the load directly.

D. Fourth level output

When the switch Q_1, Q_2 and Q_3 are switched on and Q_i
(i=4, 5) are in off state then diodes D_1, D_2, D_3, D_4 are in
conduction state and the capacitance C_2, C_3, C_4 are charging.
For the H bridge, switches S_1 and S_4 are switched on
whereas S_2 and S_3 maintained in off state. The voltage V_{in} is developed by the input power feed the load directly.

E. Fifth level output

When the switch Q_1, Q_2, Q_3 and Q_4 are switched on and Q_5
is in off then diodes D_1, D_2, D_3, D_4 are conducting and
the capacitance C_1, C_2, C_3, C_4 are charging. For the H
bridge, switches S_1 and S_4 are switched on whereas S_2 and S_3 are maintained as OFF state. The voltage V_{in} is developed by the input power directly connected to load. Fig. 2 to Fig.6 show the connection diagram of all levels.
Table 1: Working States Combination For The Proposed Inverter

Table 1 explains the on and off conditions of the switches corresponding to the voltage level.

IV. MODULATION STRATEGIES

To produce the output voltage of multilevel inverters, different modulation strategies are used and it made output as close as possible to the sinusoidal waveform. It is shown in Fig. 7

<table>
<thead>
<tr>
<th>Voltage level</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q5 or Q0</th>
</tr>
</thead>
<tbody>
<tr>
<td>5Vdc</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4Vdc</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3Vdc</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2Vdc</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>0</td>
</tr>
<tr>
<td>1Vdc</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0VDC</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>-1Vdc</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>-2Vdc</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-3Vdc</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-4Vdc</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-5Vdc</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1 Simulation parameters

<table>
<thead>
<tr>
<th>MODES</th>
<th>U</th>
<th>Proposed</th>
<th>Existing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Parameters</td>
<td>Forward voltage drop across diodes (V_D)</td>
<td>0.8V</td>
<td>0.3V</td>
</tr>
<tr>
<td>On state resistance of switches (R_{on})</td>
<td>1mΩ</td>
<td>4.8mΩ</td>
<td></td>
</tr>
<tr>
<td>Circuit Parameters</td>
<td>Capacitance value</td>
<td>4700µf</td>
<td>1000µf</td>
</tr>
<tr>
<td>Input DC source (V_{dc})</td>
<td>30V</td>
<td>60V</td>
<td></td>
</tr>
<tr>
<td>Output frequency (F_o)</td>
<td>50HZ</td>
<td>1KHZ</td>
<td></td>
</tr>
<tr>
<td>Load impedance (Z_L)</td>
<td>100Ω</td>
<td>32Ω</td>
<td></td>
</tr>
</tbody>
</table>
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The Fig 8 and 9 show the pulses given to inverter and switches Q1 to Q5. A converter topology with only voltage source, 9 switches and a flying capacitor was proposed [13]. It can produce output at a anticipated level such as 1/3Vdc when the normal frequency modulation strategy keeps the capacitor voltage with eleven levels exactly. A step-up multilevel topologies which is in series based on switched-capacitor (SC) techniques is proposed

V. SIMULATION MODEL

Fig. 10 shows the simulink model of novel eleven multi-level inverter with one AC source with reduced components.

VI. RESULTS & DISCUSSIONS

The matlab model is constructed for existing nine level and proposed eleven level. The results are compared and specifications are shown in Table 2 and in Table 1

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>9 LEVEL INVERTER</th>
<th>11 LEVEL INVERTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak voltage</td>
<td>124V</td>
<td>172V</td>
</tr>
<tr>
<td>Peak current</td>
<td>2.150A</td>
<td>1.175A</td>
</tr>
<tr>
<td>THD Value</td>
<td>9.78%</td>
<td>7.58%</td>
</tr>
<tr>
<td>Nsource</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Ncap</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Nswitch</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>Ndiode</td>
<td>2</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 2 Comparison of proposed system

The input dc source with load through multilevel inverter with control technique has been supported using matlab/simulink.

The input DC voltage is shown in Fig.11. In this constant power supply is given by the help of DC sources. (solar or Batteries)

The voltage across the H-bridge is shown in Fig.12. The input voltages will be increased according to the requirements.

The five level in the output is observed. Output voltage of the multi-level inverter is shown in Fig.13. The load current is shown in Fig.14.

If the load is resistor, then the output voltage and current are in phase. Voltage and current RMS values obtained are 85.17 V and 2.66 A respectively. For series RL load (Ro = 24Ω, Lo = 3.2mH), thus the voltage leads current with an angle 40°, which is the impedance angle of the inductive load.

Fig 11 Input DC voltage

Fig 12 Output of H bridge inverter

High frequency AC Source can be introduced, here 50 Hz standard frequency is used. It can also be implemented at low frequency and step level increased from nine levels to eleven levels with some modification in design and it leads to reduced harmonics.
VIL ANALYSIS OF THD VALUE

Integral multiple of the fundamental frequency are the harmonics. When the current and voltage are distorted from sinusoidal waveforms it indicates the harmonics presence.

Total harmonic distortion values five level inverters (>10%) and nine level (>5%) are found to be high [15]. So eleven level inverter is proposed to reduce the total harmonic distortion and to make the output voltage more sinusoidal. Analysis of THD values are shown in the graph.

The number of level increases, THD can be reduced. In existing system THD is 9.78% and the proposed inverter THD is 7.58% FFT analysis is shown in Fig. 15.

VIII. CONCLUSION AND FUTURE SCOPE

In this paper switched-capacitor step-up multilevel inverter which is consists of a multilevel DC-DC converter and full bridge is introduced. The DC-DC conversion contains multiple switched-capacitor cells. The output voltage level is varied flexibly by connecting numerous SC cells, It has been analyzed that this inverter gives eleven levels in the output using only 4 capacitors and 9 switches which are active devices. So it leads to the simple assembly and little cost of the gate driver circuits.

High switching and fundamental switching frequency modulation methods are discussed for this swapped capacitor multilevel inverter. The logic for Multi-carrier modulating circuit is designed and modelled for the inverter using Matlab. With analysis of THD the performance and operation of this eleven level inverter are verified. In future it is extended toe level of output further and it can also be verified using experimental setup.[17] The optimization algorithm will be also introduced to improve the output performance further.[16].It can also be verified with solar system with different load conditions.[18]

REFERENCES


