FPGA Implementation of Discrete Phase Locked Loop with No Dead Zone

Bharanidharan N, D.Preethi, Baranidharan V

Abstract— A discrete phase locked loop with dead zone avoidance based on FPGA is implemented and validated for better results. The null dead zone is actually achieved by using less complex design of discrete PLL with full phase lock-in-range which is efficient in terms of area followed by a reference signal and NCO at the output. The major contribution of this paper is full phase tracking-range which is achieved by using novel simple equation instead of a loop filter. The overall system is simulated for validation using Xilinx ISE and its functionality is verified in DPLL for analysis. Also the parameters such as phase tracking time and phase tracking- range performance are measured.

Keywords— FPGA, PLL, CORDIC

I. INTRODUCTION

A wide range of applications has evolved from 1930's pertaining to the concepts of phase locked loop (PLL) in communication systems. The various applications include synchronizing the digital clock and demodulation as being in digital domain. The digital phase locked loop such as Discrete PLL and their derivatives can be easily implemented using simple algorithms [1]. Thus the proposed structure for no dead zone is limited to digital signals with FPGA implementation. In general, three important blocks of PLL are phase detector, loop filter and Voltage Controlled Oscillator (VCO). The blocks such as Phase detector formed by Hilbert transform and CORDIC (in vector mode) are utilized as phase detector for the generation of reference signal as well as NCO output signal.

The phase lock-in-range is a very important parameter of DPLL and it should be large for better performance. But when the input to DPLL is out of that range, the total system will meet dead lock situation. Hence it is much important to make a DPLL with full phase tracking range. All existing DPLL structure requires a loop filter but loop filter usage makes the limitation for phase lock-in-range. Hence loop filter should be replaced by another suitable block to achieve full phase lock-in-range.

II. PROPOSED DPLL

Two major yet common algorithms used for the generation of analytical signal and instantaneous phase detection are Hilbert transform and vector mode of CORDIC algorithm respectively. The PI controller to behave as a loop filter with characteristics of a low pass filter in existing structure of discrete phase locked loop [2-3] is replaced with a simple equation to have full phase lock-in-range. Since the controller is comparatively complex for implementation and consumes more area on FPGA, the later proposed overcomes the issue. The phase offset difference between discrete sinusoidal values and reference sinusoidal signal across the NCO output can be computed using simple equation.

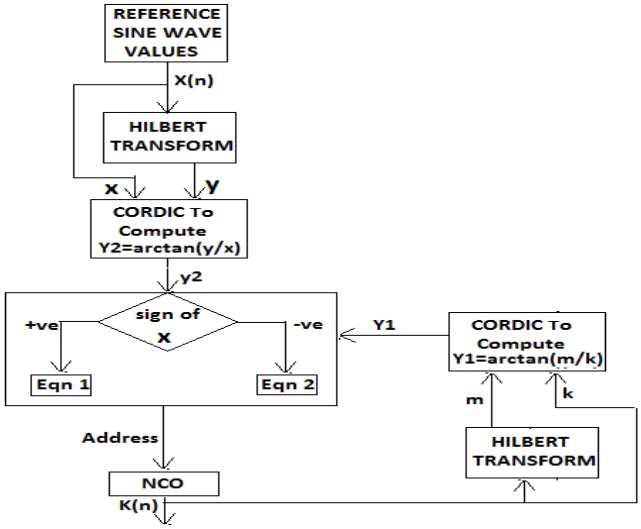

Fig. 1 Flowchart depicting Discrete PLL with no dead zone

To obtain the phase the analytic signal [4], where H{x(n)} represents the Hilbert transform of an input x(n). The corresponding equation can be written as,

$$A(n) = x(n) + jH\{x(n)\} \quad (1)$$

By setting the initial values, the required mathematical function can be performed using the CORDIC iterative equations [5] in rotation mode. The sine wave generated using CORDIC in NCO, with initial values X0=1, Y0=0, and Z0=θ at the end of iterations is as follows:

$$\begin{bmatrix} X_i \\ Y_i \\ Z_i \end{bmatrix} = \begin{bmatrix} cos\theta \\ sin\theta \\ 0 \end{bmatrix} \quad (2)$$

As discussed earlier regarding the generation of phase detection instantaneously using analytic signal of CORDIC in vector mode, initial values of Hilbert transform with X0 = Re{A(n)}, Y0 = Im{Y(n)} and Z0=0 at the end of every iteration is as follows:

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$$\begin{bmatrix} X_i \\ Y_i \\ Z_i \end{bmatrix} = \begin{bmatrix} P\sqrt{\mathrm{Re}\{A(n)\}^2 + \mathrm{Im}\{A(n)\}^2} \\ 0 \\ \arctan\frac{\mathrm{Im}\{A(n)\}}{\mathrm{Re}\{A(n)\}} \end{bmatrix} \quad (3)$$

The NCO in rotation mode can be constructed by using either LUT method or CORDIC algorithm. The step size for the generated sine wave is inversely related to accuracy. Since the realization of intermediate fractional values in FPFA gets tough, the values of sine wave varying from -1 to 1 are multiplied by hence the discrete values now ranges between -100 to 100. Hence to complete a one full cycle, a step size of 15° for both LUT and CORDIC methods with 24 discrete values are needed. i.e., sin0°, sin15°, sin30°,…..sin345° giving rise to 0,25,50,….-25 on multiplying by 100. The value stacked in "LUT Address" varies between 0 and 23. On gradually increasing the address by one at every step, discrete sine values from array in LUT method are used.

A. System implementation: As the calibration values starts ranging from -100 to 100, word sizes are predefined to be eight bits. Approximation based Hilbert transform method is used for ease of implementation as it constitutes a FIR filter for its simplicity. Filter design toolbox of MATLAB is used for easy optimization of desired frequency through computation of the coefficients with least square method. The decrease in the order of Hilbert filter retains phase information whereas the magnitude of filter output gets affected. Thus the minimum order of filter is selected to be 10 and implemented for word size of 8 bits for better results.

In all the aforementioned computations, the discrete values at the output of the sine signal are multiplied with a constant K of value 0.611 from previous six iteration stages. In order to circumvent the percentage error, X0=61(0.611x100=61), Y0=0 and Z0= θ are assigned respectively. Here θ is varied as 0,15,30,45,…,345,0,15.., and henceforth are computed for various values of θ with an instance of each rising edge of clock .

For LUT based sine wave generator:

Equation 1

$$\text{LUT address} = \frac{y2-y1}{\text{step size}} + \frac{y1+90}{\text{step size}}$$

Equation 2

$$\text{LUT address} = \frac{y2-y1}{\text{step size}} + \frac{y1+90}{\text{step size}} + \frac{180}{\text{step size}}$$

For CORDIC based sine wave generator:

Equation 1 Z0 = (y2 - y1) + (90+y1)

Equation 2 Z0 = (y2 - y1) + (90+y1) + 180

The equations 1 and 2 are predominant in computing the address of phase offset in NCO with only y2 but without y1. But y1 is very crucial for achieving the feedback in PLL structure. Both y1 and y2 varies gradually with multiples of step size as -90,-75,…,-15,0,15,…75,90,75,..75(step size= 15) for θ varying from 0,15,30,45,…,345.

III. RESULTS AND DISCUSSION

The proposed discrete PLL implementation is simulated on the target device of xc3s500e-4fg320 using Xilinx Spartan 3E board. In table 2, the already available CORDIC based system [1,3] operated along vector mode is validated over DPLL with overall LUT and CODIC. The results reveal that the area occupied or the device utilization is very less in both the methods.

Table 1. Summary of device utilization for proposed DPLL and CORDIC system

Logic Utilization	LUT based DPLL	CORDIC based DPLL	Existing CORDIC block
No. of Slices	276	421	595
No. of Slice Flip-Flops	313	423	1027
No. of 4-input LUTs	463	759	1160
No. of bonded IOBs	28	28	69
No. of GCLKs	2	2	2
No. of Multipliers	9	9	--

The output of N iteration stages appearing after $(N+1)^{th}$ clock pulses is one of the setbacks of CORDIC algorithm. Apart from that constraint, there is no backlog in accurate output that is produced at every rising edge of clock cycle.

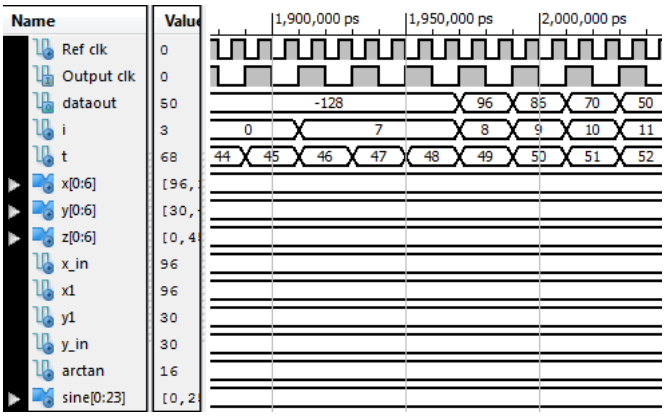

Fig. 2 Results of Discrete PLL Using LUT method

In Fig 2, the reference clock i.e., 'ref clk' is multiplied with '2' giving rise to the clock output of NCO, where the offset address and number of clock pulse are denoted by 'i' and 't' respectively. As in the above scenario, within a clock period of 10 ns, a complete sine wave will be generated on utilizing all the 24 discrete values. Therefore for 4.16 MHz of reference frequency, the time period is measured to be 240ns. Also NCO output frequency will be 02.08 MHz for a time period of 480 ns, with the output clock period of 20ns.

The output frequency of NCO is divided by 2 and frequency be synthesized (Fnco = M x Fref). At reference signal with value of 96 (sin(105°)), the phase offset is 105° followed by output signal at NCO along with phase offset tuning. The Discrete PLL output will be generated after 49th and 55th clock pulse for LUT based DPLL and CORDIC based approaches. The estimated phase lock time is 0.96µs (20ns*48) for the NCO frequency of 2.08 MHz in LUT.

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Even though the output frequency is 1 KHz of NCO, the phase lock time of 2ms & 2.45 ms will be synthesized for LUT & CORDIC based DPLL respectively.

From Fig.3, the observed inference is that as the frequency increases appropriately the phase lock time reduces. The validation of DPLL pertaining for the performance parameters such as lock-in-range and phase offset difference is verified and without dead zone over any number of frequencies with similar efficiency as before approaches.

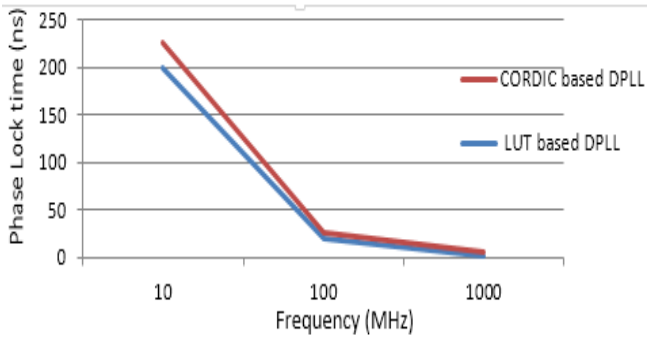

Fig. 3 Analysis of Discrete PLL with respect to time for phase tracking

IV. CONCLUSION

An accurate and impressive analysis of discrete PLL of all phase tracking-range is simulated under every possible constraint. From the summary on device utilization, it is observed that the proposed technique occupies very less area when compared against the previous approaches of PLL. All the existing DPLL structure requires the loop filter but simple equation for DPLL has removed dead zone without any compromise in the accuracy of DPLL and also phase lock time is very less especially when the range of step size drops below 15°. Owing to the following parameters, CORDIC based system is preferred for sine wave generation in terms of area required for memory allocation. The percentage of error is 2.42% for CORDIC based DPLL.

V. REFERENCES

1. Abhiskek Das, Suraj Dash, B.Chitti Babu, A.K.Sahoo, ‘A Novel Phase Detection System for Linear All-Digital Phase Locked Loop’ IEEE Students’ Conference on Engineering & Systems (SCES 2012), MNNIT, Allahabad, pp.1-6, 2012
2. Martin Kumm, Harald Klingbeil, and Peter Zipf, Member, ‘An FPGA-Based Linear All-Digital Phase-Locked Loop’ IEEE Transaction on Circuits Systems I, Regular paper, vol. 57, no. 9, Sept. 2010, pp.2487-2497
3. Abhiskek Das, Suraj Dash, B.Chitti Babu, A.K.Sahoo, ‘Design and Implementation of FPGA based Linear All Digital Phase-Locked Loop’ 2012 Annual IEEE, Kochi, pp.280 to 285
4. M.Kumm and M. S. Sanjari, ‘Digital Hilbert transformers for FPGA-based phase-locked loops’ International Conference on Field Programmable Logic and Applications, pp. 251–256, 2008
5. J. E. Volder, ‘The CORDIC trigonometric computing technique’ IRE Trans. Electron. Comput, vol. 8, no. 3, pp. 330–334, Sep. 1959

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