Performance Comparison of JL FinFETs with Variability in Fin Structure and Shape

Ayoob Khan T. E, Shahna M, Shahul Hameed T. A.

Abstract*: *To avoid the scaling challenges of CMOS the Junctionless transistors (JLT) has recently been proposed. Unlike conventional transistors, JLT have no junctions i.e source/drain /channel regions are uniformly doped with same species and that is the main advantage of JLT. In this study, the impact of work function variation(WFV), spacer dielectric, material engineering on the performance of conventional P channel Junctionless FinFET is analyzed. Trapezoidal and Multifin structures of JL FinFETs are proposed and same impact is considered under similar conditions at supply voltage -0.9 V. All studies are carried out using Silvaco Atlas TCAD tool. The basic performance parameters under consideration are off current ,VTH, SS & ION/IOFF ratio and observed characteristics fluctuations on the devices. The proposed architecture shows better short channel characteristics and also provides better ION/IOFF ratio compared to conventional JL FinFET.

Index Terms*: *JL FinFET, Spacer Dielectric, Sub threshold Slope, Work Function Variation

I. INTRODUCTION

In conventional MOSFETs scaling of channel length leads to severe critical challenges, such as the requirement to minimize short channel effects, to have higher ON current, low leakage current, to minimize power consumption. Many approaches for eradicating these issues have been came into existence. High-k metal gate technology, strain engineering and evolution of multigate structures such as FinFET & nanowire structures have been introduced. FinFETs, due to their quasiplanar structure are compatible with existing CMOS technology. To reduce the short channel effects and to avoid the challenges and difficulties in the device fabrication, a junction less transistor (JLT) has recently been proposed [1]. JL transistors require high channel doping in the range of 10191020cm-3.The main advantages of junction less FinFET over conventional FinFET is that it have i) no doping concentration gradient ii)better scalability iii)better immune to short channel effects iv)low leakage current v)simplified fabrication process. (JLT) comes into existence. This device is a multigate transistor without any junctions which yields better scalability and immune to short channel effects. Since they do not have junctions, the process is highly simplified and it reduces the need for ultrafast annealing techniques. Junctionless transistors (JLT) is simply a resistor i.e. the gate voltage can control the drive current. The most important characteristics of device performance are I_{ON},I_{OFF},I_{ON}/I_{OFF} ratio, V_{TH} and sub threshold swing(SS).This work aims to make a study on the above mentioned performance parameters of JL FinFET by tuning the work function of gate metal (gate electrode work function engineering)spacer engineering, and material(fin)engineering. This study is carried out with an objective of proposing different fin based architectures (trapezoidal and multifin) of P channel JL FinFET and to make a comparative study on these parameters. As trapezoidal fin is used, there is a significant variation occurs in the performance parameters of the device compared to the rectangular fin based structure. Multi fin structure provides better electrostatic control of gate over the channel and thus improves the operating parameters.

This paper is organized as follows. Section II demonstrates the device structures of different fin based architectures. In section III, device characteristics and performance parameters of device are analyzed. Section IV compares different fin based architectures. Section V concludes this paper.

II. DEVICE STRUCTURE

In P type rectangular junction less FinFET under study, the source, drain, and channel regions are uniformly doped with a concentration of 1019 cm-3.The simulated devices has SiO2 gate oxide with an equivalent oxide thickness (EOT) of 0.8 nm, box layer thickness (T_{BOX}) of 10 nm ,physical gate length (L_G)of 20 nm ,fin width(W_{FIN}) of 8 nm, and fin height(H_{FIN}) of 15 nm. TiN metal with a metal work function equals 4.33 eV is used as gate metal. The basic device specifications are given in Table I [2]. Silvaco TCAD simulator from SILVACO is used to perform all the simulations. General device models such as drift diffusion model with density-gradient quantum correction and mobility model is used. The mobility model incorporates the doping dependent and normal field dependent mobility degradation. Band gap narrowing model is also activated. Default values of some parameters of the simulator are modified.

The modified values of such parameters are mumin1 = 40 cm2/Vs, mumin2 = 22 cm2/Vs, mu1 = 18 cm2/Vs, Cr = 2.33 × 1020 cm−3, and α = 0.8 [2]. The physics section of DEVEDIT includes the appropriate models for quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. Newton and Gummel method is used in simulations to obtain accurate numerical results.

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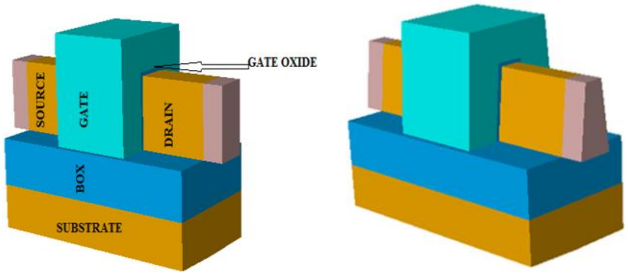
Table I. Device Specifications

Parameters	Typical Value
Gate Length(L_G)	20 nm
Fin Width(W_{FIN})	8 nm
Fin Height(H_{FIN})	15 nm
Equivalent Oxide Thickness(EOT)	0.8 nm
T_{BOX}	10 nm
Channel/Source/Drain Doping Concentration(P type)	$1*10^{19}$ cm^{-3}

Trapezoidal and Multi fin junctionless FinFET device structures has been proposed in this study. The device specifications of these structures are similar to the rectangular JL FinFET. The trapezoidal fin based approach is proposed in order to improve the operating parameters of JL FinFET. As trapezoidal fin is used, there is a significant variation occurs in the performance parameters of the device compared to the rectangular fin based structure. The schematic device structure of rectangular and trapezoidal JL FinFET is shown in Fig. 1(a) and (b) respectively.



(a) (b)

Fig. 1.(a) Rectangular JL FinFET (b) Trapezoidal JL FinFET

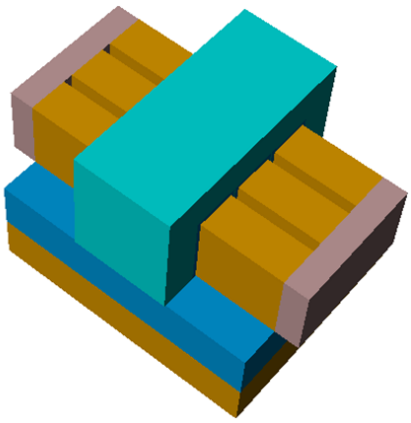


Fig. 2. Multifin JL FinFET

III. PERFOMANCE ANALYSIS

In each device the impact of work function engineering, spacer engineering, & material engineering is analyzed and a study on the performance parameter is carried out.

A. Work Function Engineering

Impact of work function engineering is studied by tuning the work function of gate electrode from 4.3 to 4.4 eV [3]. Fig. 3. and Fig. 4. shows the variation of I_{ON} and I_{OFF} as work function of gate electrode tuned from 4.3 to 4.4 eV. It can be observed that both I_{ON} and I_{OFF} increases as work function increases resulting in lower I_{ON}/I_{OFF} ratio.

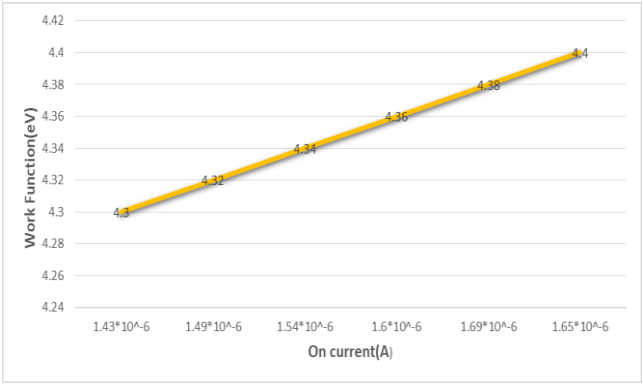


Fig. 3. Variation of I_{ON} with work function

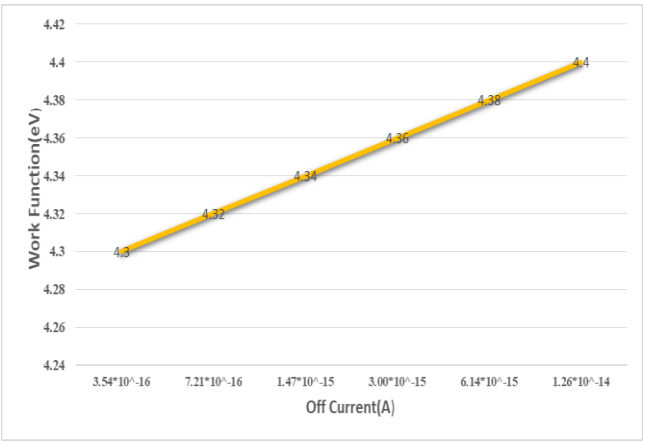


Fig. 4. Variation of IOFF with Work Function

Variation of threshold voltage and sub threshold swing of rectangular JL FinFET is shown in Fig. 5 and Fig. 6 .For P channel devices threshold voltage is found to be decreasing as work function increases. The subthreshold slope remains constant as work function changes.

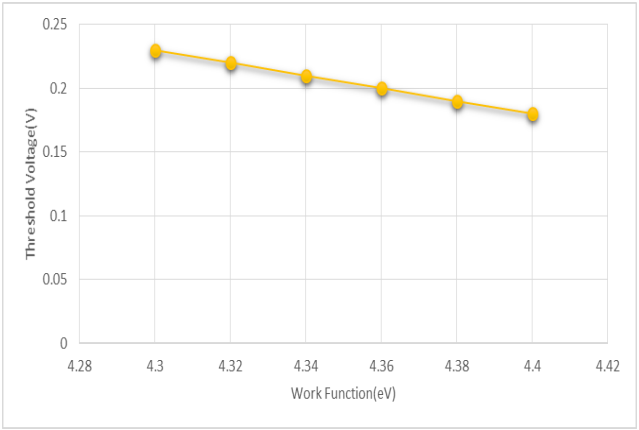


Fig. 5. Variation of V_{TH} with work function

It can be observed that the same impact as there in rectangular FinFET is obtained in trapezoidal and multifin JL FinFET.

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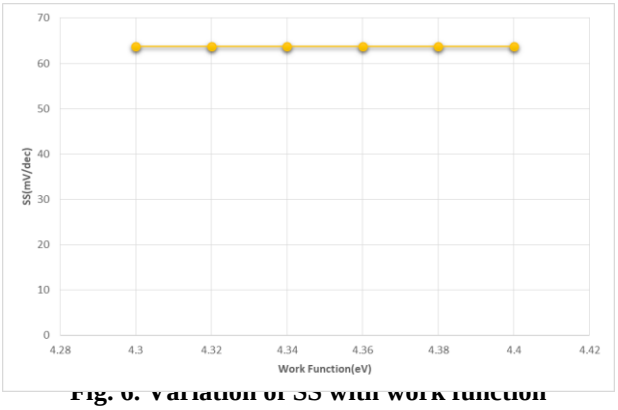

Fig. 6. Variation of SS with work function

B. Spacer Engineering

Devices with high–k spacers can be electrically induced which can minimize short channel effects [4].Use of high-k spacers can improve electrostatic integrity of the device ,that in turn decreases leakage current [5]. A single spacer material is used throughout the source /drain length(10 nm) on both sides of gate. Spacer materials such as SiO2 (k=3.9),Si_3N_4(k=7.5),HfO_2 (k=22) are considered in this study.In each device dielectric constant of spacer material is changed from 1 to 22 to investigate the fringing field effect with different spacers [6]. Fig. 7 and Fig. 8. shows I_D-V_{GS} characteristics of trapezoidal and multifin JL FinFET with high-k spacers respectively.

Leakage current is reduced with increase in dielectric constant of spacer due to the high vertical electric field in the OFF state. In the ON state flat band condition arises zero electric field and ON current is almost constant. Also multifin JL FinFET with HfO_2 spacer provides I_{ON}/I_{OFF} ratio of the order of 10^{20} and thus showing better performance.

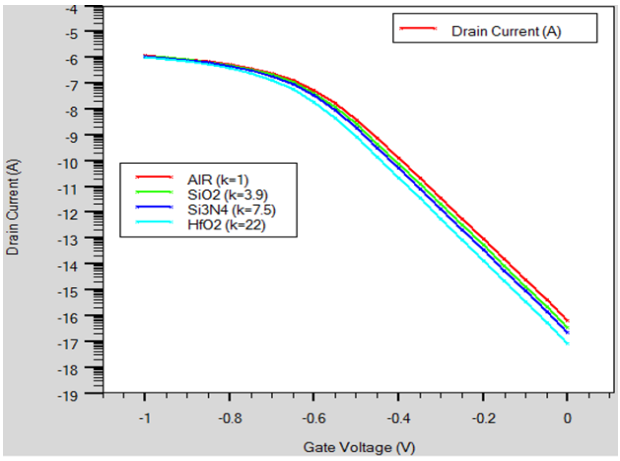

Fig. 7. I_D-V_{GS} characteristics of trapezoidal JL FinFET with high-k spacers.

C. Material Engineering

Performance of each device is analyzed with varying fin material. Material engineering is carried out by replacing the Si fin by InAs,InGaAs,SiGe material. For rectangular JL FinFET the performance parameters are improved significantly with the use of InAs and SiGe as the fin material.

Fig. 9. and Fig. 10. shows I_D-V_{GS} characteristics of trapezoidal and multifin JL FinFET with varying fin material respectively. Multifin JL FinFET with SiGe and InAs fin offers leakage current in the order of 10-18 with I_{ON}/I_{OFF} ratio in the order of 10^{11}.

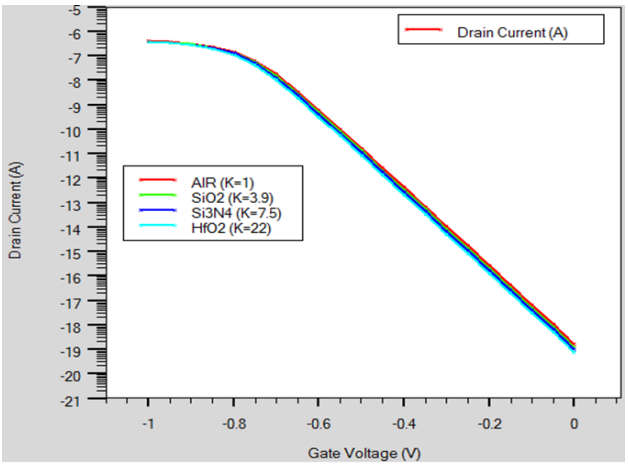

Fig. 8. I_D-V_{GS} characteristics of multifin JL FinFET with high-k spacers

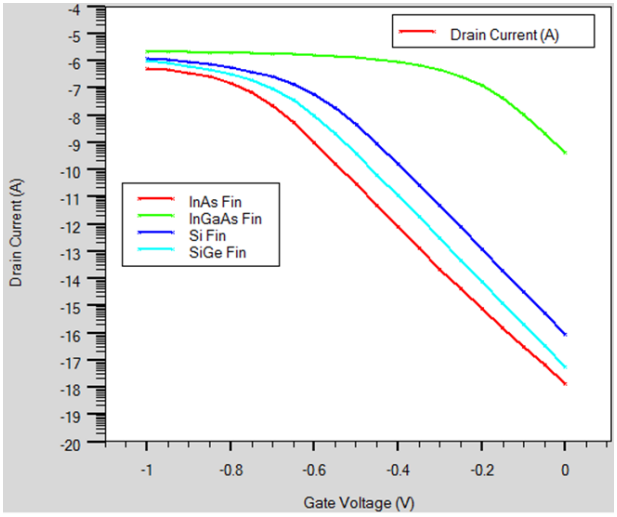

Fig. 9. I_D –V_{GS} characteristics of Trapezoidal JL FinFET with varying fin material

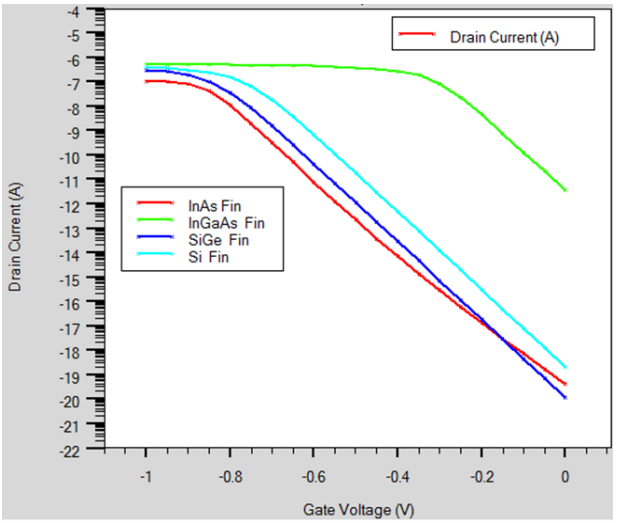

Fig. 10. I_D –V_{GS} characteristics of Multifin JL FinFET with Varying Fin Material

IV. COMPARISON

This section compares three fin based structures of JL FinFETs in terms of leakage current, I_{ON}/I_{OFF} ratio, threshold voltage and sub threshold swing. Fig .11- 13 shows the comparison of different shaped fin structures on I_{ON}/I_{OFF} ratio, V_{TH} and SS respectively.

The proposed structures of JL FinFET have a higher I_{ON}/I_{OFF} ratio and better short channel characteristics compared to the existing JL FinFET structure. Multifin structure has an I_{ON}/I_{OFF} ratio of the order 10^{12} and sub threshold swing 62.5mV/dec along with lower leakage current.

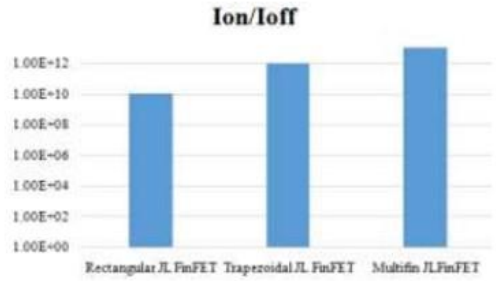

Fig. 11. Comparison on I_{ON}/I_{OFF} ratio

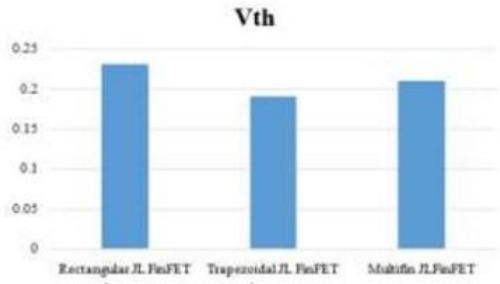

Fig. 12. Comparison on VTH

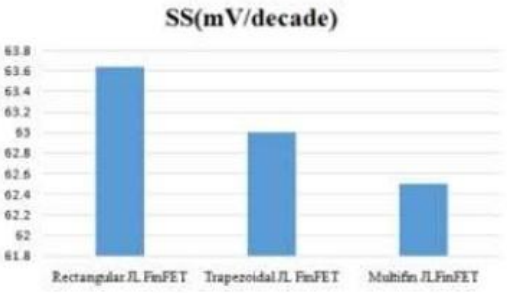

Fig. 13. Comparison on Subthreshold Slope

V. CONCLUSION

Trapezoidal and Multifin structure of JL FinFETs are proposed and the impact of WFV, spacer dielectric, &material engineering are studied. Same effects are analyzed on the performance of conventional P channel JL FinFET . A comparative study is done on different fin based structures and it is observed that Multifin JLFinFET shows better short channel characteristics with I_{ON}/I_{OFF} ratio in the order of $10^{12}$and SS value as 62.5mV/dec. High k spacers improve the electrostatic integrity of the device results in reduction of leakage current and WFV affects the performance of JL devices.

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