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A Cascaded H-Bridge Multilevel Inverter based on Switched-Capacitor for High Frequency Ac Applications

M. S. S. Bhadri Nadh, R. V. D. Rama Rao

Abstract: ***High frequency ac applications with a reduced component of a cascaded multilevel inverter using switched capacitor are proposed in this project. Here switched capacitor and H-Bridges are constructed in front end and back end through the connections of series and parallel conversions. An increasing the voltage level by switched capacitor, output harmonics can be reduced. High Frequency AC Applications (HFAC) is alternative to DC distribution due to lower cost. These are most commonly used to apply for small scale and closed electrical network in electric vehicles due to moderate size and reduction of weight for distribution network. The type of multilevel inverter used in this project is cascaded H-Bridge and they built by the series connection of H-Bridges. It is similar to dc-dc converters. The cascaded H-Bridges needs individual input and four power switches for construction in order to increase number of voltage levels with their staircase output. However control strategy is difficult because of input current will be in discontinuous; therefore Electromagnetic Interference (EMI) becomes worst. The advantages for this topology at rated output frequency of about 20 kHz are feasible to operate, increasing reliability and high efficiency. By increasing number of voltage levels, the total harmonic distortion (THD) content of staircase output can be decreased and further in such a way that, has a particular meaning to simplifying the filter design. This topology will be analyzed by symmetrical modulation for 13–level inverter, which is based on switched capacitor of a cascaded multilevel inverter for HFAC PDS. The entire system is simulated in MATLAB/SIMULINK TOOL.***

Keywords: Cascaded H-Bridge, High–Frequency Ac (HFAC), Multilevel inverter, Switched Capacitor (SC), Symmetrical Phase-Shift Modulation (PSM).

I. INTRODUCTION

HIGH-FREQUENCY ac (HFAC) power distribution system (PDS) potentially becomes an alternative to traditional dc distribution due to the fewer components and lower cost. The existing applications can be found in computer [1], telecom [2], electric vehicle [3], and renewable energy micro grid [4], [5].However; HFACPDS has to confront the challenges from large power capacity, high electromagnetic interference (EMI), and severe power losses [6].A traditional HFAC PDS is made up of a high-frequency (HF) inverter, an HF transmission track, and numerous voltage-regulation modules (VRM). HF inverter accomplishes the power conversion to accommodate the requirement of point of load (POL).In order to increase the power capacity; The most popular method is to connect the inverter output in series or in parallel. However, it is impractical for HF inverter, because it is complicated to simultaneously synchronize both amplitude and phase with HF dynamics. Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity is easy to be achieved by multilevel inverter with lower switch stress. Non polluted sinusoidal waveform with the lower total harmonic distortion (THD) is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of staircase output, thus significantly simplifying the filter design [7]. HF power distribution is applicable for small-scale and internal closed electrical network in electric vehicle (EV) due to moderate size of distribution network and effective weight reduction [8]. The consideration of operation frequency has to make compromise between the ac inductance and resistance [9], so multilevel inverter with the output frequency of about 20 kHz is a feasible trial to serve as power source for HF EV application.

The traditional topologies of multilevel inverter mainly are diode-clamped and capacitor clamped type [10], [11]. The former uses diodes to clamp the voltage level, and the latter uses additional capacitors to clamp the voltage. The higher number of voltage levels can then be obtained; however, the circuit becomes extremely complex in these two topologies. Another kind of multilevel inverter is cascaded H-Bridge constructed by the series connection of H-Bridges [12], [13]. The basic circuit is similar to the classical H-bridge DC–DC converter [14]. The cascaded structure increases the system reliability because of the same circuit cell, control structure and modulation. However, the disadvantages confronted by cascaded structure are more switches and a number of inputs. In order to increase two voltage levels in staircase output, an H-Bridge constructed by four power switches and an individual input are needed. Theoretically, cascaded H-Bridge can obtain staircase output with any number of voltage levels, but it is inappropriate to the applications of cost saving and input limitation. A number of studies have been performed to increase the number of voltage levels. A switched-capacitor (SC) based multilevel circuit can effectively increase the number of voltage levels. However, the control strategy is complex, and EMI issue becomes worse due to the discontinuous input current [15].

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A single-phase five-level pulse width modulated (PWM) inverter is constituted by a full bridge of diodes, two capacitors and a switch. However, it only provides output with five voltage levels, and higher number of voltage levels is limited by circuit structure[16].An SC-based cascaded inverter was presented with SC frontend and full bridge backend. However, both complicated control and increased components limit its application [17].The further study was presented using series/parallel conversion of SC. However, it is in appropriate to the applications with HF output because of multicarrier PWM (MPWM)[18],[19].If output frequency is around 20 kHz, the carrier frequency reaches a couple of megahertz. Namely, the carrier frequency in MPWM is dozens times of the output frequency. Since the carrier frequency determines the switching frequency, a high switching loss is inevitable for the sake of high-frequency output. A boost multilevel inverter based in partial charging of SC can increase the number of voltage levels theoretically. However, the control strategy is complicated to implement partial charging [20]. Therefore, it is a challenging task to present an SC-based multilevel inverter with high-frequency output, low-output harmonics, and high conversion efficiency [21]. Based on the study situation aforementioned, a novel multilevel inverter and simple modulation strategy are presented to serve as HF power source. The rest of this paper is organized as follows. The discussions of nine-level inverter are presented in Section II, including circuit topology, modulation strategy, operation cycle, and Fourier analysis. The parameter determination and loss analysis are discussed in chapter III. The further enhancement of 13-level inverter is studied in chapter IV. The performance evaluation accomplished by simulation is described in chapter VI followed by concluding remarks.

II. SC BASED CASCADED H-BRIDGE MULTI LEVEL INVERTER WITH 13-LEVEL OUTPUT

The proposed circuit is made up of the SC frontend and cascaded H-Bridge backend.

A. Circuit Topology.

Fig. 1 shows the circuit topology of nine-level inverter ($N_1 = 2$, $N_2 = 2$), where S_1, S_2, $S_1^{'}$, $S_2^{'}$ as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of C_1 and C_2 . S_{1a}, S_{1b} , S_{1c} , S_{1d} , S_{2a} , S_{2b} , S_{2c} , S_{2d} are the switching devices of cascaded H-Bridge. V_{dc1} and V_{dc2} are input voltage. D_1 and D_2 are diodes to restrict the current direction. i_{out} and v_o are the output current and the output voltage, respectively.

The number of voltage levels can be further increased via two approaches. One is to increase the level number generated by SC circuit. The other one is to increase level number generated by cascaded H-Bridge. Thirteen-level inverter, 2×3 structure as shown in Fig.1 is derived by the enhancement of H-Bridge circuit, which needs 3 diodes, 3 capacitors, 18 switches, and 3 dc inputs.

It can be found that 3×2 structure requires more diodes and capacitors than 2×3 structure. However, the number of power switches in 3×2 structure is less than that in 2×3 structure. Because the traditional cascaded H-bridge needs 24 switches and 6 inputs to produce 13 voltage levels, the numbers of power switches and inputs are greatly decreased by proposed inverter.

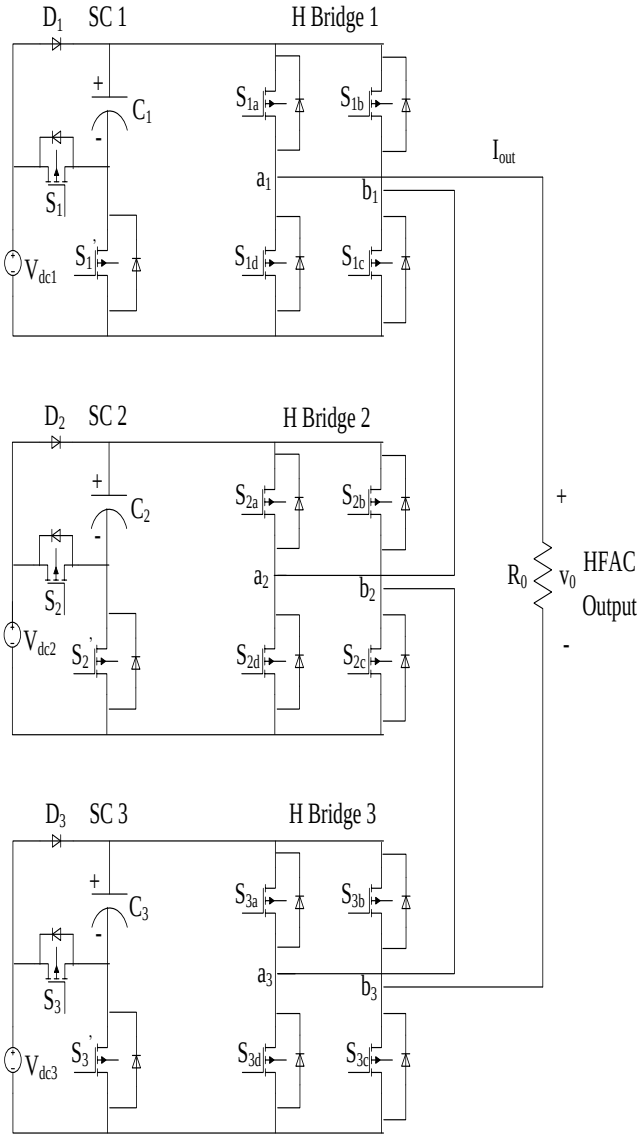

Fig.1 Circuit Topology of 13-Level Inverter 2×3 with Three Dc Inputs

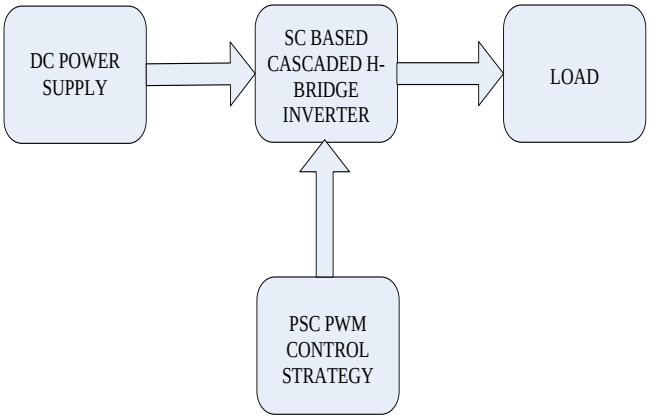

Fig. 2. Block Diagram for SC based Cascaded H-Bridge Inverter

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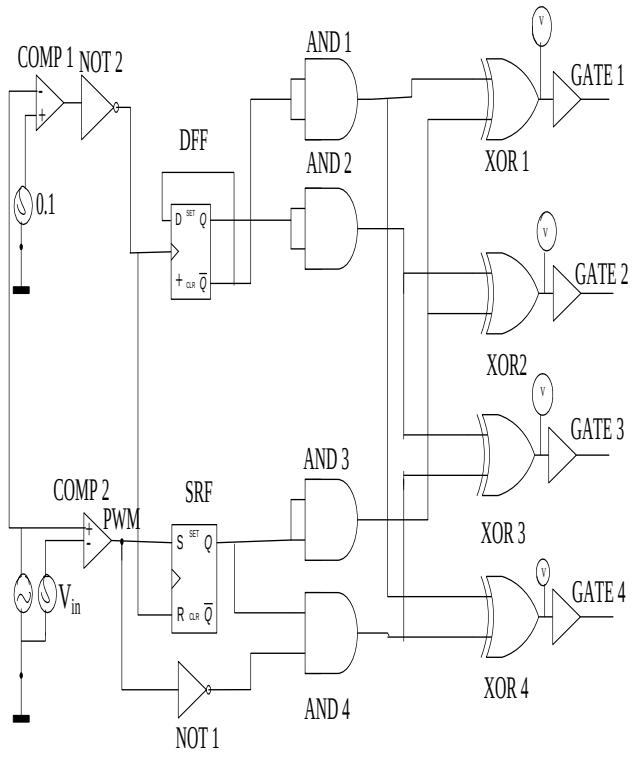

Fig.3. (a) Circuit of Symmetrical PSM

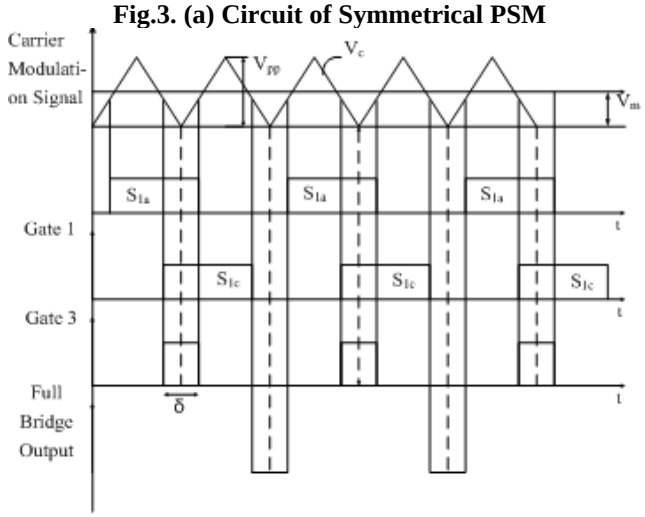

Fig.3.(b) circuit and operational waveform of symmetrical PSM (a)circuit of symmetrical PSM (b) Operational waveforms of symmetrical PSM.

III. SYMMETRICAL MODULATION

There are many modulation methods to regulate the multilevel inverter, the popular modulations are the space vector modulation [22], the multicarrier PWM [23], and the selective harmonic elimination [24], [25], sub harmonic pulse width modulation [26], etc. However, most of them greatly increase the carrier frequency that is dozens times the frequency of reference or output. A symmetrical phase-shift modulation (PSM) is introduced into the proposed multilevel inverter. The symmetrical PSM ensures the output voltage of full bridge is symmetrical to the carrier, so voltage levels can be superimposed symmetrically and carrier frequency is twice as that of the output frequency [27]. The structure of symmetrical PSM is shown in Fig. 2(a), and the operational waveform of symmetrical PSM is shown in Fig. 2(b).

The logic operations of gate signals are

$$\text{gate1} = XOR\{Q(RS), \bar{Q}(D)\}$$
$$\text{gate2} = XOR\{Q(RS), Q(D)\} \quad (1)$$
$$\text{gate3} = XOR\{AND\{Q(RS), NOT\,(PWM)\}, Q(D)\}$$
$$\text{gate4} = XOR\{AND\{Q(RS), NOT(PWM)\}, \bar{Q}(D)\}. \quad (2)$$

A controlled PWM with pulse width δ is symmetrically generated by the comparisons of the triangle carrier V_c and modulation signal V_m. The rising edge matching of V_c and V_m triggers the polarity inversion of the leading bridge, while the falling edge matching of V_c and V_m triggers the polarity inversion of the lagging bridge. When V_m has a change ΔV_m, this modulation simultaneously moves gate 1 and gate 3 in the opposite direction. Thus, the derived Vab is symmetrical with respect to Vc.

Table-1. In Order to Accomplish the Staircase Output with 4n + 1 Voltage Levels, the Component Counts are Compared in Table-1.

Table-1 Components Comparison of Proposed Inverter and Cascaded h-Bridge.

Inverter type	Proposed inverter enhanced by SC n*2 topology	Proposed inverter enhanced by H-Bridge 2*n topology	Cascaded H-Bridge
Switching device	2n+8	6n	8n
Capacitor	2n-2	n	0
Diode	4n-6	n	0
DC bus	2	n	2n
Power Losses	$(2n2)loss_{cap}+$ $(4n6)loss_{diode}+$ $(2n+8)loss_{switch}$	$nloss_{cap}+$ $nloss_{diode}+$ $6nloss_{switch}$	$8nloss_{switch}$

A 2*n topology needs n capacitors, 6n switches, and n dc inputs; n*2 topology needs 2n –2 capacitors, 2n+8 switches, and 2 dc inputs. The traditional cascaded H-Bridge needs 8n switches and 2n dc inputs. With the same number of voltage levels, the proposed inverter needs less switching devices and inputs than the traditional cascaded H-Bridge. Considering the power losses, the traditional cascaded H-bridge has the higher switching losses caused by more switch devices. However, the proposed inverter newly introduces the capacitor loss that has already been examined in last section. Moreover, a flexible circuit structure becomes possible. It is feasible for the proposed multilevel inverter to select suitable enhancement that can ac-commodate the requirements from different applications.

For example, 2×n topology can be used for the power application sourced by multiple solar panels or batteries, and n×2topology can be used for the power application sourced by dual power sources.

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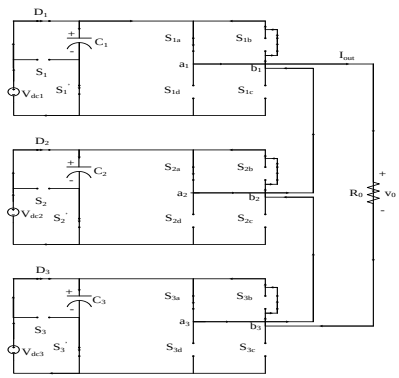
A. Modes of Operation

The mode of operation with reference to the switching pattern given to the circuit as shown in figure.1 is tabulated in table-II.

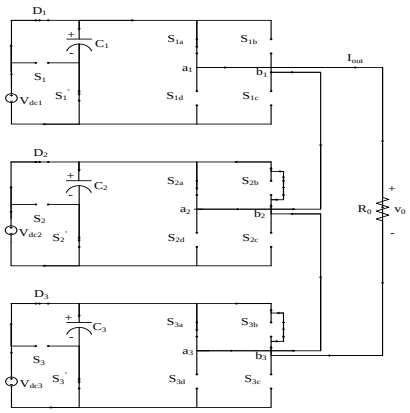
Mode of Operation		
On-State Switches	**Output Voltage**	**Capacitor State**
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1, S_2, S_3	$6V_{in}$	C_1, C_2, C_3 Discharging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1', S_2, S_3	$5V_{in}$	C_2, C_3 Discharging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1', S_2', S_3	$4V_{in}$	C_3 Discharging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1', S_2', S_3'	$3V_{in}$	C_1, C_2, C_3 charging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3b}, S_1', S_2', S_3'	$2V_{in}$	C_1, C_2, C_3 charging
S_{1a}, S_{1c}, S_{2a}, S_{2b}, S_{3a}, S_{3b}, S_1', S_2', S_3'	V_{in}	C_1, C_2, C_3 charging
S_{1a} (or) S_{1c}, S_{2a}(or)S_{2c}, S_{3a}(or)S_{3c}, S_1', S_2', S_3' S_{1b} (or) S_{1d}, S_{2b}(or)S_{2d}, S_{3b}(or)S_{3d}, S_1', S_2', S_3'	0V	C_1, C_2, C_3 charging
S_{1b}, S_{1d}, S_{2b}, S_{2a}, S_{3b}, S_{3a}, S_1', S_2', S_3'	$-V_{in}$	C_1, C_2, C_3 charging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3a}, S_1', S_2', S_3'	$-2V_{in}$	C_1, C_2, C_3 charging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1', S_2', S_3'	$-3V_{in}$	C_1, C_2, C_3 charging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1', S_2', S_3	$-4V_{in}$	C_3 Discharging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1', S_2, S_3	$-5V_{in}$	C_2, C_3 Discharging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1, S_2, S_3	$-6V_{in}$	C_1, C_2, C_3 Discharging

For Positive Half Cycle

For 0V:



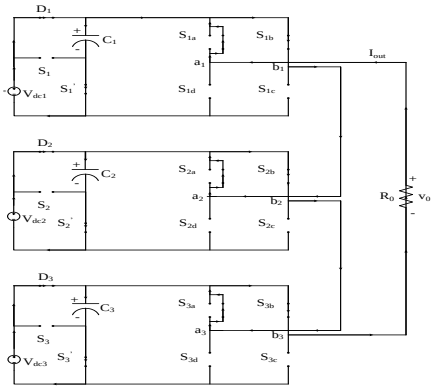
For V_{in}:



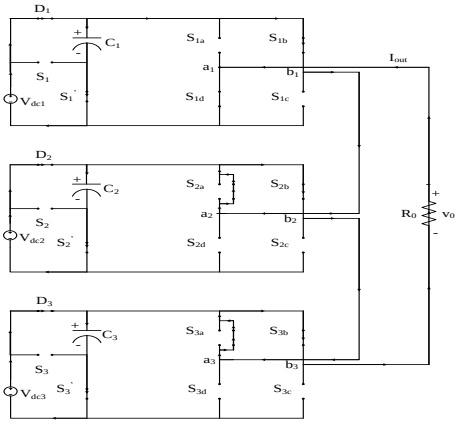
For $2V_{in}$:

For Negative Half Cycle

For 0V:



For $-V_{in}$:



For $-2V_{in}$:

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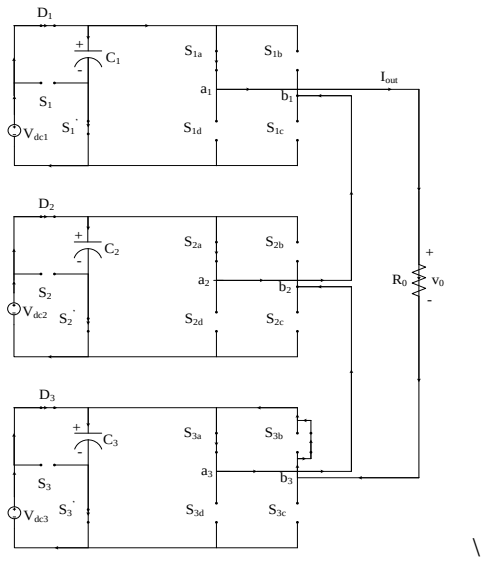
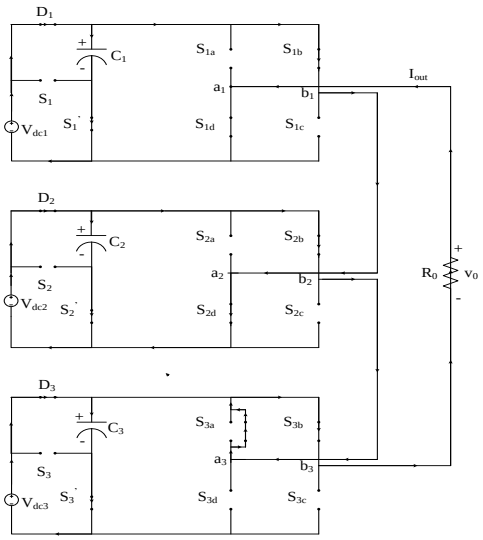
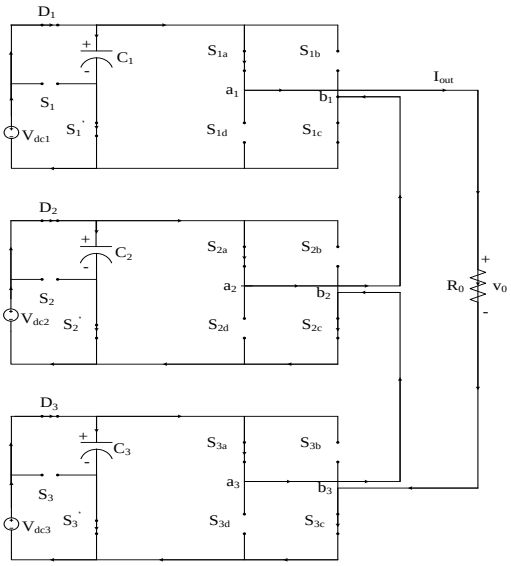


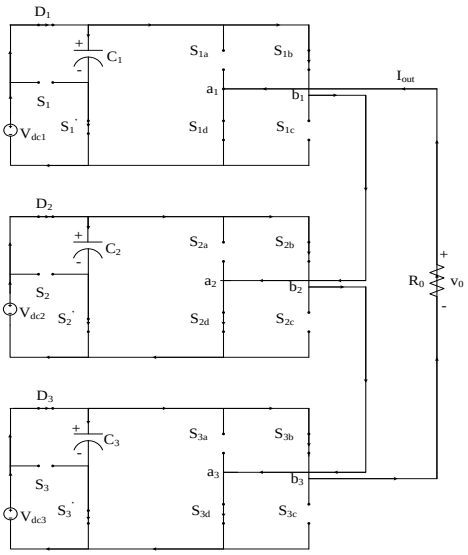
For $3V_{in}$:



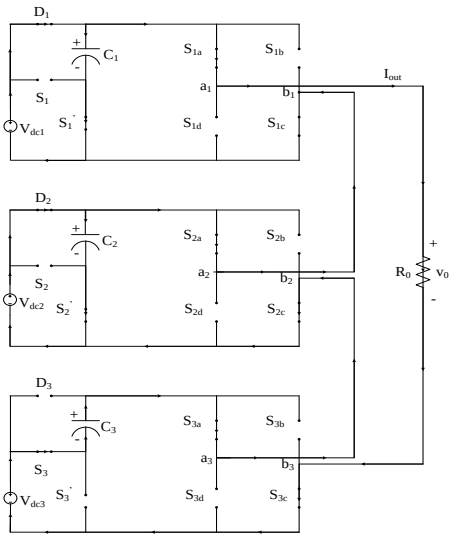
For $-3V_{in}$:



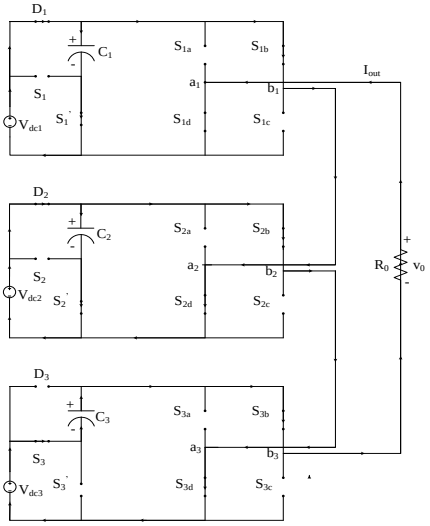
For $4V_{in}$:



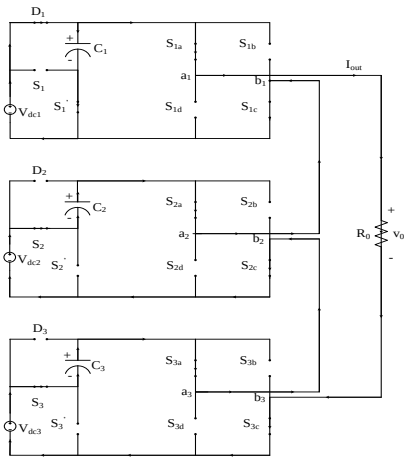
For $-4V_{in}$:



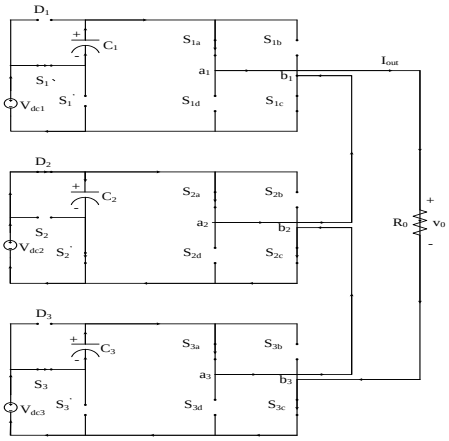
For $5V_{in}$:



For $-5V_{in}$:



For $6V_{in}$:



The above figureS shows the Positive half cycle's and Negative Half Cycle's.

For Positive Half Cycle

For 0V:

At the instant when t satisfies $t_0<t<t_1$ the switches

S_{1a} (or)S_{1c}, S_{2a}(or)S_{2c}, S_{3a}(or)S_{3c}, S_1', S_2', S_3'

S_{1b} (or)S_{1d}, S_{2b}(or)S_{2d}, S_{3b}(or)S_{3d}, S_1', S_2', S_3'

& C_1, C_2, C_3 charging.

The operational mode 1: t_0–t_1

Applying KVL equation, we get,

$V_0=0$

$V_0 = 0V$

For V_{in}:

At the instant when t satisfies $t_1\leq t<t_2$ the switches

S_{1a} , S_{1c}, S_{2a}, S_{2b}, S_{3a}, S_{3b}, S_1', S_2', S_3'

& C_1, C_2, C_3 charging.

The operational mode 1: t_1–t_2

Applying KVL equation, we get,

$-V_{dc1}+V_0=0$

$V_0=V_{dc1}$ $[V_{dc1}=V_{dc2}=V_{in}]$

$V_0 = V_{in}$

For $2V_{in}$:

At the instant when t satisfies $t_2\leq t<t_3$ the switches

S_{1a} , S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3b}, S_1', S_2', S_3'

& C_1, C_2, C_3 charging.

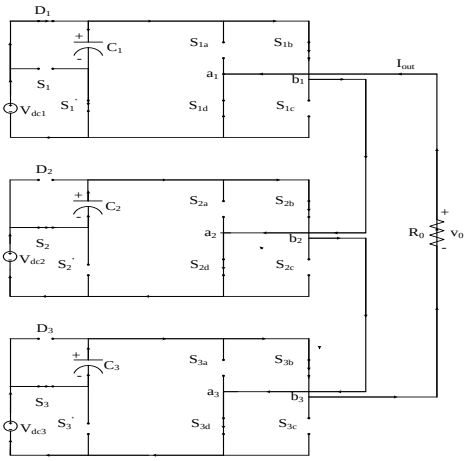
The operational mode 1: t_2–t_3

Applying KVL equation, we get,

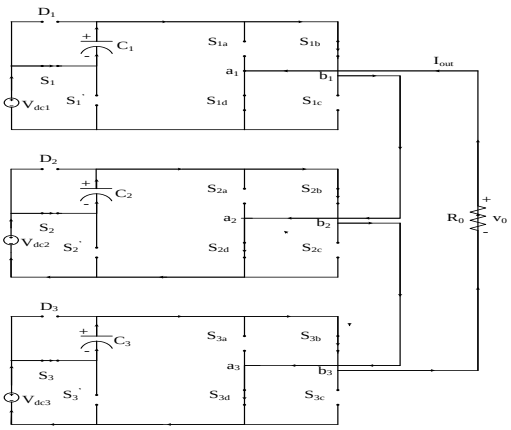
$-V_{dc1}+V_0-V_{dc2}=0$

$V_0= V_{dc1}+ V_{dc2}$

$V_0 = 2V_{in}$



For $-6V_{in}$:



For $3V_{in}$:

At the instant when t satisfies $t_3\leq t<t_4$ the switches

S_{1a} , S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1', S_2', S_3' & C_1, C_2, C_3 charging.

The operational mode 1: t_3–t_4

Applying KVL equation, we get,

$-V_{dc1}+V_0-V_{dc2}-V_{dc3}=0$

$V_0= V_{dc1}+ V_{dc2}+ V_{dc3}$

$V_0 = 3V_{in}$

For $4V_{in}$:

At the instant when t satisfies $t_4\leq t<t_5$ the switches

S_{1a} , S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1', S_2', S_3 & C_3 Discharging.

The operational mode 1: t_4–t_5

Applying KVL equation, we get,

$-V_{dc1}+V_0-V_{dc2}-V_{dc3}-V_{c3} = 0$

$V_0= V_{dc1}+V_{dc2}+ V_{dc3}+ V_{c3}$

$V_0 = 4V_{in}$

For $5V_{in}$:

At the instant when t satisfies $t_5\leq t<t_6$ the switches

S_{1a} , S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1', S_2, S_3& C_2, C_3 Discharging.

The operational mode 1: t_5–t_6

Applying KVL equation, we get,

$-V_{dc1}+V_0-V_{dc2}-V_{c2}-V_{dc3}-V_{c3} = 0$

$V_0= V_{dc1}+V_{dc2}+ V_{c2}+ V_{dc3}+ V_{c3}$

$V_0 = 5V_{in}$

For $6V_{in}$:

At the instant when t satisfies $t_6 \le t < t_7$ the switches
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_{3a}, S_{3c}, S_1, S_2, S_3 & C_1, C_2, C_3 Discharging.
The operational mode 1: t_6–t_7
Applying KVL equation, we get,
$-V_{dc1}-V_{c1}+V_0-V_{dc2}-V_{c2}-V_{dc3}-V_{c3} = 0$
$V_0 = V_{dc1}+V_{c1}+V_{dc2}+V_{c2}+V_{dc3}+V_{c3}$
$V_0 = 6V_{in}$
At the instants active circuits for $t_7 \le t < t_8$, $t_8 \le t < t_9$, and $t_9 \le t < t_{10}$, $t_{10} \le t < t_{11}$, $t_{11} \le t < t_{12}$ are same as the operations in $t_6 \le t < t_7$, $t_5 \le t < t_6$, $t_4 \le t < t_5$ $t_3 \le t < t_4$, $t_2 \le t < t_3$, $t_1 \le t < t_2$ respectively.
For Negative Half Cycle
For 0V:
At the instant when t satisfies $-t_0 < t < -t_1$ the switches
S_{1a} (or)S_{1c}, S_{2a}(or)S_{2c}, S_{3a}(or)S_{3c}, S_1', S_2', S_3'
S_{1b} (or)S_{1d}, S_{2b}(or)S_{2d}, S_{3b}(or)S_{3d}, S_1', S_2', S_3'
& C_1, C_2, C_3 charging.
The operational mode 1: $-t_0$–$(-t_1)$
Applying KVL equation, we get,
$-V_0 = 0$
$-V_0 = 0V$
For $-V_{in}$:
At the instant when t satisfies $-t_1 \le t < -t_2$ the switches
S_{1b}, S_{1d}, S_{2b}, S_{2a}, S_{3b}, S_{3a}, S_1', S_2', S_3' & C_1, C_2, C_3 charging.
The operational mode 1: $-t_1$–$(-t_2)$
Applying KVL equation, we get,
$-V_{dc1}-V_0=0$
$-V_0=V_{dc1}$ $[V_{dc1}=V_{dc2}=V_{in}]$
$V_0 = -V_{in}$

For $-2V_{in}$:
At the instant when t satisfies $-t_2 \le t < -t_3$ the switches
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3a}, S_1', S_2', S_3'
& C_1, C_2, C_3 charging.
The operational mode 1: $-t_2$–$(-t_3)$
Applying KVL equation, we get,
$-V_{dc1}-V_0-V_{dc2}=0$
$-V_0 = V_{dc1}+V_{dc2}$
$V_0 = -2V_{in}$

For $-3V_{in}$:
At the instant when t satisfies $-t_3 \le t < -t_4$ the switches
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1', S_2', S_3'
& C_1, C_2, C_3 charging.
The operational mode 1: $-t_3$–$(-t_4)$
Applying KVL equation, we get,
$-V_{dc1}-V_0-V_{dc2}-V_{dc3}=0$
$-V_0 = V_{dc1}+V_{dc2}+V_{dc3}$
$V_0 = -3V_{in}$

For $-4V_{in}$:
At the instant when t satisfies $-t_4 \le t < -t_5$ the switches
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1', S_2', S_3
& C_3 Discharging.
The operational mode 1: $-t_4$–$(-t_5)$
Applying KVL equation, we get,
$-V_{dc1}-V_0-V_{dc2}-V_{dc3}-V_{c3} = 0$
$-V_0 = V_{dc1}+V_{dc2}+V_{dc3}+V_{c3}$
$V_0 = -4V_{in}$

For $-5V_{in}$:
At the instant when t satisfies $-t_5 \le t < -t_6$ the switches
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1', S_2, S_3
& C_2, C_3 Discharging.
The operational mode 1: $-t_5$–$(-t_6)$
Applying KVL equation, we get,
$-V_{dc1}-V_0-V_{dc2}-V_{c2}-V_{dc3}-V_{c3} = 0$
$-V_0 = V_{dc1}+V_{dc2}+V_{c2}+V_{dc3}+V_{c3}$
$V_0 = -5V_{in}$

For $-6V_{in}$:
At the instant when t satisfies $-t_6 \le t < -t_7$ the switches
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_{3b}, S_{3d}, S_1, S_2, S_3
& C_1, C_2, C_3 Discharging.
The operational mode 1: $-t_6$–$(-t_7)$
Applying KVL equation, we get,
$-V_{dc1}-V_{c1}-V_0-V_{dc2}-V_{c2}-V_{dc3}-V_{c3} = 0$
$-V_0 = V_{dc1}+V_{c1}+V_{dc2}+V_{c2}+V_{dc3}+V_{c3}$
$V_0 = -6V_{in}$
At the instants active circuits for
$-t_7 \le t < -t_8$, $-t_8 \le t < -t_9$, and $-t_9 \le t < -t_{10}$, $-t_{10} \le t < -t_{11}$, $-t_{11} \le t < -t_{12}$ are same as the operations in $-t_6 \le t < -t_7$, $-t_5 \le t < -t_6$, $-t_4 \le t < -t_5$ $-t_3 \le t < -t_4$, $-t_2 \le t < -t_3$, $-t_1 \le t < -t_2$ respectively.

OPERATION CYCLES

Derivation of Harmonics & Fourier Analysis for Operation Cycles

In aforementioned nine-level inverter, the staircase output v_o can be divided into four components v_{01},v_{02},v_{03}, and v_{04} as shown in Fig.4. The durations of each component are decided by the comparisons of reference signal (V_{m_1c},V_{m_1b}, V_{m_1d},V_{m_2c},V_{m_2b}, V_{m_2d}) and triangular carrier (V_c). If pulse widths of the constituted component are defined as δ_1, δ_2, α_1, and α_2, Fourier analysis is accomplished for this nine-level staircase.

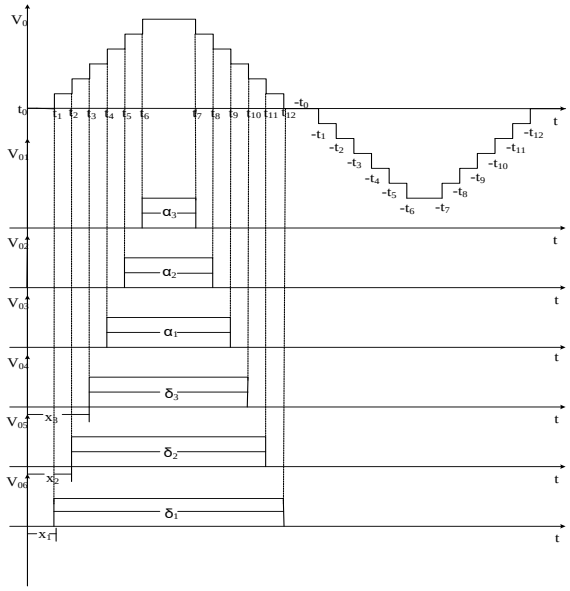


Fig.3 Output Voltage Decomposition for Fourier Analysis in the Operational Mode

The magnitude of the harmonics is derived by

$$Vn = \frac{6V_{in}}{n\pi}\left(\cos\left(n\left(\frac{\pi-\alpha_1}{2}\right)\right) + \cos\left(n\left(\frac{\pi-\delta_1}{2}\right)\right) +\right.$$

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$$\cos(n(\tfrac{\pi-\alpha_2}{2})) + \cos(n(\tfrac{\pi-\delta_2}{2})) + \cos(n(\tfrac{\pi-\alpha_3}{2}))\cos(n(\tfrac{\pi-\delta_3}{2}))) \quad (1)$$

Where,

n= 1, 3, 5...

In operational mode 1

$$\delta_1 = \frac{Vm\_2b}{Vpp}\pi, \qquad \alpha_1 = \frac{Vm\_1b}{Vpp}\pi$$

$$\delta_2 = \frac{Vm\_2c}{Vpp}\pi, \qquad \alpha_2 = \frac{Vm\_1c}{Vpp}\pi$$

$$\delta_3 = \frac{Vm\_2d}{Vpp}\pi, \qquad \alpha_3 = \frac{Vm\_1d}{Vpp}\pi \quad (2)$$

To further describe the relations of output THD and pulse widths α_1, α_2, α_3, δ_1, δ_2, δ_3 six parameters are pre-defined

$$k_1 = \frac{\alpha_1}{\delta_1}, \quad k_2 = \frac{\alpha_2}{\delta_2}, \quad k_3 = \frac{\alpha_3}{\delta_3},$$

$$x = \frac{\pi-\delta_1}{2}, \quad x_2 = \frac{\pi-\delta_2}{2}, \quad x_3 = \frac{\pi-\delta_3}{2}, \quad (3)$$

The output waveforms can be characterized by these four constants. According to the definitions as (THD = $(\sqrt{\sum_{n=2.....}^{\infty} V_n^2}/V_1) \times 100\%$), THD of output voltage can be calculated by the harmonic magnitudes. The relations of output THD to x_1, x_2, x_3 are given with the fixed k_1, k_2 and k_3.

IV. DETERMINATION OF CAPACITANCE

As shown in Fig.3.2, the capacitors are charged when they are in parallel with power source, and the capacitors are discharged when they are in series with power source. The switch S_1 and S_1' are driven alternatively during the half of output cycle. Therefore, the driven frequency of S_1 and S_1' is twice the frequency of output voltage, as well as the driven frequency of S_{1a}–S_{1d} is the same as the frequency of output voltage.

The capacitance of C_i is determined by the voltage ripple of C_i that denotes the voltage fluctuation of multilevel output. The larger capacitance has the fewer ripple voltage. The voltage fluctuation over a narrow scope has a smaller power losses and higher capacitor efficiency. The appropriated method of capacitance calculation is that the maximum voltage ripple is 10% of the maximum capacitor voltage [28]. Before obtaining the capacitance of C_i, two assumptions are given to simplify the derivations:

1) The output load is pure resistive load, and

2) The same duration is given in each level of staircase output. Therefore, the time points in Fig. 3.2 are

$t_0 = 0$, $t_1 = \frac{1}{20}t_s$, $t_2 = \frac{1}{10}t_s$, $t_3 = \frac{3}{20}t_s$, $t_4 = \frac{1}{5}t_s$, $t_5 = \frac{3}{10}t_s$, $t_6 = \frac{7}{20}t_s$, $t_7 = \frac{2}{5}t_s$, $t_8 = \frac{9}{20}t_s$ (1)

where t_s is the period of the output voltage derived by

$$t_s = \frac{1}{f_s} \quad (2)$$

Where f_s is the frequency of the output voltage. In the operational mode 1, as shown in Fig.3.2 (a), the longest discharging cycle of C_1 is between t_4 and t_5, and the longest discharging cycle of C_2 is between t_3 and t_6. In the operational mode 2, as shown in Fig.3.2 (b), the longest discharging cycle of C_1 is the same as the operational mode 1, while the longest discharging cycle of C_2 is between t_2 and t_7. Therefore, the maximum discharging amount of C_1 is Q_{c1} and is defined as

$$Q_{c1} = \int_{t_4}^{t_5} I_{out}\sin(2\pi f_s t - \Phi)dt \quad (3)$$

Where,

I_{out} is the amplitude of the output current i_{out} and Φ is the phase difference between the output voltage v_o and current i_{out}.If 10% ripple voltage is considered, Qc1 should be less than 10% of the maximum charge of C_1, i.e.

$$C_1 \geq \frac{Q_{c1}}{0.1V_{in}}. \quad (4)$$

Furthermore, the maximum discharging amount of C_2 is Q_{c2} and is defined as

$$Q_{c2} = \int_{t_3}^{t_6} I_{out}\sin(2\pi f_s t - \Phi)dt, \text{ mode 1} \quad (5)$$

$$Q_{c2} = \int_{t_2}^{7} I_{out}\sin(2\pi f_s t - \Phi)dt, \text{mode 2} \quad (6)$$

Then

$$C_2 \geq \frac{Q_{c1}}{0.1V_{in}} \quad (7)$$

It can be seen from the equations that the operational mode 2 needs larger C_2 than that in operational mode 1. When the load is resistive, the phase of load current is agreed with the load voltage. The maximum discharging amount of capacitor is obtained in resistive load, because the peak load current is the midpoint of integration period. In other words, if the capacitance of C_i is derived in pure resistive load, it also maintains the less voltage ripples in inductive load.

The peak current of the capacitor C_i is derived by

$$I_{ci} = \frac{V_{in} - V_{C_i} - V_{dF}}{r_c + r_{on} + r_d} \quad (8)$$

Where,

V_{Ci} is the voltage on the capacitors C_i, V_{dF} is the forward voltage drop of diode, r_c is the equivalent series resistance (ESR) of the capacitors, r_{on} is the internal on-state resistance of the switching device and r_d is the internal on-state resistance of the diode. Because of a small voltage difference of V_{in} and V_{C_i}, the peak current I_{ci} is fewer for the larger C_i. Thus, the larger capacitor is needed to cut down undesirable peak current and prolong the capacitor lifetime.

The analysis of switching loss is similar to the traditional cascaded H-bridge, while the capacitor losses consisting of ripple loss P_{rip} and conduction loss P_{cond} are newly introduced by the proposed inverter. When the capacitor C_i is connected from series to parallel, the ripple is derived by the difference between the input voltage V_{in} and the capacitor voltageV_{C_i}. The voltage ripple of C_i is

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$$\Delta V_{rip} = \frac{1}{C_i} \int_{t-}^{t+} i_{C_i} dt \qquad (9)$$

Where i_{Ci} is the transient current of the capacitor C_i, and the discharging interval is denoted by t_- and t_+. For C_1 in operational mode 1, t_- and t_+ are t_4 and t_5, respectively. For C_2 in operational mode 1, t_- and t_+ are t_3 and t_6, respectively. Thus, the loss from voltage ripple is resulted by

$$P_{rip} = \sum_{i=1}^{k} C_i \Delta V_{rip}^2 f_s \qquad (10)$$

Where,
k is the number of switched capacitors (SCs), and f_s is the frequency of the output voltage. It can be found that the ripple loss is inversely proportional to the capacitor C_i. The conduction losses can be further calculated by

$$P_{cond} = 2f_s \sum_{i=1}^{k} \int_{t-}^{t+} r_c i_{Ci}^2 dt \qquad (11)$$

The larger capacitor current leads to a large conduction loss. Lastly, the losses from SCs are denoted by

$$P_{sc} = P_{rip} + P_{cond}. \quad (12)$$

Both ripple loss and conduction loss are proportional to the frequency of the output voltage and number of capacitors. It is concluded that a larger capacitor can improve efficiency and prolong capacitor lifetime. However, the larger capacitor leads to the higher cost. Thus, a trade off of cost and efficiency need to be taken into account.

According to (4), (7), and (9), the relation curves of SCs (C_i) and ripple voltage are illustrated in Fig.4.3(a) with the fixed 25 kHz output frequency, and relation curves of SC (C_i) and output frequency are illustrated in Fig.5.2(b) with the fixed 10% ripple voltage.

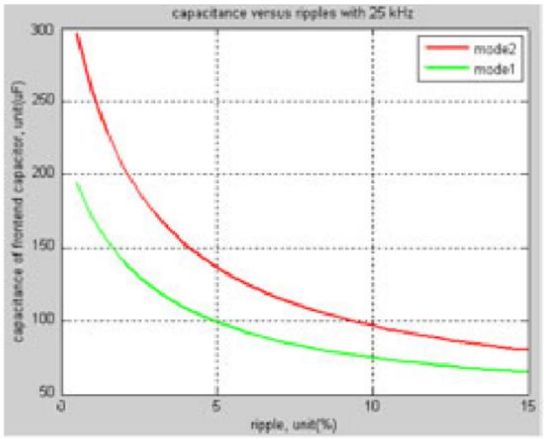


Fig.4.1 (a) Curves of Frontend Capacitor Versus Voltage Ripple with 25 kHz Output Frequency.

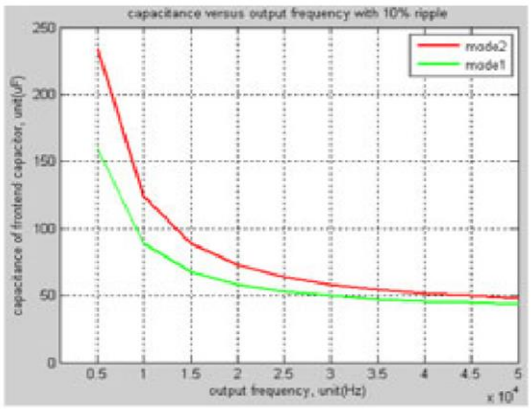


Fig.4.2 (b) Curves of frontend capacitor versus output frequency with 10% voltage ripple.

It can be found from Fig.4.3 (a) that the less capacitance leads to larger ripple voltage. Operational mode 2 needs larger capacitance than mode 1 to keep the ripples low. The gradient of capacitor to ripple is larger in low-ripple zone, and the gradient of capacitor to ripple is lower in high-ripple zone. The gradient variation is caused by inversely proportional relation between capacitance with ripple voltage. It can be found from Fig.4.3 (b) that the less capacitance is required for higher frequency applications to maintain 10% ripple voltage. Thus, capacitor cost can be greatly saved for HF application compared with low-frequency counterpart.

V. PERFORMANCE EVALUTION

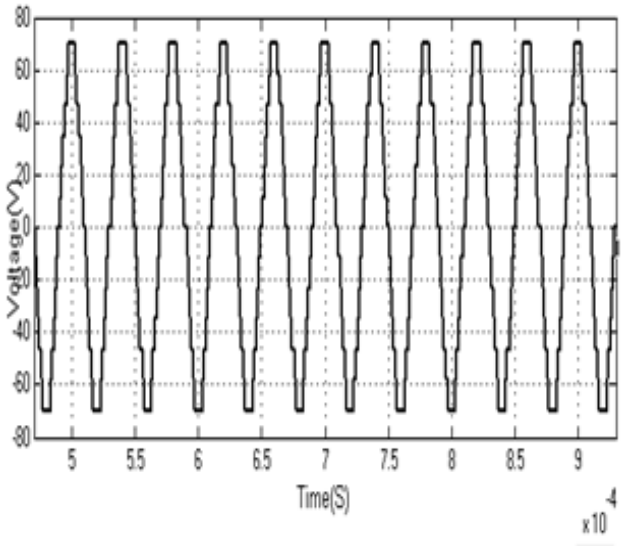
The SC based cascaded H-Bridge inverter for 13-level using phase shift carrier modulation are as shown in fig1 are developed in MATLAB/SIMULINK tool. The parameters of the SC based cascaded H-Bridge inverter are listed in table-III.

Table- III Parameters of the SC based Cascaded H-Bridge Inverter

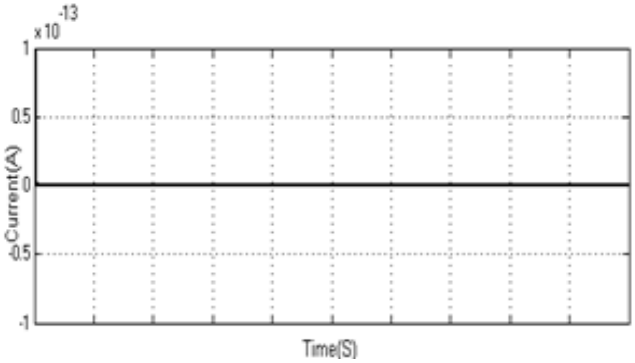
Inverter type	13-Level
Switching devices	18
Capacitors	3
Diodes	3
DC buses	3

The waveforms of output voltage v_o, capacitor currents (i_{C1}, i_{C2}, i_{C3}) and capacitor voltages (v_{C1}, v_{C2}, v_{C3}) are shown in Fig.6.1

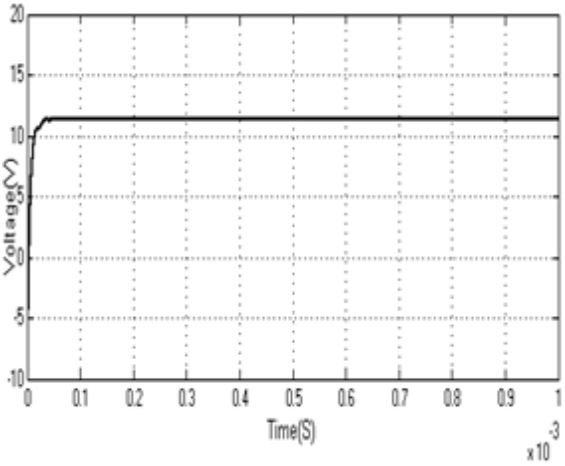
The waveforms for 13-level SC based cascaded inverter is taken as V_{in}=12v, C_1=100µf, C_2=120µf, C_3=220µf, Ro=50Ω. The output frequency f_s is 25 kHz.



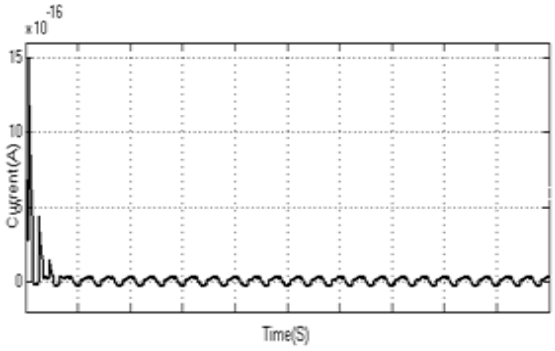
(a)Voltage (V_0) versus Time(S)



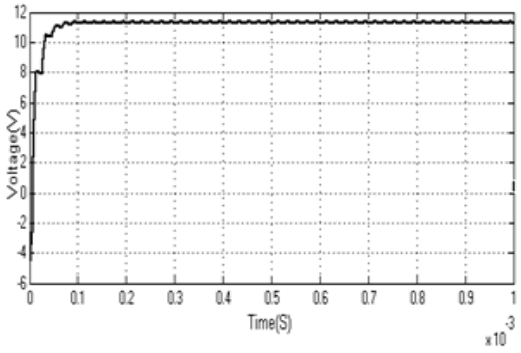
(b)Current (i_{c1}) versus Time(S)



(c)Voltage (V_{c1}) versus Time(S)

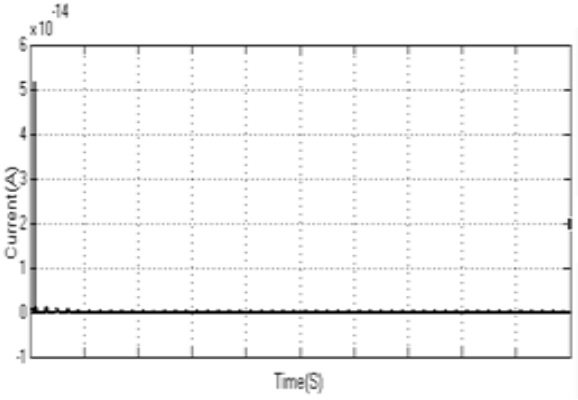


(d)Current (i_{c2}) versus Time(S)

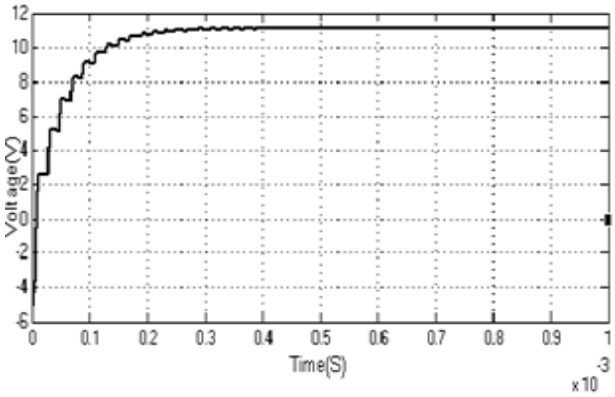


(e)

Voltage (V_{c2}) versus Time(S)



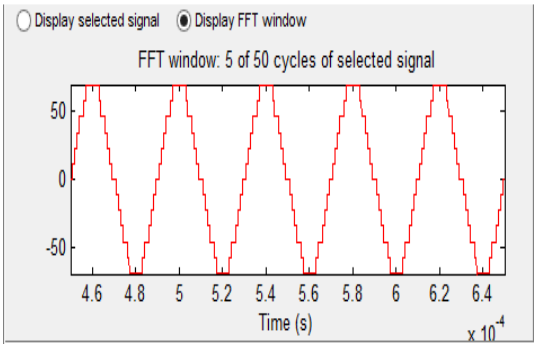
(f) Current (i_{c3}) versus Time(S)



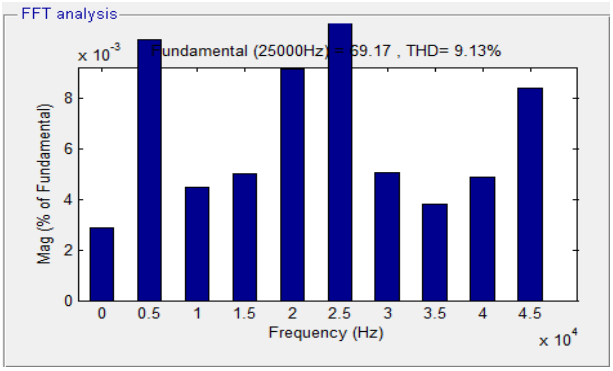
(g)Voltage (V_{c3}) versus Time(S)

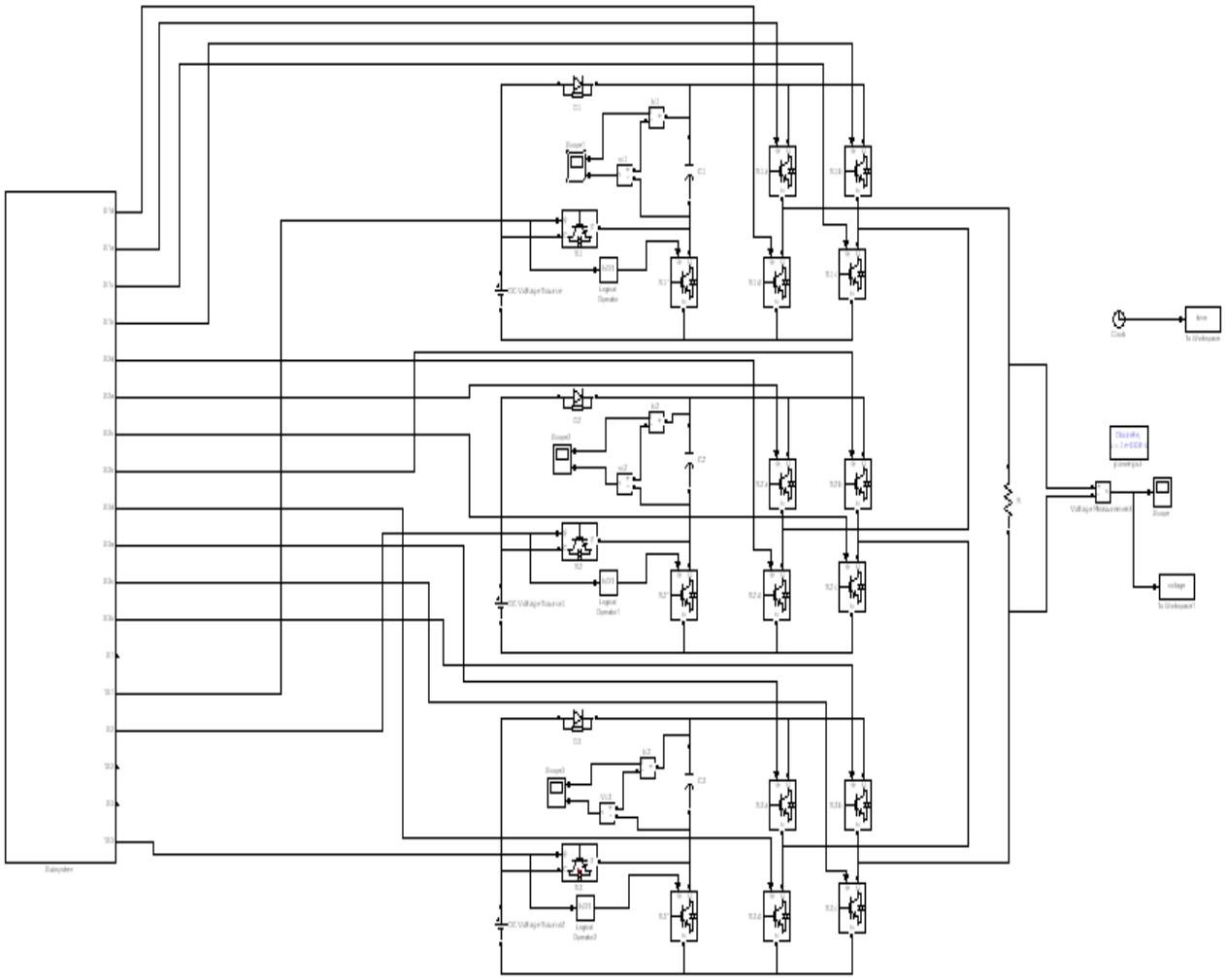
The Above Fig.5 Shows [a,b,c,d,e,f,g] In The Simulation waveforms of 13-level SC based cascaded inverter.

It can be found from Fig.5 that the voltage drop is indistinctive in each step of stair case output because the discharging periods of SCs become shorter for 13-level inverter. The output spectrums of 13-level inverter are illustrated in below Fig.6 respectively. The fundamental frequency is 25 kHz that is the same as output frequency. It can be observed that the fundamental harmonic is significantly higher than the other harmonics. The magnitude of fundamental component is 55V for a 13-level inverter.

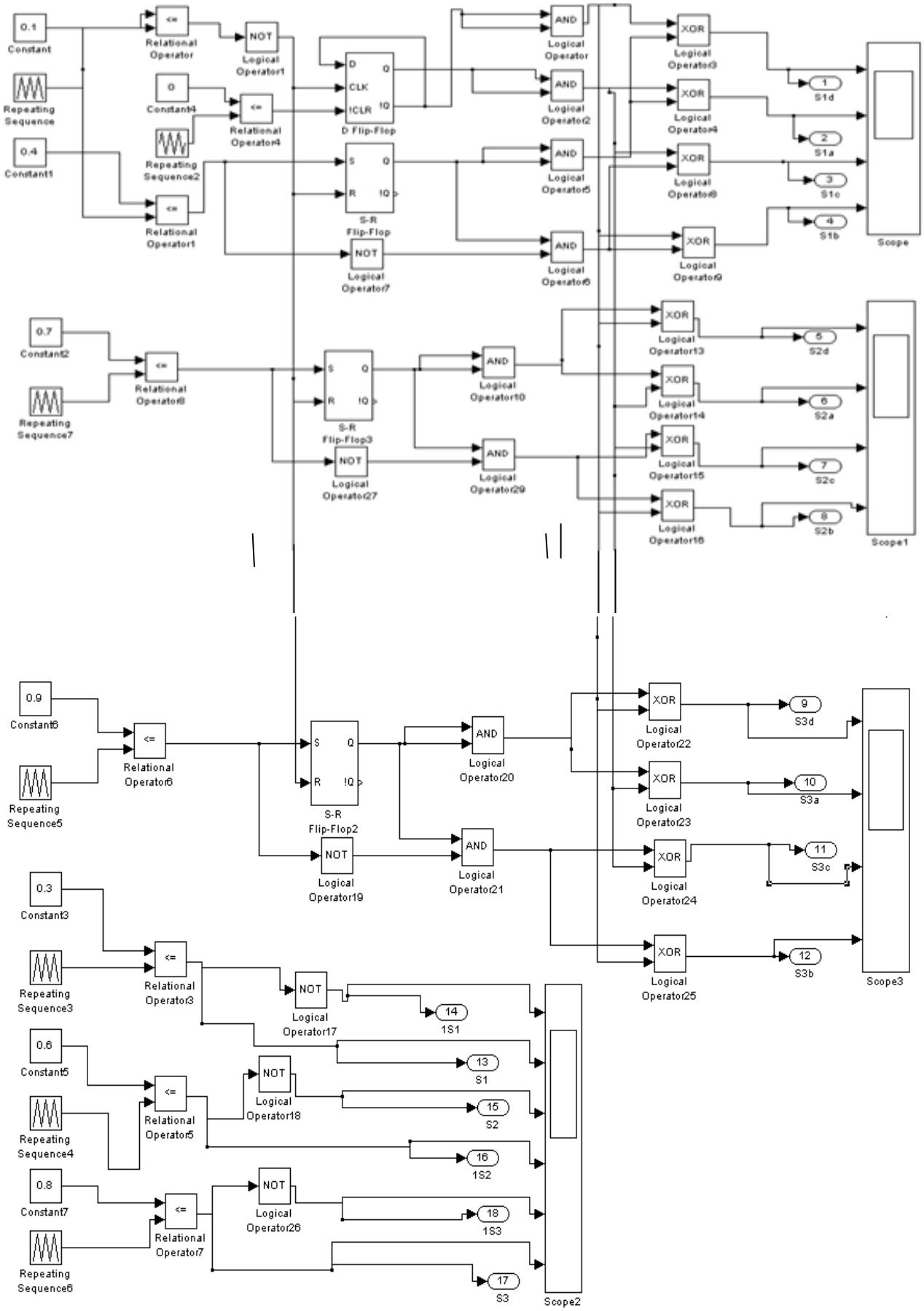


Output voltage & output spectrum of 13-level inverter The above fig.6 shows the Simulation waveforms of 13-level inverter The calculated THD 9.13% for 13-level inverter. A 13-level inverter has fewer high order harmonics than nine-level inverter. It can be estimated that the harmonics can be further cut down along with the increasing number of voltage levels. Thus, the proposed inverter produces near sinusoidal staircase output, and two methods can make it more sinusoidal. One is to optimize the duration of voltage levels; the other one is to increase the number of voltage levels.





MATLAB/Simulink for 13- level cascaded h-bridge inverter.



MATLAB/Simulink for 13- Level Cascaded h-Bridge Inverter for a Sub System.

VI. CONCLUSION

A novel SC-based cascaded multilevel inverter was proposed. 13-level circuit topology are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The accordant results of simulation further confirm the feasibility of proposed circuit and modulation method.

Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. For instance, the number of voltage levels increases three times in half cycle of 13-
level circuit. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. Meanwhile, the magnitude control can be accomplished by pulse width regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and fewer harmonics. This paper mainly analyzes 13-level inverters. The method of analysis and design is also applicable to other members of the proposed inverter. The proposed inverter can be applied to the electrical induction cooker.

FUTURE SCOPE OF WORK

The proposed inverter can also be applied to grid-connected photovoltaic system and electrical network of EV, because the multiple dc sources are available easily from solar panel, batteries, ultra capacitors, and fuel cells. The hardware can also be implemented to the proposed multilevel inverter for the given parameters in simulation.

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