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Performance Analysis of Devices in Double Gate MOSFET

Tanushree Debilata Das, Ramdulari Pradhan, Debabrata Singh, Adyasha Rath, Sonali Pattnaik

Abstract: ***The silicon CMOS technology moves into the sub-20nm regime and due to manufacturing limits the fundamental curb the traditional scaling of transistors. Rapid development in device structures and materials will be need for transistor miniaturization and improvement of performances. Device dimensions are approaching to their scaling limit rise to undesirable effects i.e. drain induced barrier lowering (DIBL), gate leakage current, short channel effects etc. Tri-Material Double Gate (DMDG) structure offers an alternative way of simultaneous SCE suppression and improved device performance by careful control of the gate material work function. We study and analyze the short channel effects (SCE), potential distributions, impact ionization, ion scattering, hot carrier effect and sub threshold swing. Analysis and comparative study of the electrical characteristics of DOUBLE GATE FETs shows that TMDG MOSFET exhibits better performance than DMDG and SMDG MOSFET in terms of surface potential, electric field, carrier mobility, and electron velocity to suppress the scaling effects like DIBL, HCEs etc.***

Keywords: ***Dual Material Double Gate FETs, Scaling, short channel effects (SCE), potential distributions, impact ionization, ion scattering, sub threshold swing.***

I. INTRODUCTION

As MOSFET scaling aggressively continues down to the sub-50 nm scale, single and double-gate (DG) devices on silicon-on-insulator (SOI) substrates are likely to replace conventional bulk devices. DG MOSFETs have an ultrathin and fully depleted SOI device geometry. In the DG MOSFETs, the inversion layer can be formed throughout the entire silicon film thickness. Therefore, due to dominance of the CMOS logic, to date the design efforts involving such novel devices have concentrated on the DG characteristics optimized for maximum saturation current and minimum leakage performance.

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***** Correspondence Author (s)
Tanushree Debilata Das*, Department of Electronics & Communication, ITER, S'O'A University, BBSR, Odisha, India. E-mail: tanushreedas.199537@gmail.com
Ramdulari Pradhan, Department of Electronics & Communication, ITER, S'O'A University, BBSR, Odisha, India. E-mail: ramdulari.pradhan@gmail.com
Debabrata Singh, Department of Computer Science & Information Technology, ITER, S'O'A University, BBSR, Odisha, India. E-mail: debabratasingh@soauniversity.ac.in
Adyasha Rath, Department of Computer Science & Information Technology, ITER, S'O'A University, BBSR, Odisha, India. E-mail: adyasharath1996@gmail.com
Sonali Pattnaik, Department of Electronics & Communication, ITER, S'O'A University, BBSR, Odisha, India, E-mail: sonalipatnaik82@gmail.com

By constantly reducing the gate length of the MOSFET devices for improving device performance, designers are gradually facing the constraints of the physical limitation of the device, such as short channel effects (SCEs). Therefore, reduction of the SCEs is assumed to play a major role in pushing the CMOS technology into the nanoscale regime. Hence, due to advances in gate material engineering, Dual material double gates (DMDG) MOSFETs have been investigated and are expected to suppress the SCEs [1]. The DMDG MOSFET has two laterally contacting gate materials with different work functions to achieve threshold voltage modulation and improved carrier transport efficiency [2].
Further-more, it induces a step potential at the interface between the different gate materials and creates a peak electric field in the channel region, which improves the carrier transit speed and increases the device driving capability [1]. To enhance immunity against the SCEs ,which results in device reliability in high performance circuit applications, a new nanoscale device structure, tri-material double-gate (TMDG) MOSFET ,is proposed .The TMDG MOSFET[16] is similar to a conventional single material DG SOI MOSFET [1] with the exception that the front gate of the TMDG structure involves three materials [3,4]. In addition, the material with the lowest work function as the gatematerial1 M1, is selected close to the drain as the screen gate and the material with the highest work function asthegate material 3 M3,is selected close to the source as the control gate, The main advantage of the TMDG SOI structure is to minimize the adverse SCEs.

Objectives

The main aim of this paper was to calculate the different types of the semiconductor devices. In order to achieve the aim, we imitate by Silvaco's Semiconductor TCAD tools and different types of intermediate aims were needed.

- Detailed description about each device and its applications.
- Implement the process of Silvaco's TCAD software and its use.
- Introduce a device design with reference material from Silvaco's website.
- Optimize the application.
- Change the parameters and result effects from the performance.
- Determine the optimized values for each device parameter.
- Combine the optimized parameters into a full and final optimized device.

The other paper is organized as follows. In the next phase, we described the related works and summarized the previous work.

Component design and device dimension for dual material double gate MOSFET structure described in section 3. Simulations and results of experiments are discussed in the section 4. In section 5, we conclude the work with some references.

II. RELATED WORKS

2.1. Surface Potentials

The surface potential ψs is the change in potential from bulk surface, where as the bulk potential is the change in potential from doped to intrinsic. The symbol ψs is used to signify the potential in the semiconductor measure relative potential at a position x deep inside the semiconductor .

2.2. Electric Fields

The two different electric field distributions occurred in the MOSFET structure are:

- The transverse field was caused by the potential difference between the conductive gate and the substrate. This field supports the substrate depletion region and inversion layer.
- The lateral field from non zero source to drain potential, and it is the main mechanism for current flow in the MOSFET.

In MOSFET when the channel is very sort (<0.1mm); the lateral electric field is very high and carrier drift velocities can reach their situation levels.Fig.1 describes Lateral and Transverse electric field of a MOSFET.

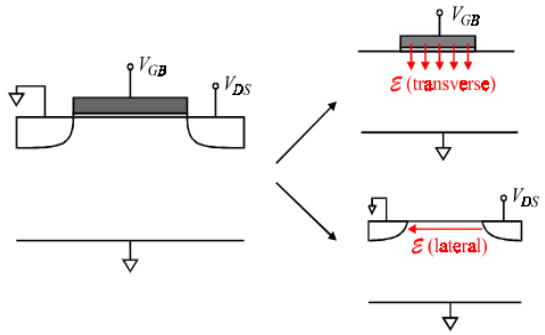

Fig .1. Lateral and Transverse electric field of a MOSFET

2.3. Metal Gates

Initially, poly-Si combination gate was considered as a pathway to improve gate leakage. However the theoretical data and experimental data show the degradation of mobility as compared to the use of metal gates. The work function varies due to different band alignments, depending on the gate dielectric.

3.1.1 Multiple Gates

Multi-gate MOSFETS realized on thin films are the promising devices for the ultimate integration of MOS[5] structures due to the volume inversion or volume accumulation in the thin layer (for enhancement-and depletion-type devices, respectively),which leads to an increase in the number and mobility of electrons and holes as well as driving current(additional gain in performance in loaded environment), the most favorable swing is the best control of short channel effects and off-state current , which is the main demand for future Nano-devices due to the power consumption crisis and the need to develop green/sustainable ICs.

3.1.2 Multi Material Gate

One of the most prominent ways to get rid of the hot carrier effect (HCE) is by using cascading gate structure consisting of two or more metals of different work-functions. This structure is commonly known as Double-Material –Gate (DMG) structure, proposed in 1999 by Long et. al.[3] or Triple –Material-Gate(TMG) proposed by Razavi et al[8]. The metal gates are cascading in a way that the gate near the source metal (M1) with higher work-function and the drain side metal (M2) is of relatively lower work-function. As a result of this, the electron velocity and the lateral electric field along the channel increased sharply at the interface of the two gate material which further gave results in the increased gate transport efficiency. Li Jin et. al .[12] described how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained –Si on insulator MOSFET[8]. Further, a step-like surface potential profile in the channel was created by the structure and thereby screening of the minimum potential point from drain voltage variations is ensured. The metal gate M1 is thus known as the control Gate (L1) and the metal M2 as the screen gate (L2).

2.4. Concept of Dual Material Gate MOSFET

In 1999, Long et. al. [7] proposed a new gate structure called the Double Material Gate (DMG)-MOSFET. Unlike the asymmetric structures employed doping engineering in which the channel field distribution is continuous, gate-material engineering with different work functions introduces a field of discontinuity along the channel, resulting in simultaneous transport enhancement and suppressed SCEs.

The two gate metals are so cascading that the gate near the source metal (M1) with higher work –function and the drain side metal (M2) is of relatively lower work function. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the two gate material which further results in the increase gate transport efficiency [11]. Li Jin et al. describes that how reduction of the HCE may be achieved by decreasing the control gate to screen gate ratio in a DMG strained-Si on insulator MOSFET [6][12]. Further, the structure creates a step-like surface potential profile in the channel and thereby ensures screening of the minimum potential point from drain voltage variations.

The metal gate M1 is thus rightfully known as the Control Gate and the metal M2 as the Screen Gate. Fabrication techniques for DMG CMOS [13-16] structure are presented in Fig 2. DMG CMOS device with the gate length of 55nm is already fabricated [15]. So, considering the development of the process technology over the years, the 30 nm DMG MOSFET can also be fabricated in the near future.

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2.5. Concept of Tri-Material Gate MOSFET

The research is based on tri-material gate was developed by Kirti Goel et.al 2006[3]. They presented a model and simulation of a nanoscale three-region tri-material gate stack MOSFET.

As MOSFET gate length are scaled down to sub-100 nm and gate oxide thickness to below nm, short channel effects (SCEs) such as [18]:

1. Increase in effective gate oxide thickness (EOT) due to polysilicon gate depletion.
2. Threshold voltage change due to boron penetration from p+ polysilicon gate into the channel region
3. Degradation of device reliabilty due to gate leakage current
4. Reduced gate controllability due to drain-induced barrier lowering (DIBL) becomes predominant.

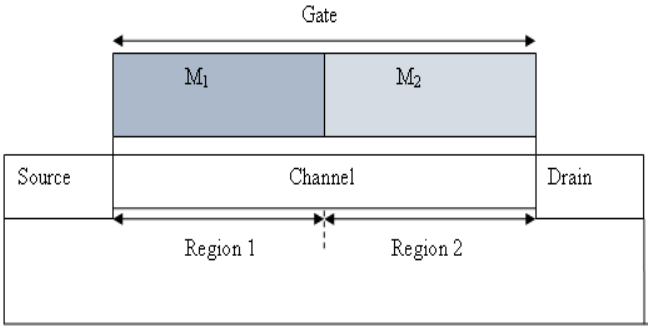

Fig. 2. Basic DMG MOSFET Structure

These SCEs needs to be eliminated or minimize for proper device operation. By replacing the polysilicon gate to metal gates, it will eliminate polysilicon depletion width effects and polysilicon doping penetration. In this research, the tri-material gate structure was proposed by taking three different metal gates as gate oxide [19]. The reason of replacement of the polysilicon gates by different metal gates in their structure was reduced to the polysilicon depletion width effects and also to simplify the model of metal gate [18].

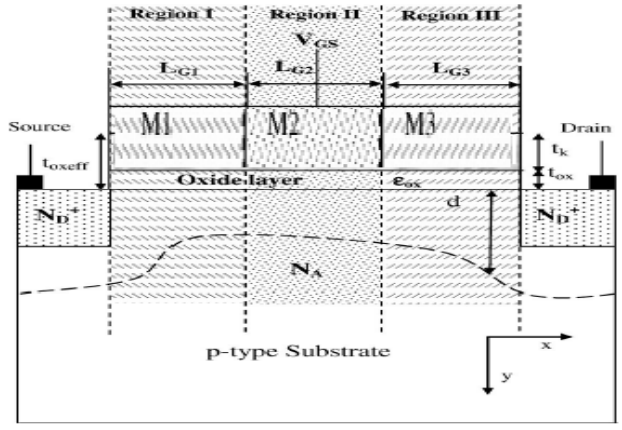

Fig.3. Schematic structure of the tri-material gate MOSFET [24]

Fig. 3. shows the structure of tri-material gate MOSFET with M1, M2 and M3 of gate length Lg1, Lg2, and Lg3, respectively. For device simulation, used the gate length ratio Lg1:Lg2:Lg3=1:1:1, and gate length Lg=Lg1+Lg2+Lg3.

2.6. Concept of Dual Material Double Gate MOSFET

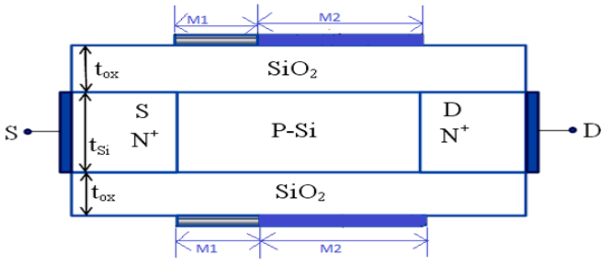

Fig.4. Structure of the dual material double gate MOSFET

To incorporate the advantages of both DG and DMG structures, a new structure is proposed i.e. Dual-Material Double-Gate (DMDG) SOI MOSFET as shown in Fig.4. The structure illustrates that it is similar to an asymmetrical DG SOI MOSFET, with the exception that the front gate of the DMDG structure consists of two materials (p+ poly and n+ poly). Using two-dimensional simulation, the reduced short channel effect exhibited by the DMDG structure below 100nm, achieves a higher Trans conductance and reduced drain conductance compared to the DG SOI MOSFET. Thus this proposed structure exhibits the desired features of both the DMG and the DG structures. The structure also demonstrates a considerable reduction in the peak electric field near the drain end, increased drain breakdown voltage, improved trans conductance, reduced drain conductance and a desirable threshold voltage “roll-up” even for channel lengths far below 100 nm.

2.6.1. Concept of Tri-Material Gate MOSFET

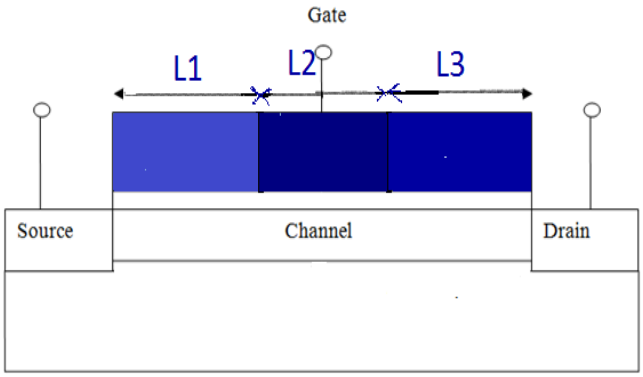

Fig.5. Structure of the Tri-material gate MOSFET

To enhance the immunity against short channel effects, a new structure called tri-material gate (TMG) MOSFET is proposed as in Fig. 5. This has 3 metals in the gate M1 & M2 & M3 with different work functions. This proposed structure has two steps in a surface potential profile which is advantageous for simultaneous suppression of short channel effects and improvements of carrier transport efficiency [20, 21]. This structure having steps in surface potential profile thus provides reduced electric field at the drain and exhibiting smaller Hot carrier effect(HCE)’s.

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III. COMPONENT DESIGN

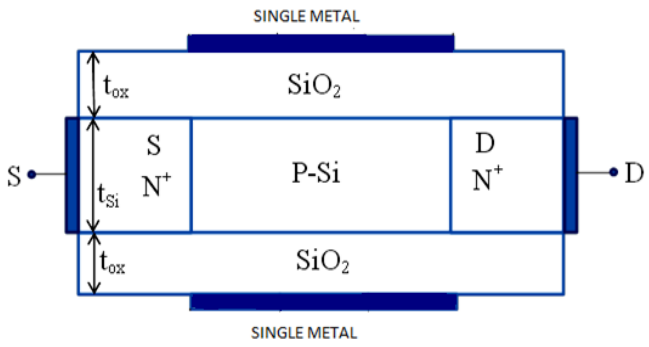

Fig.6. Single Metal Double Gate MOSFET

The schematic cross sectional view of a planar-channel DG-MOSFET is illustrated in Fig. 6. Here asymmetric device structure has been considered. Source and drain extensions are 20 nm long from the edges of the gates with metal contacts vertically placed at their ends. The channel doped as p-type $1x10^{18}cm^{-3}$and the source/drain as heavily doped n-type$1x10^{20}cm^{-3}$ to reduce the effect of mobility degradation by coulomb scattering .The structure has been calibrated to meet the requirement of international technology roadmap for semiconductors(ITRS) for 60 nm physical gate length. Channel thickness (t_{si}) is taken as 10nm. Thickness SiO_2 (t_{ox}) is taken as 2nm. Gate Work Function is taken as 4.8 eV.

3.1. Device Dimension for Dual Material Double Gate MOSFET

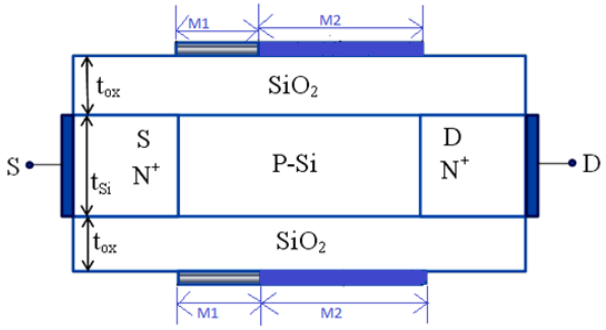

Fig.7. Unsymmetrical Dual Metal Double Gate MOSFET

The schematic cross sectional view of a planar-channel DG-MOSFET is shown in Fig. 7. In this asymmetric device structure has been considered. Source and drain extensions are 20 nm long from the edges of the gates with metal contacts vertically placed at their ends. The channel doped as p-type $1x10^{18}cm^{-3}$and the source/drain as heavily doped n-type $1x10^{20}cm^{-3}$ to reduce the effect of mobility degradation by coulomb scattering .The structure has been calibrated to meet the requirement of international technology roadmap for semiconductors(ITRS) for 60 nm physical gate length. Channel thickness (t_{si}) is taken as 10nm. Thickness SiO_2 (t_{ox}) is taken as 2nm. Gate Work Function is taken as 4.8 eV for metal gate M_1 and gate work function is taken as 4.6 eV for metal gate M_2.

3.2. Device Dimension for Tri-Material Double Gate MOSFET

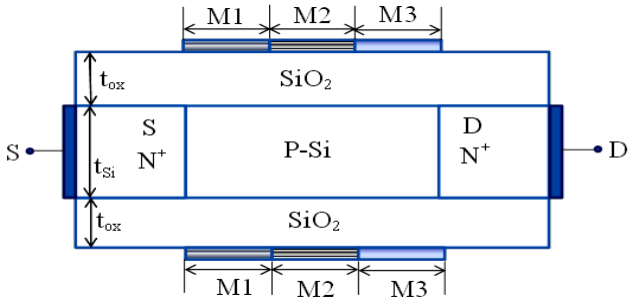

Fig. 8. Tri Metal Double Gate MOSFET

The schematic cross sectional view of a planar-channel DG-MOSFET is illustrated in Fig. 8. In this asymmetric device structure has been considered. Source and drain extensions are 20 nm long from the edges of the gates with metal contacts vertically placed at their ends. The channel doped as p-type $1x10^{18}cm^{-3}$and the source/drain as heavily doped n-type$1x10^{20}cm^{-3}$ to reduce the effect of mobility degradation by coulomb scattering .The structure has been calibrated to meet the requirement of international technology roadmap for semiconductors (ITRS) for 60 nm physical gate length. Channel thickness (t_{si}) is taken as 10nm. Thickness SiO_2 (t_{ox}) is taken as 2nm. Gate Work Function 4.8 eV for metal gate M_1, work function taken as 4.6eV for metal gate M_2 and for metal gate M_3 work function is taken as 4.4 eV.

IV. TESTING PARAMETERS AND SIMULATION

Table.1. Device Dimensions for Tri-material Double GATE MOSFET

Attributes	Value
Channel Length (L)	60 nm
Channel thickness (t_{si})	10 nm
Thickness SiO_2 (t_{ox})	2 nm
Channel Doping (N_A)	$1x10^{18}$ cm^{-3}
S/D Doping (N_D)	$1x10^{20}$ cm^{-3}
Gate Work Function	4.8ev(M1), 4.6ev(M2), 4.4ev(M3)

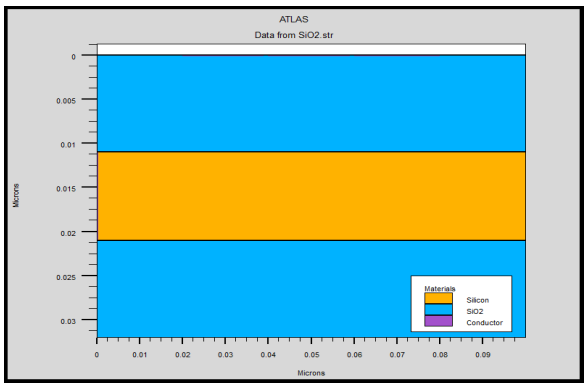

Fig. 9. Describes the Simulation Results of Tri-material i.e. Silicon, Sio2, Conductor in DG MOSFET

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4.1. Parameter Analysis of Devices

Fig.10. illustrates that the shift in the point of the minimum potential is almost fixed regardless of the applied drain bias [Fig.10. V_{DS}=0.1V].Here the figure indicates that the DIBL effect is considerably reduced for tri-material gate compare to dual material gate and single material gate.

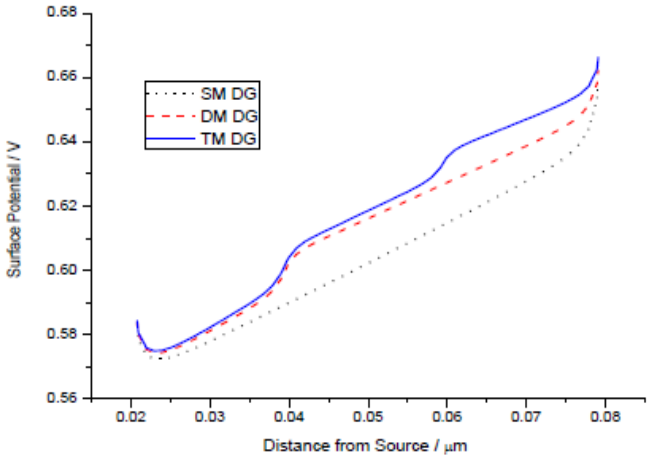

Fig. 10.The surface channel potential along the channel for TMG, DMG and SMG.

It is shown that the slope of surface potential to the drain side for tri-material gate stack MOSFET is much smaller than that for single-material gate(SMG) MOSFET and double material gate(DMG) MOSFET. It implies that in comparison to single-material gate (SMG) MOSFET and double material gate (DMG) MOSFET, the tri-material gate (TMG) MOSFET can effectively reduce the electric field near the drain side and exhibits a strong immunity to SCE induced by the increased drain voltage.

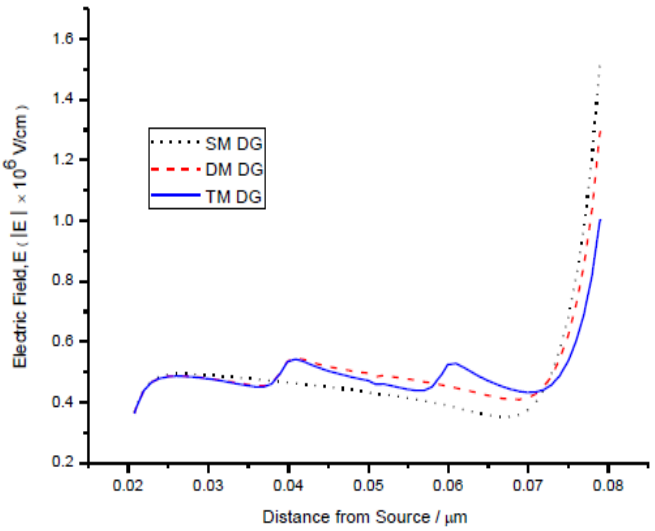

Fig.11. Horizontal surface electric field

The surface horizontal electric field in the top channel is illustrated in Fig. 11 at V_{DS}=0.1V. It is observed that the tri-material gate (TMG) will induce the peak of electrical field along with the channel compared to that of dual material gate (DMG) and single material gate (SMG) hence increasing the carrier velocity and improves the device speed. However, the single gate material (SMG) will induce the large electric field near the drain side compared to that of dual material gate (DMG) and tri-material gate (TMG) and enhance the hot carrier effects that degrade the device performance.

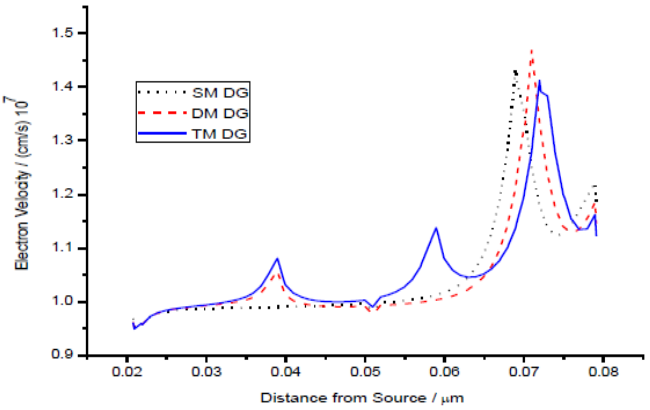

Fig.12. Distribution for the carrier velocity in the top channel

Fig. 12 shows the distribution for the carrier velocity in the top channel of the tri-material gate (TMG), dual material gate (DMG) and single material gate (SMG) like that of electric field at Vds=0.1V.Here it is also observed that the tri-material gate (TMG) will induce the peak of electron velocity along with the channel compare to that of dual material gate (DMG) and single material gate (SMG). Hence increase in the carrier velocity for the tri-material gate (TMG) improves the device speed. However, the single gate material (SMG) will have the large electron velocity near the drain side compare to that of dual material gate (DMG) and tri-material gate (TMG) and enhance the hot carrier effects that degrade the device performance.

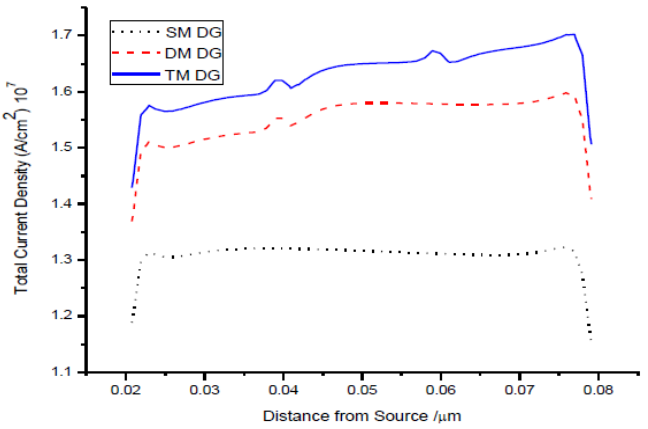

Fig.13. Total current density along the top channel of TMG, DMG and SMG at V_{DS}=.1V

We need higher current density for better switching application. Fig. 13 illustrates total current density along the top channel of TMG, DMG and SMG DG MOSFETs [Fig. 13 at V_{DS}=.1V].It is observed from the figure that tri-material gate (TMG) DG MOSFET gives higher total current density compared to that of dual material gate (DMG) and single material gate (SMG) which is better for faster switching applications. It is observed from the Fig. 13.

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that in case of tri-material DG MOSFET we are having two peaks which conclude that the carrier mobility is faster in the channel region compare to that of dual material DG MOSFET and single material DG MOSFET.

V. CONCLUSION

The work proposes the device performance of double gate MOSFET. From the result of simulation, it is shown that TMDG MOSFET exhibits better performance than DMDG and SMDG MOSFET in terms of surface potential, electric field, carrier mobility, and electron velocity to suppress the scaling effects like DIBL, HCEs etc. The developed 2-D analytical model for surface potential and threshold voltage analyses the effectiveness of TMDG structure in an on substrate to suppress the hot carrier effects (HCEs) and drain induced barrier lowering (DIBL). The suppression of HCE and DIBL by the introduction of the tri-material gate is attributed to the creation of a step-function in the channel potential profile which is verified by the simulations.

An extensive analysis of the impact of numerous device parameters on the threshold voltage has been carried out. It may be concluded that the depreciation in the threshold voltage with increasing strain is improved by increasing the length of control gate for the given channel length and increasing the thickness. The derived 2-D analytical model is found to be in excellent agreement with the simulation results obtained from ATLAS™ from Silvaco. The developed model may prove to a useful tool to optimize the desired performance of the device parameters.

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