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Design of MIPS based 64-bit RISC Processor

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Abstract: ***A major paradigm shift where power dissipation has become an important consideration as performance and area. RISC is termed as Reduced Instruction Set Computer, computer arithmetic-logic unit that uses a minimal instruction set, emphasizing the instructions used most often and optimizing them for the fastest possible execution In this work, a 64 bit RISC processor is presented with higher performance and efficiency being the main aim. This processor comprises of Control unit, general purpose registers, Arithmetic and logical unit, shift registers. Control unit follows instruction cycle of 3 stages fetch, decode and execute cycle. According to the instruction to the fetch stage, control unit generate signal to decode the instruction. The architecture supports 16 instructions for arithmetic, logical, shifting and rotational operations.***

Keywords: RISC, control unit, ALU, shift register, instruction cycle.

I. INTRODUCTION

Now a days, Computers are mainstream in quotidian activities. RISC Processor is a CPU design strategy that uses simplified instructions for higher performance with faster execution of instruction. It also reduces the delay in execution. It uses general instructions rather than specialized instructions. They are less costly to design, test and manufacture. This has helped in implementation of RISC in technological field. Its range of application includes signal processing, convolution application, supercomputers such as K computers and wider base for smart phones.

In conventional approach system consumes too much of power. The power reduction in conventional RISC processor is done at fabrication step itself, but which is too complex process. Here utilization of chip area is more and the system consumes more power leads to increased performance. To overcome this disadvantage low power RISC Architecture is designed with less number of gates. Low power design means reducing the power consumption. We have took this project to design such an architecture of RISC processor in which we can perform certain number of operations with less power and more reliability using clock constraints. Even low power helps in less heat dissipation. Processors with pipelining consists of modules internally which can work on microinstructions separately. Each stage in the pipeline is linked to next stage by flip-flops, through this the overall processing time is reduced as output of previous stage acts as an input to next stage. An instruction pipeline is said to be fully pipelined if it accept a new instruction every clock cycle.

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The proposed processor is 64 bit low power RISC processor with pipelining architecture which gets instructions on a regular basis using dedicated buses to its memory, executes all its native instructions in stages with pipelining. It can communicate with external devices with its dedicated parallel IO interface.

II. LITERATURE REVIEW

- RISC, or Reduced Instruction Set Computer. is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other types of architectures.
- Reduced instruction set computing, or RISC (pronounced 'risk'), is a CPU design strategy based on the insight that a simplified instruction set (as opposed to a complex set) provides higher performance when combined with a micro-processor architecture capable of executing those instructions using fewer microprocessor cycles per instruction. A computer based on this strategy is a reduced instruction set computer, also called RISC. The opposing architecture is called complex instruction set computing, i.e. CISC.

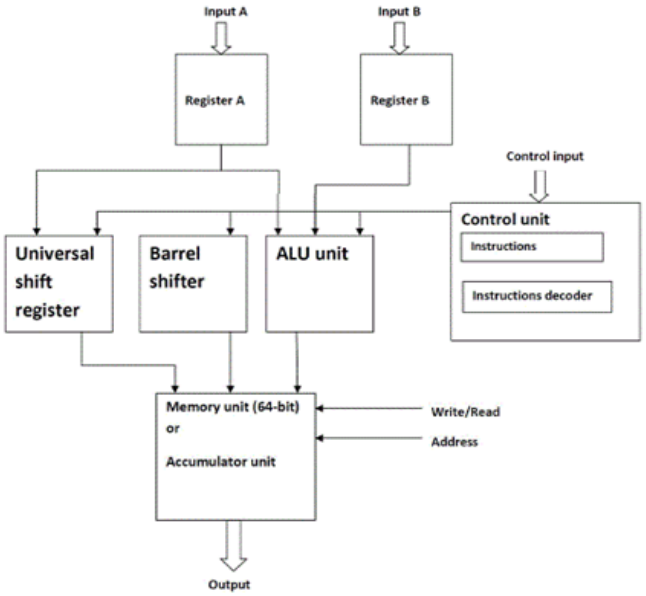

Figure 1.Architecture of 64 bit RISC processor

The architecture of 64 bit RISC processor comprises of Control unit, general purpose register, ALU, Barrel shifter, universal shift register and accumulator. The control unit consists of two registers i.e. instruction register and instruction decoder. Instruction and data are fetched sequentially in order to reduce the latency in the machine cycle. Pipeline structure has been incorporated that further utilizes three execution cycle fetch, decode and execute.

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This pipeline structure helps in enhancing the speed of operation. In fetch cycle, instruction and relevant data are inferred from the memory while in decode cycle, instruction and data drawn from the memory are bifurcated to activate component and data path for execution and in the execution cycle instruction is executed, data is manipulated and result is stored in the accumulator. The control unit accepts the opcode and generate the signal that triggers the components and data path to work accordingly and perform the desired function. The control unit has two instruction decoders. These two decoders decode the instruction bits and direct the signal to either into ALU, universal shift register or barrel shift rotator. The operands are received from register A or register B. Upon receiving the operands from registers and the decoded instruction bits arithmetic and logical unit perform arithmetic and logical functions. Universal shift register and barrel shift rotator receives the input from register A and depending upon the decoded information perform the desired operation of either shifting or rotation and the result is stored in the accumulator register. Modules are the building blocks of a Processor. This segment deals with the modules of 64 bit RISC processor.

III. SCOPE OF THE THESIS

Processors with pipelining consists of modules internally which can work on microinstructions separately. Each stage in the pipeline is linked to next stage by flip-flops, through this the overall processing time is reduced as output of previous stage acts as an input to next stage. An instruction pipeline is said to be fully pipelined if it accept a new instruction every clock cycle. The proposed processor is 64 bit low power RISC processor with pipelining architecture which gets instructions on a regular basis using dedicated buses to its memory, executes all its native instructions in stages with pipelining. It can communicate with external devices with its dedicated parallel IO interface.

Table 1: Comparison Between RISC and CISC

RISC vs. CISC

CISC	RISC
Emphasis on hardware	Emphasis on software
Multiple instruction sizes and formats	Instructions of same set with few formats
Less registers	Uses more registers
More addressing modes	Fewer addressing modes
Extensive use of microprogramming	Complexity in compiler
Instructions take a varying amount of cycle time	Instructions take one cycle time
Pipelining is difficult	Pipelining is easy

IV. METHOD OF IMPLEMENTATION

MIPS is the most elegant among the effective RISC architectures; even the competition thought so, as evidenced by the strong MIPS influence to be seen in later architectures like DEC's Alpha and HP's Precision. Elegance by itself doesn't get you far in a competitive marketplace, but MIPS microprocessors have generally managed to be among the most efficient of each generation by remaining among the simplest. Relative simplicity was a commercial necessity for MIPS Computer Systems Inc., which spun off in 1985 from an academic project to make and market the chips. As a result, the architecture had (and perhaps still has) the largest range of active manufacturers in the industry—working from ASIC cores (MIPS Technologies, Philips) through low-cost CPUs (IDT, AMD/ Alchemy) to the only 64-bit CPUs in widespread embedded use (PMC-Sierra, Toshiba, Broadcom). At the low end the CPU has practically disappeared from sight in the "system on a chip"; at the high end Intrinsity's remarkable processor ran at 2 GHz—a speed unmatched outside the unlimited power/heat budget of contemporary PCs. ARM gets more headlines, but MIPS sales volumes remain healthy enough.

100 M MIPS CPUs were shipped in 2004 into embedded applications. The MIPS CPU is one of the RISC CPUs, born out of a particularly fertile period of academic research and development. RISC (Reduced Instruction Set Computing) is an attractive acronym that, like many such, probably obscures reality more than it reveals it. But it does serve as a useful tag for a number of new CPU architectures launched between 1986 and 1989 that owe their remarkable performance to ideas developed a few years earlier in a couple of seminal research projects. Someone commented that "a RISC is any computer architecture defined after 1984"; although meant as a jibe at the industry's use of the acronym, the comment is also true for a technical reason—no computer defined after 1984 can afford to ignore the RISC pioneers' work. One of these pioneering projects was the MIPS project at Stanford. The project name MIPS (named for the key phrase "microcomputer without interlocked pipeline stages") is also a pun on the familiar unit "millions of instructions per second."

The Stanford group's work showed that pipelining, although a well-known technique, had been drastically underexploited by earlier architectures and could be much better used, particularly when combined with 1980 silicon design.

Pipe lines:- Once upon a time in a small town in the north of England, there was Evie's fish and chip shop. Inside, each customer got to the head of the queue and asked for his or her meal (usually fried cod, chips, mushy peas,1 and a cup of tea). Then each customer waited for the plate to be filled before going to sit down. Evie's chips were the best in town, and every market day the lunch queue stretched out of the shop. So when the clog shop next door shut down, Evie rented it and doubled the number of tables.

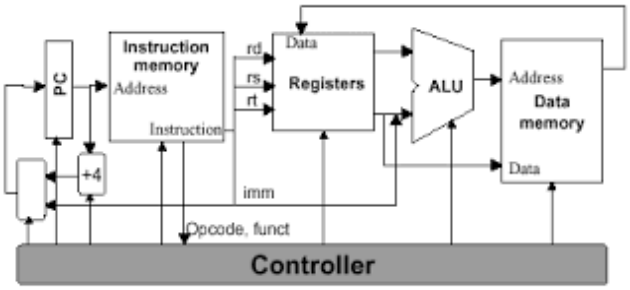

Figure2. MIPS Architecture

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But they couldn't fill them! The queue outside was as long as ever, and the busy townsfolk had no time to sit over their cooling tea. They couldn't add another serving counter; Evie's cod and Bert's chips were what made the shop. But then they had a brilliant idea. They lengthened the counter and Evie, Bert, Dionysus, and Mary stood in a row.

As customers came in, Evie gave them a plate with their fish, Bert added the chips, Dionysus spooned out the mushy peas, and Mary poured the tea and took the money. The customers kept walking; as one customer got the peas, the next was already getting chips and the one after that fish. Less hardy folk don't eat mushy peas—but that's no problem; those customers just got nothing but a vacant smile from Dionysus. The queue shortened and soon they bought the shop on the other side as well for extra table space. That's a pipeline. Divide any repetitive job into a number of sequential parts and arrange them so that the work moves past the workers, with each specialist doing his or her part for each unit of work in turn. Although the total time any customer spends being served has gone up, there are four customers being served at once and about three times as many customers being served in that market day lunch hour. Evie's organization, as drawn by her son Einstein in a rare visit to non virtual reality.2 Seen as a collection of instructions in memory, a program ready to run doesn't look much like a queue of customers. But when you look at it from the CPU's point of view, things change.

The CPU fetches each instruction from memory, decodes it, finds any operands it needs, performs the appropriate action, and stores any results—and then it goes and does the same thing all over again. The program waiting to be run is a queue of instructions waiting to flow through the CPU one at a time. The various different jobs required to deal with each instruction already require different specialized chunks of logic inside the CPU, so building a pipeline doesn't even make the CPU much more complicated; it just makes it work harder. The use of pipelining is not new with RISC microprocessors. What makes the difference is the redesign of everything—starting with the instruction set— to make the pipeline more efficient.

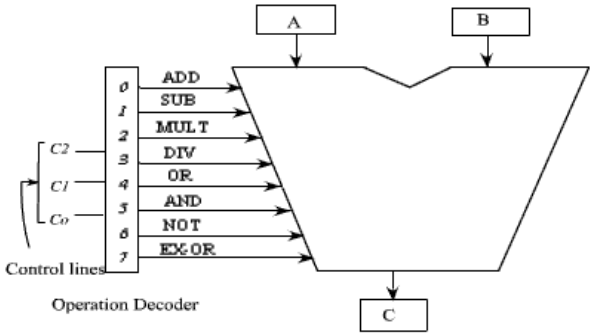

Figure 3. ALU

V. POWER_ANALYSIS

Power analysis and estimation is available throughout the design process, as shown in the following figure:

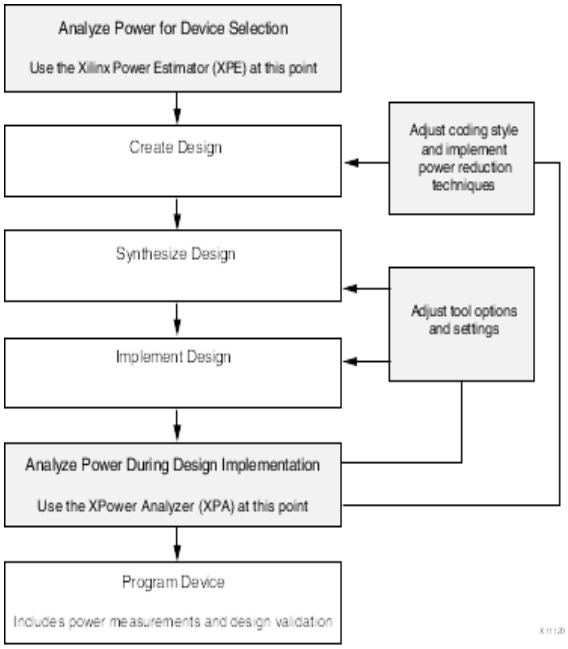

Figure 4: Flow Chat for Power Analysis

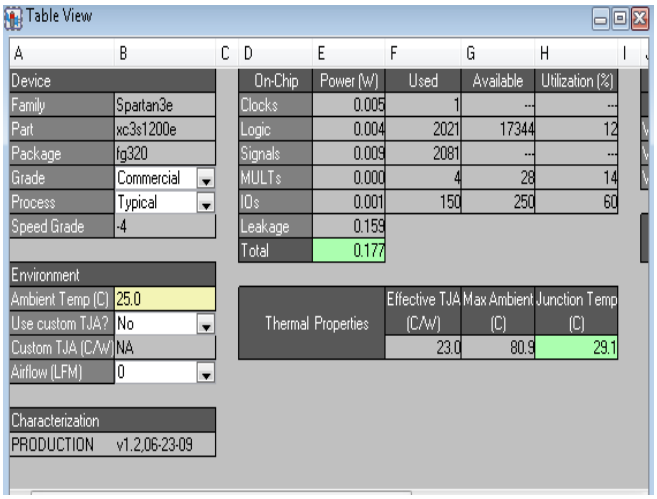

Figure 5: Power Overview

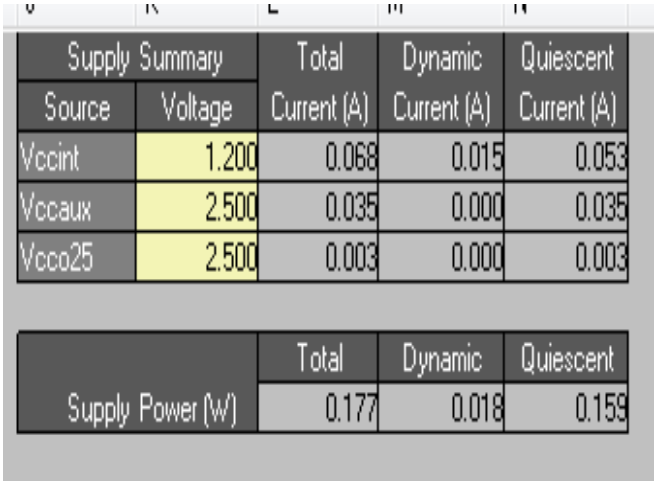

Figure 6: Final Power Obtained

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VI. CONCLUSION

Application of low power methodology to MIPS processor reduces 90% of the total power and makes it more efficient. Though there is 27% increase in area the efficiency of the processor in terms of power makes it an ideal system. Cadence tool and Xilinx were used to verify the output. The project is advanced by the utilization of Hazard Detection Unit, Uses low power technique and MIPS instruction Set. Hence the justification is done to the name of the project.

FUTURE SCOPE

The above developed design can be reduced further using system portioning. Consumption of the power can further be reduced at the manufacturing stage using lithography.

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