

Passive Voltage Contrast Technique for Semiconductor Device Analysis

C. Ramachandra, J. Venkatesh, Sarat Kumar Dash

Abstract: Passive voltage contrast is found to be very effective in localizing defect / fault at micron / submicron scale in semiconductor devices. It requires use of Focused Ion Beam (FIB) System for analysis. Effectiveness of passive voltage contrast in identifying fault location is explained with case studies in DRAM devices.

Keywords: PVC, FIB, SEM, IC, DRAM, DLCT, BPSG, ILD, RIE, GDS,

I. INTRODUCTION

Integrated circuits / semiconductor devices are of multi layer structures typically having nearly 20 layers confined in less than ten microns. Typical layers found in an IC are depicted in Figure 1.

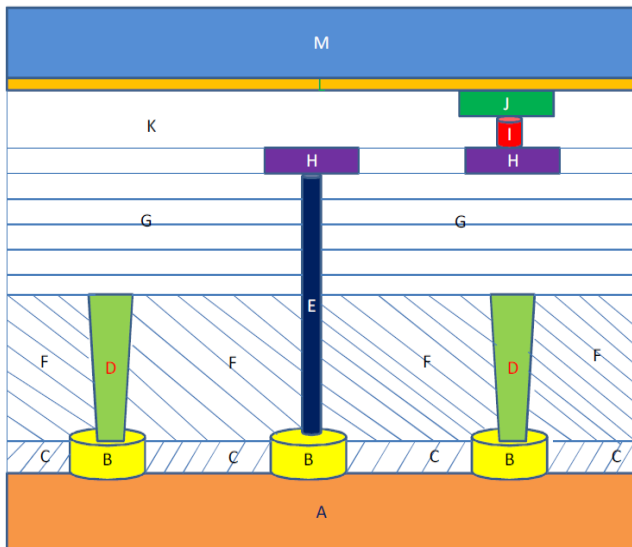


Figure 1

A: Silicon, B: Poly plug, C: BPSG 1, D: Memory Cells, E: DLCT
F: BPSG 2, G: BPSG 3, H: M1, I: Via, J: M2, K: ILD, L: Passivation
M: Polyimide

The technology node has shrunk in the last four decades from 10 microns to sub micron as shown in the table 1:

Table: 1

Technology Node	Year	Technology Node	Year
10.00 microns	1971	0.18 micron	1999
6.00 microns	1974	0.15 micron	2000
3.00 microns	1977	0.13 micron	2001
1.50 microns	1982	90 nm	2004
1.00 micron	1985	65 nm	2005
8.0 0 micron	1989	45 nm	2008
0.60 micron	1994	32 nm	2011
0.35 micron	1995	22 nm	2014
0.28 micron	1997	20 nm	2017

As a result, defects at micron / submicron scale can play significant role in degrading performance of the device. These defects can be buried in any of the layers. Localization of the defects is one of the challenges in semiconductor industry in understanding root cause of the failure.

II. PASSIVE VOLTAGE CONTRAST

Study of PVC requires decapsulation and polyimide layer removal. Decapsulation of semiconductor device is carried out using dual acid decapsulator. Polyimide layer has been stripped off using oxygen plasma in Reactive Ion Etching system. Figure 2 shows SEM image of DRAM after decapsulation and polyimide removal.

It is important to ensure no damage or degradation to wire bonds and no contamination on the surface of interest after decapsulation and polyimide removal..

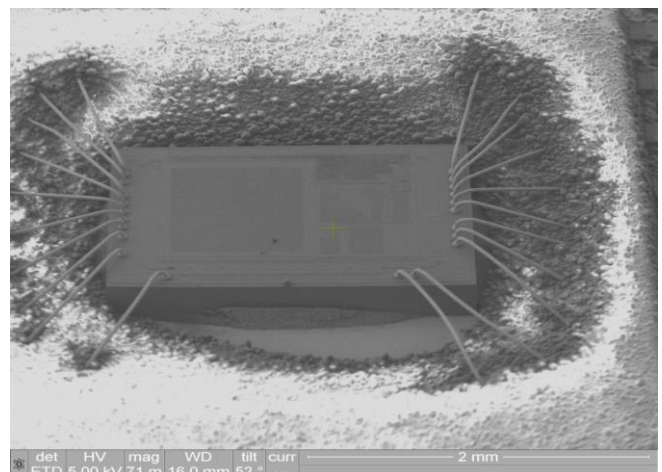


Figure 2: SEM Image of DRAM after Decapsulation and Polyimide Removal.

Manuscript published on 30 October 2017.

* Correspondence Author (s)

Dr. C. Ramachandra, Professor, School of Sciences, Jain University, Bangalore – 560011, India.

Dr. J. Venkatesh, Professor, School of Sciences, Jain University, Bangalore – 560011, India.

Dr. Sarat Kumar Dash, Scientist, ISRO Satellite Centre, Bangalore – 560017, India.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license <http://creativecommons.org/licenses/by-nc-nd/4.0/>

Passive Voltage Contrast Technique for Semiconductor Device Analysis

Interaction of focused ion beam with the semiconductor sample leads to generation of secondary electrons. These secondary electrons play a key role in forming topographical image of the sample. The selected / interested area of the device is scanned through focused ion beam (usually containing Ga^+ ions). Any circuit element / structure which are floating appear to be relatively darker. This is because in the floating structure positive ions of gallium accumulate which prevents secondary electrons from reaching the detector. This selective contrast becomes a powerful tool in localization of the fault.

The schematic view of a FIB system is shown in the figure 3. The sample in high vacuum is scanned by a focused ion beam. Interaction of ion beam with sample leads to generation of secondary electrons. These secondary electrons are collected by a detector. Grey level of the image is determined by amount of secondary electrons collected from the given point. Amount of secondary electrons emitted from a given point is a function of material, topographical feature and local bias. In semiconductor devices, most of the materials have planar structures. Hence local bias play significant role in determining grey level of the image. More the positive bias, lesser the number of secondary electrons are able to reach the detector and more darker the given point in the image.

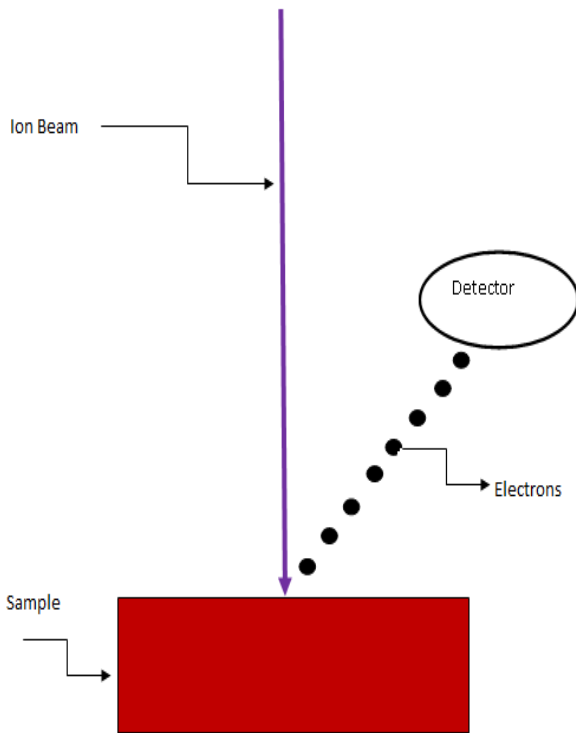


Figure 3: Sample Exposed to Focused Ion Beam.

Realization of PVC is depicted through Figures 4 and 5. Metal 2 is exposed through ion milling in the known location using GDS data. The metal 2 (Aluminium) appears quite bright (See Fig 4) compared to adjacent locations having oxide / BPSG layers. Part of the metal 2 is then milled through using Ion beam as shown in Figure 5. The floating metal structure now appears darker.

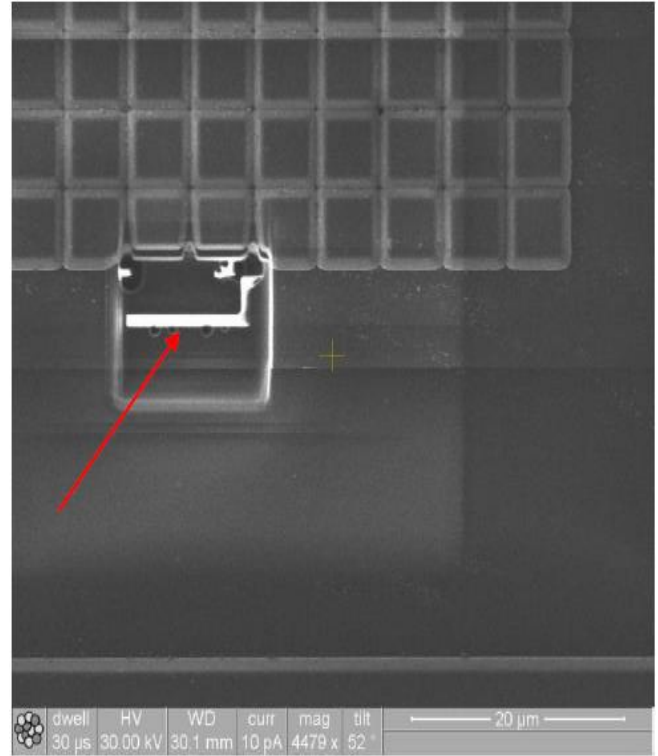


Figure 4: Metal 2 (Aluminium) Exposed After Ion Milling

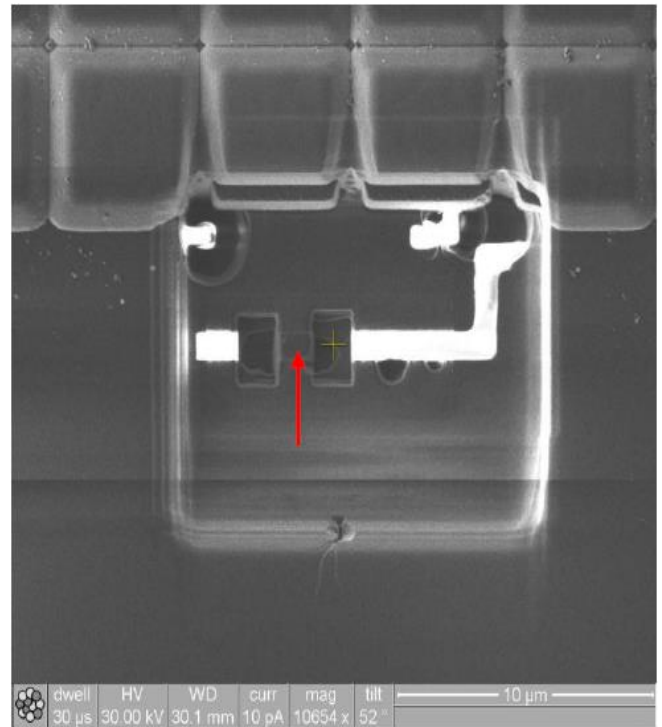


Figure 5: Floating Metal Appears Darker

In the next case, DRAM having specific memory bit failure is taken for study. Electrical testing has shown address of failing memory bit. In the failed location, FIB image shows darker contrast indicating floating memory cell. This is shown in Figure 6. This shows capability of PVC technique to detect structures smaller than 0.5 microns.

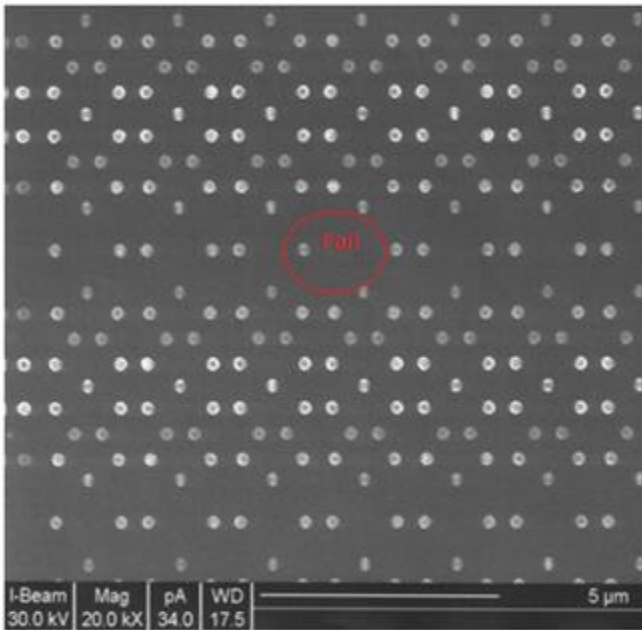


Figure 6: Floating Memory bit in DRAM

In another case, DRAM with failed Digit Line contact (DLCT) is studied. The floating DLCT is easily identified through PVC. Further deprocessing and analysis shows marginal / poor contact between memory cell and poly plug as shown in the Figure 7. Even at adjacent functional memory cells, the contact is seen to be marginal due to misalignment of cell with poly plug.

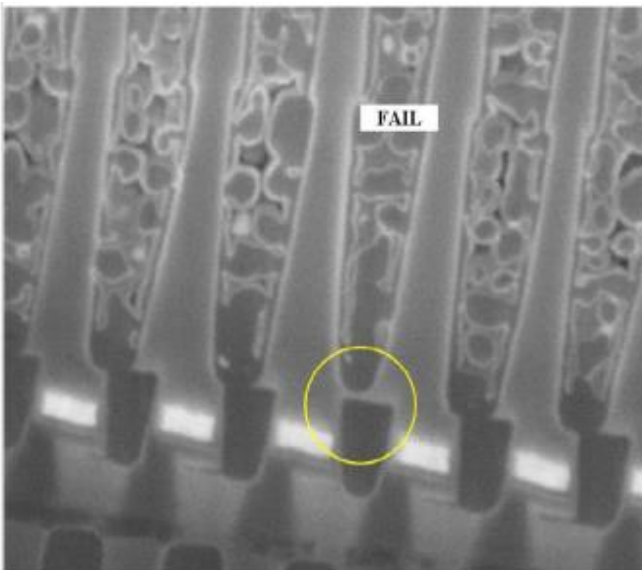


Figure 7: Poor / Marginal Contact Between Memory Cell and Poly Plug

III. CONCLUSION

PVC is found to be one of the effective techniques in identifying floating structures of micron / sub micron scale. Further analysis is required to confirm the root cause of the failure. It does not require any complicated sample preparation for testing. Also it does not use probes for biasing which would be difficult for precise positioning. Detailed electrical characterization and understanding of the device structure and layout is important to correlate the fault location with the electrical failure.

REFERENCES

1. Ruediger Rosenkrantz "Failure localization with active and passive voltage contrast in SEM and FIB" Journal of Material Science, Mater Electron, Vol:22, pp: 1523 – 1535, 2011
2. N. Nishikawa et al, " An application of passive voltage contrast (PVC) to failure analysis of CMOS LSI using secondary electron collection" ISTFA Proceeding, pp: 239 – 243 1999
3. C. Yuan et al, "Gray method of failure site isolation for flash memory devices using FIB passive voltage contrast techniques." ISTFA Proceedings, pp: 202 – 205, 2005
4. C.M. Shen et al, " Couple passive voltage contrast with scanning probe microscope to identify invisible implant issue" ISTFA Proceedings, pp: 212 – 216, 2005
5. O.D. Patterson et al, "Real time fault site isolation of front end defects in ULSI – ESRAM utilizing in – line passive voltage contrast analysis" ISTFA Proceedings, pp: 591 – 599, 2005