Low Power and High Performance ALU using Dual Mode Transmission Gate Diffusion Input (DMTGDI)

Allam Srivani, M. Lakshmi Prasanna Rani

Abstract: ***Using Dual Mode Transmission Gate Diffusion Input Logic (DMTGDI), a four bit ALU has been designed. The ALU can perform four arithmetic and four logical operations. Dual Mode Transmission Gate Diffusion Input (DMTGDI) logic has been promising in realizing increased functionality on a chip. The main advantage of this new logic called DMTGDI is low power and high performance. For low power applications there are so many conventional techniques are available. For reducing power consumption, sub-threshold circuit design is the one of the most important techniques. But the circuit in sub-threshold region operates with so many sensitivities and constraints. Mostly the performance of the circuit which is operated in sub-threshold region is degraded. To increase the performance of the circuit in sub-threshold region one of the most effective logic used is called as Dual Mode Logic (DML). So DML is the one of the techniques used for high speed. Another important technique is established for reducing power consumption is called Transmission Gate Diffusion Input (TGDI). In the next step, we propose to use Transmission Gate Diffusion Input (TGDI) as a foundation for new Dual Mode logic called "DMTGDI or Dual Mode Transmission Gate Diffusion Input" logic. So DMTGDI combines the advantages of both DML and TGDI. Simulations have been performed in mentor graphics tool using 130nm. Pre-layout simulation results reveal that ALU design using DMTGDI logic is more advantageous than ALU design using conventional CMOS logic.***

Index terms: ALU, TGDI, DML, DMTGDI, CMOS.

I. INTRODUCTION

An Arithmetic Logic Unit (ALU) [1] is a combinational circuit that performs logic and arithmetic operations on a pair of 'n' operands. If n is 4, then the inputs A represented as [3:0] and B represented as [3:0]. All the operations performed by an ALU are controlled by control signals. The design of ALU [2] follows a principle called 'Design and Conquer'. That means instead of designing a 4-bit ALU as one circuit we will first design a 1-bit ALU, which is called as "BIT-SLICE". These 'bit-slices' can then be put together to make a four-bit ALU. ALU is the main fundamental element of the CPU in a computer. In ALU [3] there are different fundamental blocks are available. Those are multiplexers and full adders. Full adder is the primary constituent of ALU circuit. The speed of the circuit depends on this full adder when compared to the other elements present in the circuit of ALU.

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To design a low power and high performance ALU, we have to choose a technique which can operate with low power consumption and high speed. We have different conventional techniques for low power operations. For reducing power consumption the circuit should operate in sub-threshold region [4]. If the circuit operates in sub-threshold region, the circuit may effect to so many constraints and sensitivities when compared to the circuit operate in above threshold region. To increase the performance of the circuit which is operated in sub-threshold region DML [5] technique is used. DML is abbreviated as Dual Mode Logic. The structure of the DML is made up of using conventional CMOS logic with an extra mode select transistor which can be a pull-up or pull-down transistor. The input of the mode select transistor is 'clk' signal. If the clk signal is high the circuit operates in static mode. And if the clk signal is low the circuit operates in dynamic mode, when the mode select transistor is pull-up transistor vise-versa. In dynamic mode the circuit performs two phases. One is pre-charge and another one is evaluation. In pre-charge phase the whole circuit pre-charged to V_{dd} for pull-up transistor and to ground for pull-down transistor independent of the input sequence. In evaluation phase the actual operation of the circuit is performed. For high speed operations we are using DML [6] technique. Another technique for low power applications is TGDI. TGDI abbreviated as Transmission Gate Diffusion Input. This logic is advanced version of GDI. GDI is abbreviated as Gate Diffusion Input. By using this logic we can implement more number of complex functions by using very less number of transistors when compared to the conventional CMOS technique. But in this technique the output swing is decreased for some input combinations. To overcome this disadvantage we have to add buffers at output of the circuit. It may leads to complexity. Another technique called TGDI is used. In this technique it decreases the output swing reduction for some input combinations in GDI logic, without adding buffers at the output stage. And it requires less power consumption than the conventional CMOS logic. In the next step we plan for inventing a new technique by taking TGDI as a basic element for new "dual mode logic" called 'DM TGDI' [7]. This can be abbreviated as "Dual Mode Transmission Gate Diffusion Input". In this logic it combines the advantages of both DML (high speed) and TGDI (low power consumption). Full adder is the main block in ALU. For getting low power and high performance this full adder block is implemented in both conventional CMOS and DMTGDI techniques,

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To compare different metrics like power, delay, power delay product, and no. of. Transistors using pre-layout [8] simulations.

II. THE DESIGN OF ALU

A four bit ALU has been implemented for less power consumption in which, the full adder alone is implemented by using both conventional CMOS and DMTGDI logic.

The full adder [9] is implemented in both logics by using two EXOR gates, two AND gates and one OR gate. It has two outputs: One is SUM bit another one is CARRY bit. The ALU has four stages, each stage consisting of input multiplexers, output multiplexers and full adder. Here 2X1 multiplexers and 4X1 multiplexers are used at input and output of the circuit. The ALU performs the following 4 arithmetic operations those are Increment, Decrement, Addition, and Subtraction. The 4 logical operations performed are Or, And, Exor, and Exnor. Here multiplexers are implemented by using conventional CMOS logic. A set of 3 select signals (s0, s1, s2) has been incorporated in the design to determine the operation being performed and the inputs and outputs being selected. Fig.1 shows the 4-bit ALU block diagram with the CARRY bit cascading all the way from first stage to fourth stage. In the below figure we have eight 4X1 multiplexers, eight 2X1 multiplexers and four full adders. Multiplexers are implemented by using CMOS technology. The full adder [10] alone implemented by using CMOS technology and DMTGDI technology. Table 1 shows the truth table of 4-bit ALU. Below fig 2 shows the 4X1 multiplexer block diagram. Table 2 shows the truth table of 4X1 multiplexer. Fig 3 shows the 2X1 multiplexer block diagram. Table 3 shows the truth table of 2X1 multiplexer.

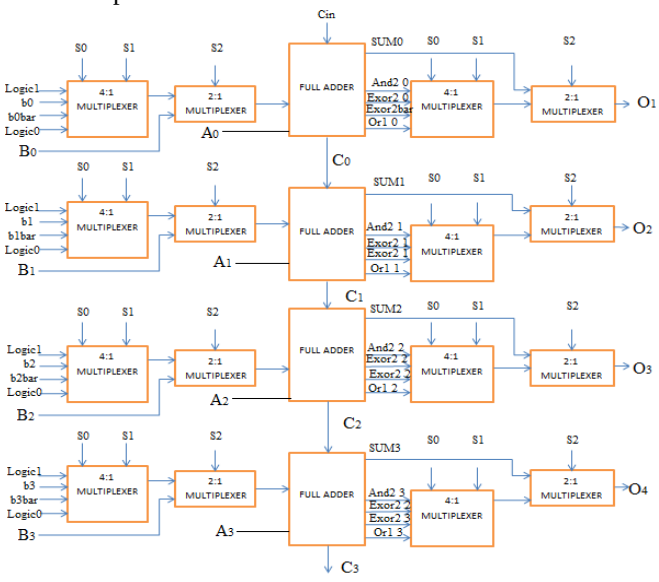

Fig 1: Block Diagram of 4-bit ALU

Table 1: Truth table of 4-bit ALU

S.NO	S2	S1	S0	OPERATION
1	0	0	0	INCREMENT
2	0	0	1	DECREMENT
3	0	1	0	ADDITION
4	0	1	1	SUBTRACTION
5	1	0	0	AND
6	1	0	1	OR
7	1	1	0	EXOR
8	1	1	1	EXNOR

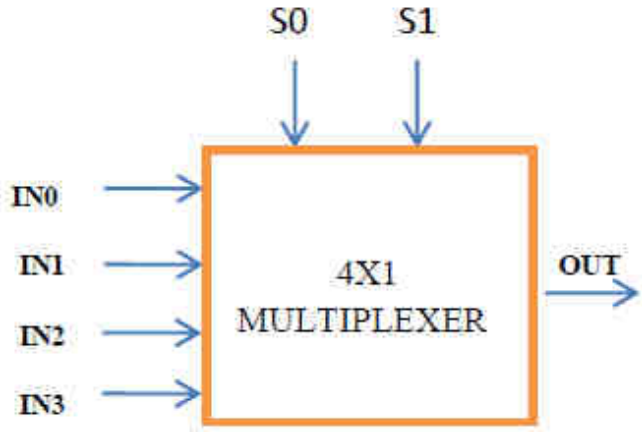

Fig 2: Block diagram of 4X1 multiplexer

Table 2: Truth table of 4X1 multiplexer

S.NO.	SELECT SIGNAL	SELECT SIGNAL	SELECTED
	S0	S1	INPUT
1	0	0	IN0
2	0	1	IN1
3	1	0	IN2
4	1	1	IN3

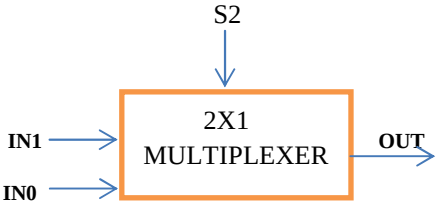

Fig 3: Block diagram of 2X1 multiplexer

Table 3: Truth table of 2X1 multiplexer

S. No	Select Signal S2	Operation Performed
1	0	ARITHMETIC
2	1	LOGICAL

III. ALU USING CMOS TECHNOLOGY

A four bit ALU has been designed by using conventional CMOS technology. In an ALU there are different multiplexers and full adders are present. All these are implemented by using CMOS gates. Below fig 4 shows the schematic diagram of 4X1 multiplexer. Fig 5 shows the pre-layout simulation results of the 4X1 multiplexer. The 4X1 multiplexer is implemented by using three 2X1 multiplexers.

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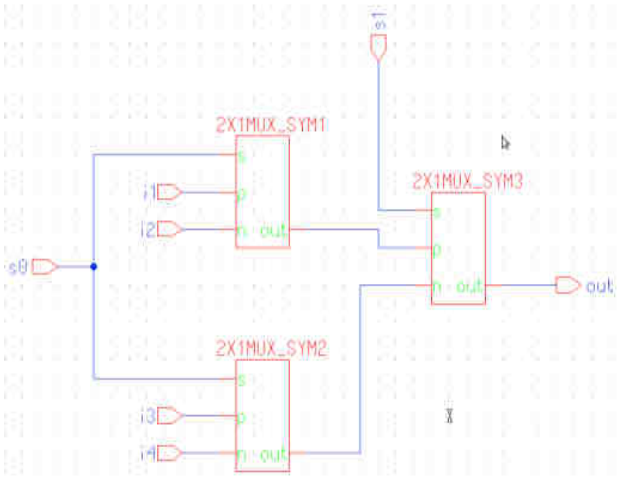

Fig 4: Schematic diagram of 4X1 multiplexer

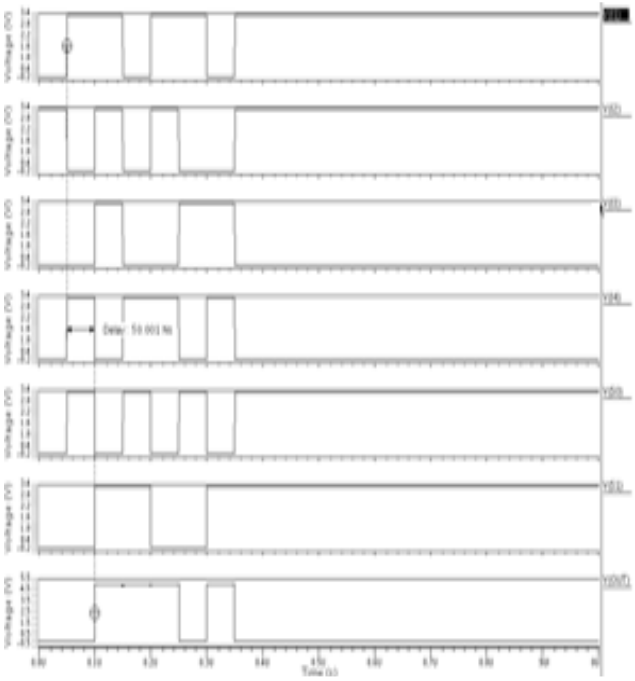

Fig 5: Pre layout simulation results of 4x1 multiplexer

The 2X1 multiplexer is implemented by using different CMOS gates like and gates, inverter and or gate. The schematic diagram of 2X1 multiplexer is shown in below fig 6. Fig 7 shows the pre-layout simulation results of 2X1 multiplexer.

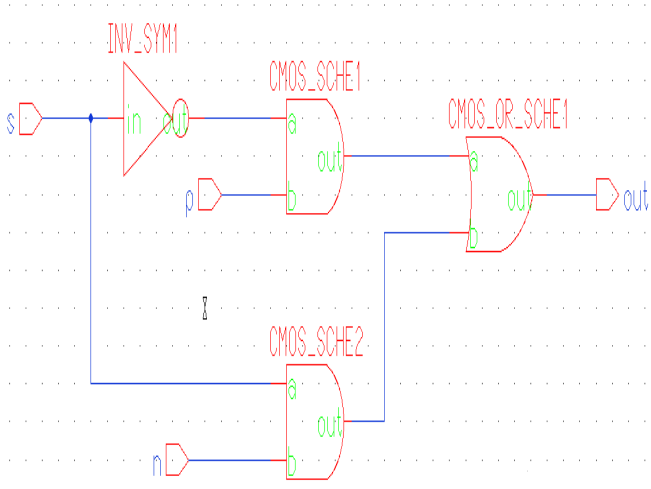

Fig 6: Schematic diagram of 2X1 multiplexer

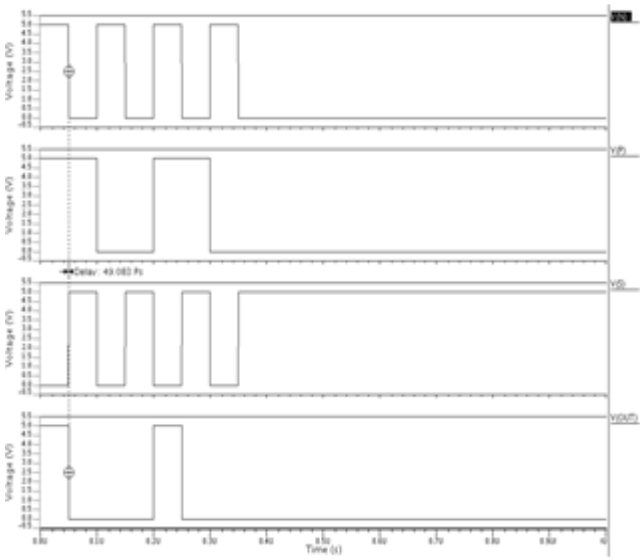

Fig 7: Pre layout simulation results of 2x1 multiplexer

In ALU another important block is full adder. This Full adder also implemented by using different conventional CMOS gates. Here it uses 2 EXOR gates, 2 AND gates and 1 OR gate. Below fig 8 shows the schematic diagram of full adder. Fig 9 shows the pre-layout simulations of full adder. Table 4 shows the truth table of full adder.

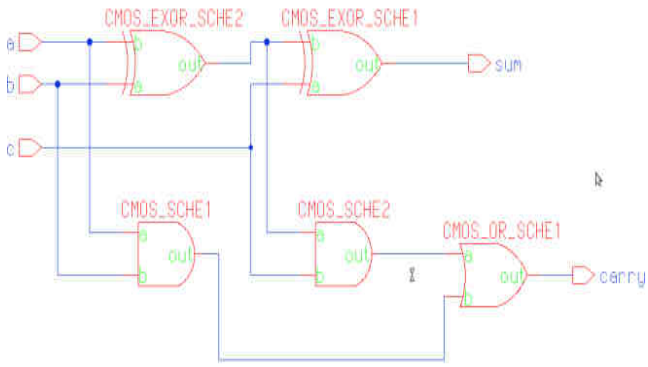

Fig 8: Schematic diagram of full adder

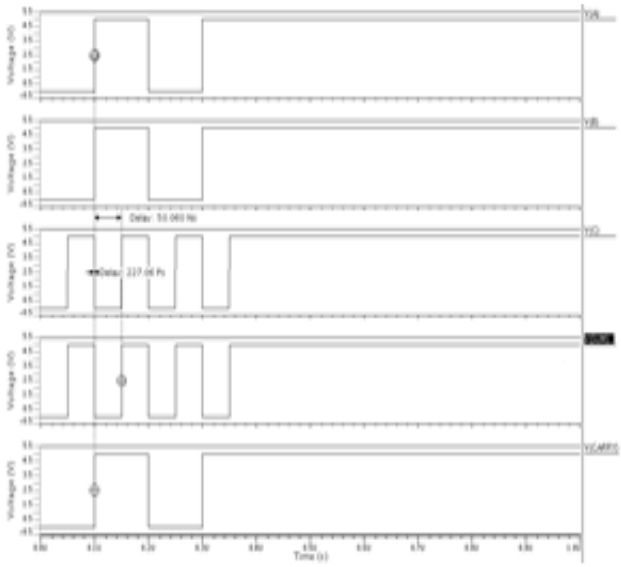

Fig 9: Pre layout simulation results of full adder

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Table 4: Truth table of full adder

S. NO.	A	B	C	SUM	CARRY
1	0	0	0	0	0
2	0	0	1	1	0
3	0	1	0	1	0
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	0	1
7	1	1	0	0	1
8	1	1	1	1	1

By using these three elements a 4-bit ALU is implemented. Below fig 10 shows the schematic diagram of four bit ALU. Fig 11 shows the pre-layout simulation results of four bit ALU.

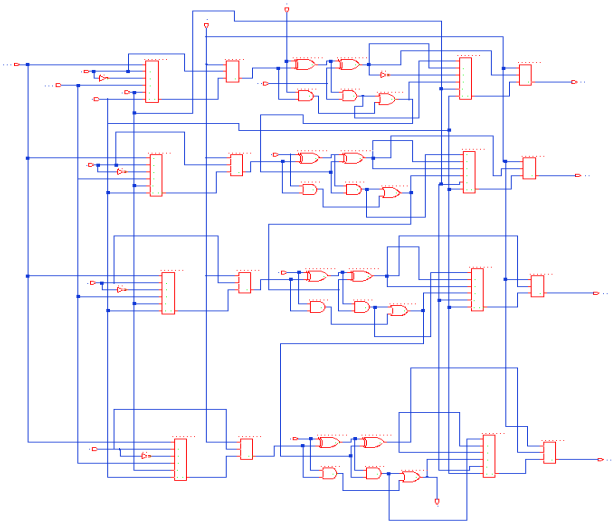

Fig 10: Schematic diagram of 4-bit ALU

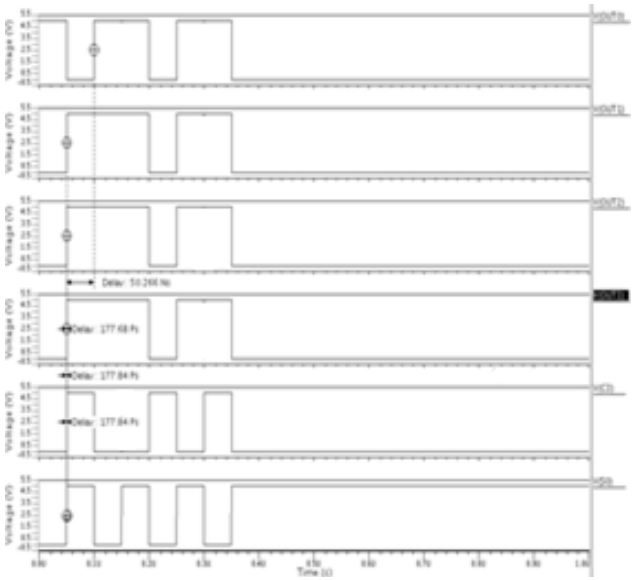

Fig 11: Pre layout simulation results of 4-bit ALU using CMOS technique

IV. ALU USING DMTGDI TECHNOLOGY

In a four bit ALU, full adder is the heart of the circuit. In CMOS technology static power dissipation is less, but For low power consumption and high speed we go for another new technique called DMTGDI. The full adder alone is implemented by using this technique. And all the multiplexers present in the ALU is implemented by using CMOS technology. The schematic diagram for full adder using DMTGDI logic is shown in below fig 12. Pre-layout simulation results of full adder using DMTGDI logic is shown in below fig 13.

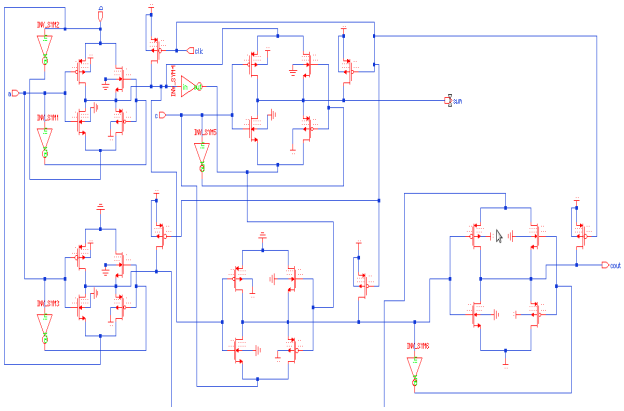

Fig 12: Full adder schematic using DMTGDI logic

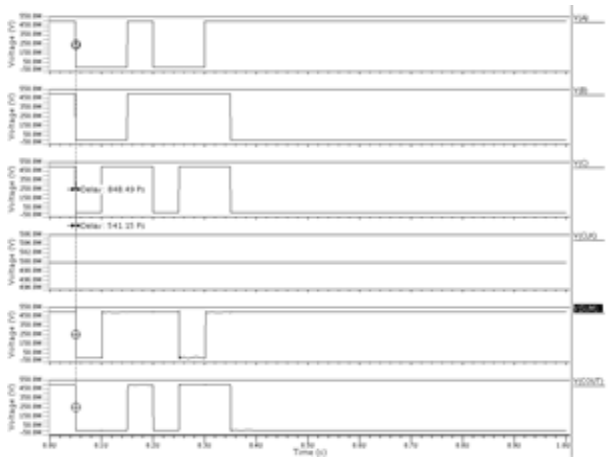

Fig 13 (a): Pre layout simulation results of the full adder circuit using DMTGDI logic in static mode

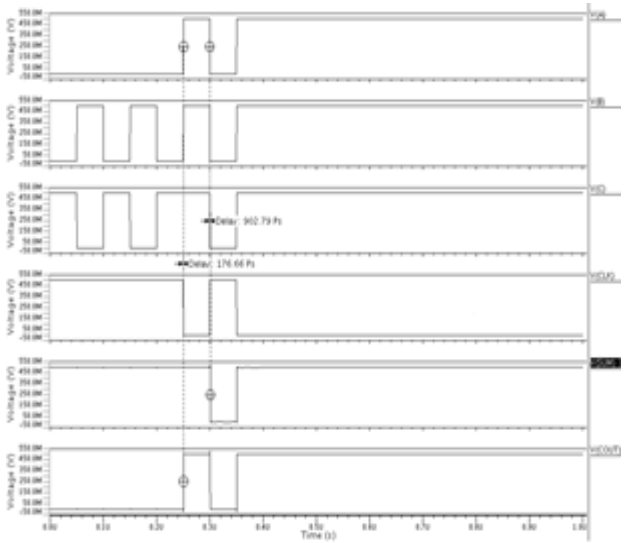

Fig 13 (b): Pre layout simulation results of the full adder circuit Using DMTGDI logic in dynamic mode.

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For the full adder circuit using DMTGDI logic, we can draw the layout using mentor graphics tool in 130nm technology. The layout of the full adder using DMTGDI logic is also shown in below fig 14.

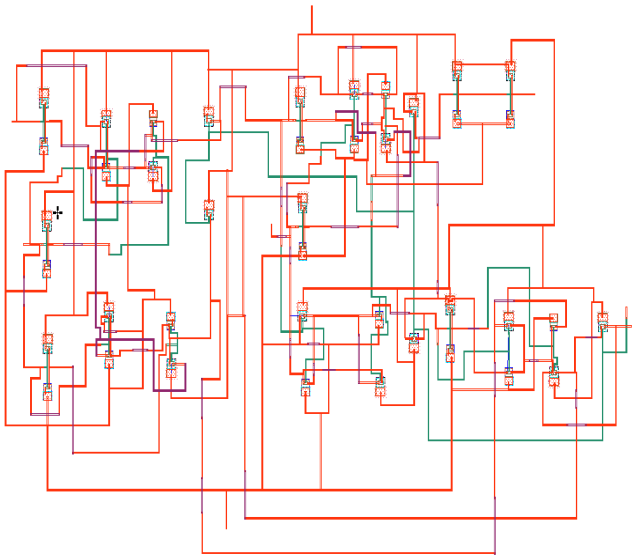

Fig 14. Layout of the full adder using DMTGDI logic

By using this full adder we can implement low power and high performance 4-bit ALU. The schematic diagram of four bit ALU using DMTGDI full adder is shown in below fig 15.Pre-layout simulation results of ALU is also as shown in below fig 16.

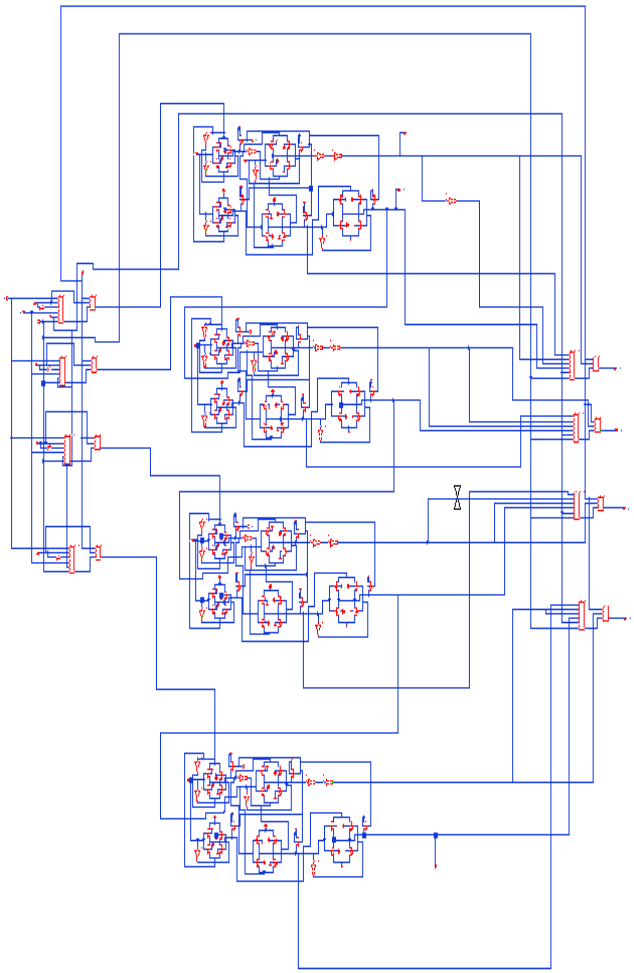

Fig 15: Schematic diagram of ALU using DMTGDI full adder

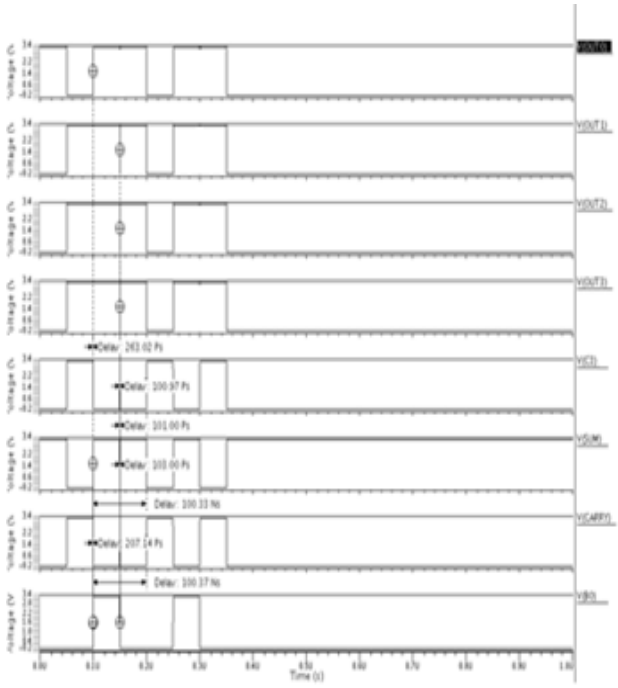

Fig 16 (a): Pre layout simulation results of ALU in static mode

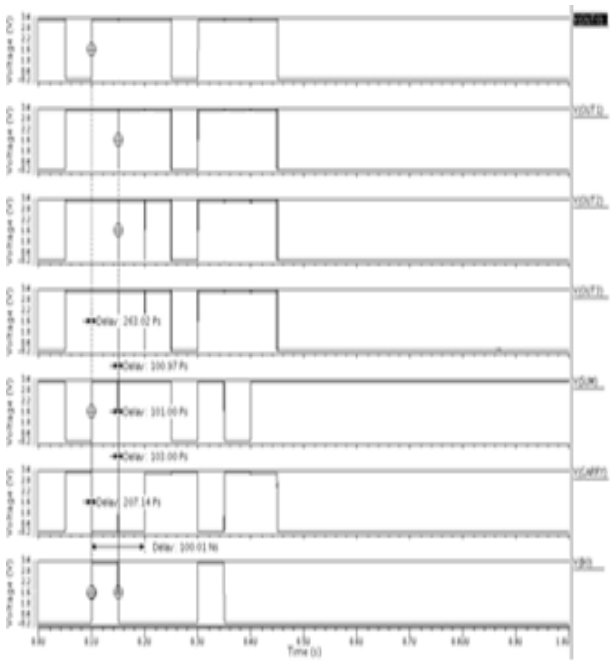

Fig 16(b): Pre layout simulation results of ALU in dynamic mode

The simulation results of both CMOS based ALU and DMTGDI based ALU is compared in presence of different parameters like no. of transistors, power, delay, and power delay product**.** Below table 5 shows the comparison table. This gives the information of pre-layout simulation results of both the technologies. In the below comparison table it shows that the new technique Dual Mode Transmission Gate Diffusion Input having better performance, less power consumption, less power delay product (PDP) and less complexity than the conventional CMOS technique.

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Table 5: Comparison table of ALU using both CMOS and DMTGDI logics

S. No.	Logics	Function	Power (n W)	Delay (n S)	PDP (a J)	#Tr
1	CMOS	ALU	11022.7	177.68	19.5851	840
2	DMTGDI (static)	ALU	2617	100.33	2.6256	804
3	DMTGDI (dynamic)	ALU	2617	100.97	2.6423	804

V. SIMULATION RESULTS AND DISCUSSION

A four bit ALU has been implemented by using both CMOS and DMTGDI techniques. These circuits are used for simulation and comparing the simulation results in the presence of different metrics. In CMOS technology static power dissipation is the drawback. To overcome to this problem and increase the speed of the circuit we used another technique called DMTGDI technique. In an ALU there are different block are available. Those are input multiplexers, output multiplexers and full adder. The total speed or performance in the ALU circuit depends on full adder. So here we use CMOS technology for all the 2x1 and 4x1 multiplexers. The full adder also implemented by using CMOS technology. To increase the circuit operation the full adder alone also implemented using DMTGDI technique. In this full adder there are different gates are used. Those are two EXOR gates, two AND gates and one OR gate. Same gates are used in DMTGDI technology also. Which are operated by input clock signal. And here 2x1, 4x1 multiplexers are operated by using selected signals s0, s1, and s2. 2x1 is implemented by using inverter, and gate, and or gate. 4x1 is implemented by using three 2x1 multiplexers. When compare the pre layout simulation results of both CMOS based ALU and DMTGDI based ALU shows that the proposed technique is more advantageous than the conventional CMOS logic.

VI. CONCLUSION

In this paper new logic called Dual Mode Transmission Gate Diffusion Input (DMTGDI) has been introduced. This logic is introduced based on two consecutive steps. First step is by replacing pass transistors on Gate Diffusion Input logic (GDI) with transmission gates in Transmission Gate Diffusion Input (TGDI) to decrease the output swing reduction. And then this TGDI is added to the DML logic. By using this logic a four bit ALU has been implemented and simulated in 130nm mentor graphics tool. And these simulation results are compared with conventional CMOS technique. This comparison results states that the proposed technique is advantageous in performance, speed, and in complexity than the conventional CMOS technique. The proposed logic can operate in sub-threshold region so it requires less voltage for the circuit operation. To further increase the performance and power characteristics of this proposed logic family, we can change widths of the transistors or we can use dynamic voltage scaling.

REFERENCES

1. Chandra Srinivasan, A Thesis “arithmetic logic unit (alu)” design using reconfigurable CMOS logic” Bachelor of Engineering, Mysore University, 1997.
2. A. Srivastava and D. Govindarajan, “A fast ALU design in CMOS for low voltage operation”, J. of VLSI Design, vol. 14, no. 4, pp. 315-327, 2002.
3. A. Srivastava and C. Srinivasan, “ ALU Design using Reconfigurable CMOS Logic”, Proc. of the 45th IEEE 2002 Midwest Symposium on Circuits and Systems , vol.2, pp. 663- 666, Aug. 2002.
4. S. Kumar Gupta, A. Ray chowdhury, K. Roy, Digital computation in subthreshold region for ultra-low power operation: a device circuit architecture co-design perspective, Proc. IEEE 98 (2) (2010) 160–190.
5. I. Levi, A. Kaizer man, A.Fish, Low voltage dual mode logic: model analysis and parameter extraction, Micro electron. J. 44(2013)553–560.
6. A. Kaizerman, S. Fisher, A. Fish, Subthreshold dual mode logic, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 21 (5) (2013) 979–983.
7. Elahe Rastegar Pashaki, M.Shalchian Electrical Engineering Department, Amirkabir University of Technology, 424 Hafez Ave., Tehran, Iran “Design and simulation of an ultra-low power high performance CMOS logic: DMTGDI” Integration, the VLSI journal 55(2016)194–201.
8. R. J. Baker, H.W. Li and D.E. Boyce, CMOS Circuit Design, Layout and Simulation, IEEE Press, 1998.
9. D. Radhakrishnan, “Low - voltage low - power CMOS full adder” , IEE Proceedings -Circuits, Devices and Systems, vol.148, pp. 19 - 24, Feb. 2001
10. A.M. Shams and M.A. Bayoumi, “A novel high- performance CMOS 1 - bit full- adder cell”, IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, pp. 478 –481, May 2000.

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