Design of Decoders using Mixed Logic for Various Applications

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Abstract: In this paper, a mixed-logic design of decoders, combining modified GDI logic, transmission gate logic, and pass transistor logic has been proposed. A novel topology is presented for the 2-4 decoders: a 15- transistor topology on the intension of achieving low power and low delay. Further, three decoders 3-8, 4-16 and 5-32 are implemented by using mixed-logic 2-4 decoders. MGDI technique uses same number of transistors present in CMOS the main difference is the providing input signals to the source and gate terminals. These all proposed decoders reduce the power and delay compared to conventional CMOS decoders. The proposed 2x4 decoder is implemented to decrease power; increase the performance is used in full adder and 4×4 bit SRAM array. Finally simulations are done by using CMOS 130nm mentor graphics tool to give a significant improvement in power and delay.

Index terms - Decoders; sense amplifier; SRAM cell; high speed; mixed logic; MGDI logic.

I. INTRODUCTION

The advancements in VLSI technology allow us to fabricate billions of transistors in one single chip. So, there is demand for low power VLSI technology. The VLSI technologies have different design levels, such as the architectural, circuit, layout, and the process technology level. The circuit level design has considerable power savings by means of selection of good logic style for implementing combinational circuits. The parameters governing power dissipation are switching capacitance, transition activity, and short-circuit currents. In most of the VLSI applications, such as digital signal processing, image and video processing, and microprocessors, extensively use arithmetic operations. The commonly used operations are Addition, subtraction, multiplication, and multiply and accumulate (MAC) [1]. With the fast advanced nature of technology, the speed of the device does matter. Memories used in computer system and digital circuit like registers and cache memories SRAM modules are frequently used memories. For every clock cycle the memories are accessed. Row and column decoders are the most important elements used in RAM. The decoder performance largely depends on the time taken to access data and power consumption in memories [3].

II. EXISTING TECHNIQUE

Implementing a 2–4 line decoder using by TGL or DVL gates consisting of total of 16 transistors (12 for AND/OR gates and 4 for inverters).

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So, by using proper signal arrangement it combines two TGL AND, OR gates, DVL AND, OR gates into one topology and forms a 14T topology. However, the usage of TGL, DVL gate would eliminate the one of the inverter from the 16T topology. So by reducing one of the inverter, the number of transistors is reduced and power dissipation also less. A, B, are the inputs. In order to eliminate the second inverter B from the circuit, DVL logic used in the implementation of D0 min-term by using A as propagation signal, and B is used as a propagate signal while implementing D1 min-term using TGL. DVL gate is used to get the min-term D2. Here the propagating signal is A. Finally, TGL gate is used to generate min-term D3 B is the propagation signal. The complementary B signal is completely removed by using this particular choices therefore: A 14 transistor topology can be obtained from the reduction of B inverter from the circuit resulting in a 14-transistor topology reducing power [1] as shown in figure 1.

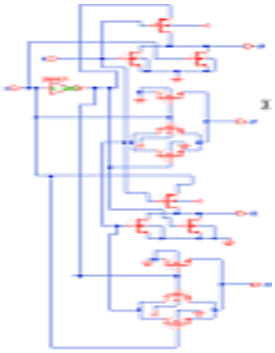

Figure 1 2:4 decoder

III. PROPOSED TECHNIQUE

In integrated circuits majority of logic gates are implemented using Static CMOS circuits. It consists of pull up and pull down network in which PMOS used in pull up network, where as NMOS is used in pull down network and present good resistance to noise, better performance and can with stand for device variations CMOS circuits have less static power dissipation. It has less scalable threshold voltage [1]. DVL (dual value logic) gate was obtained by eliminating the redundant branches and rearrangement of signals in DPL (double pass transistor logic). Signal rearrangement results in NAND gate configuration which is faster than DPL; where the AND half is faster [7]. When the pass transistor logic is compared with the CMOS logic the main difference observed is that the source side of the logic transistor networks is connected to some input signals instead of the VDD. The advantage is that one pass-transistor network (either NMOS or PMOS) requires only one transistor and it is sufficient to perform the logic operation,

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which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used [8]. The inputs in CMOS technology are used to make the MOSFET switch ON or OFF. Here the biasing voltage is passed to output depending on input. In MGDI, GDI is the basic circuit in which output is connected to the inverter and also the inputs are diffused through the switch and to the output. By using this technique power and delay will get reduced. The basic primitive of GDI cell consists of NMOS and PMOS transistors connected in parallel combination in which the input signals are applied to the source, gate terminals of transistors and output taken across the drains terminals MGDI NOR contains of four transistors in which two transistors are connected in parallel and an inverter is used at the output side to get the efficient design as shown in figure 2 and MGDI NAND gate also contains of same number of transistors present in CMOS but difference is transistor arrangement and applying input signals to the source and drain terminals of the transistors as shown in figure 3.

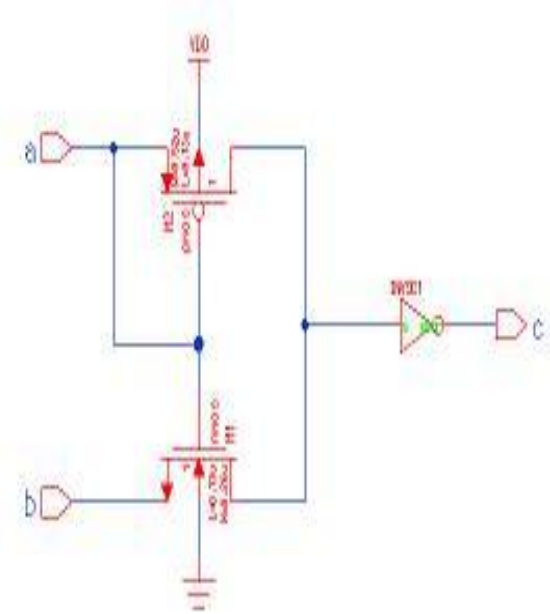

Figure 2: MGDI NOR gate

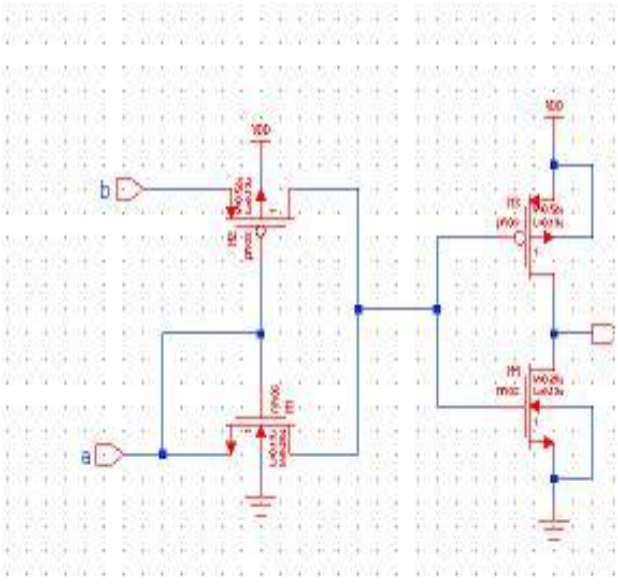

Figure 3: MGDI NAND gate

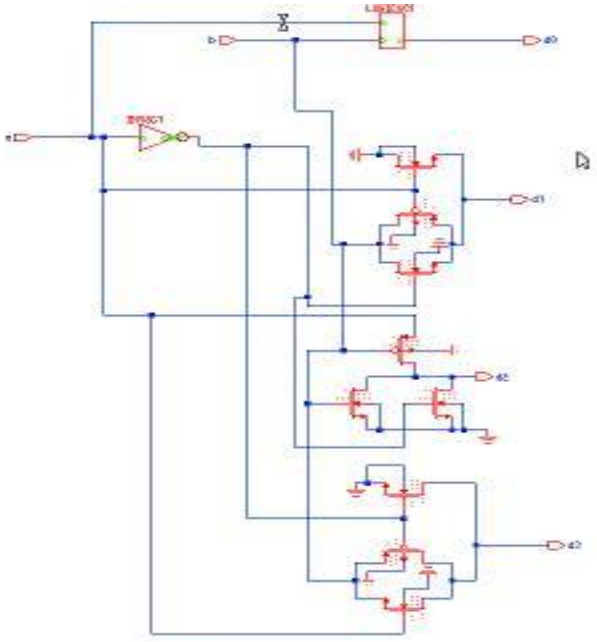

Figure 4: Modified 2 to 4 decoder

The worst case delay is the main disadvantage presented in low-power 14T topologies presented in [1] this disadvantage mainly caused by propagating signal A bar in the case of D0 and I3 min-terms. However, by using static CMOS logic D0 and I3 min-terms can be efficiently obtained without using complementary signals. Where as in proposed circuit MGDI NOR logic and MGDI NAND logic is used to generate the min-terms D0 and I3. Addition of one transistor to each topology forms 15T topology. The new 15T transistor designs is used decrease the delay and power dissipation as shown in figure 4 and its simulation waveforms are shown in figure 5.

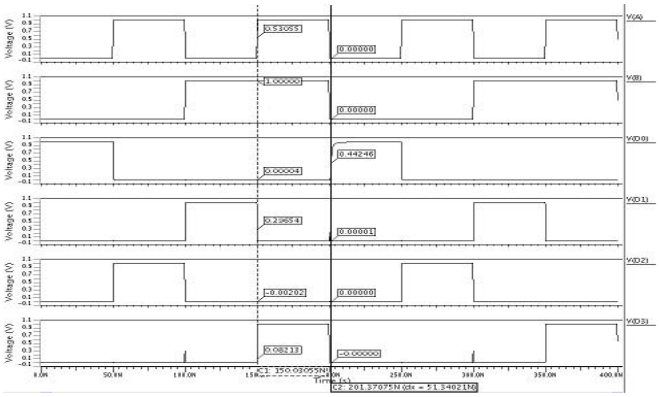

Figure 5: Output waveforms of 2 to 4 Decoder

IV. APPLICATIONS

A. Full Adder

Full adder is a fundamental block in digital systems. Here the full adder can be implemented by using two 2×4 decoders and three MGDI OR gates as shown in figure 6. MGDI full adder cell have less delay and low power as compared to the CMOS full adder and its output waveforms are as shown in figure 7. Figure 8 represents the layout of full adder circuit and figure 9 represents the corresponding post layout simulation result after the adding the effect of parasitic elements.

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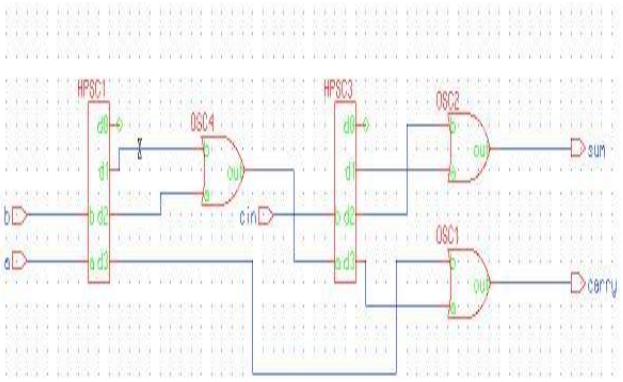

Figure 6: Full adder schematic

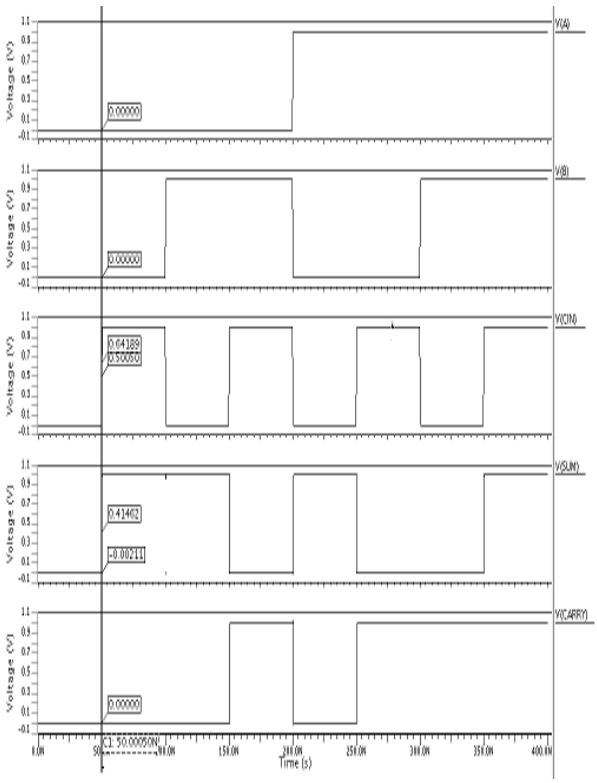

Figure 7: Output waveforms of fulladder.

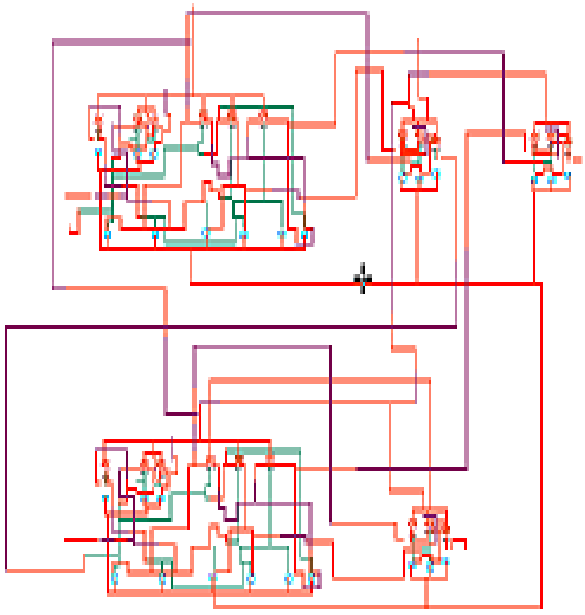

Figure 8: Full adder layout

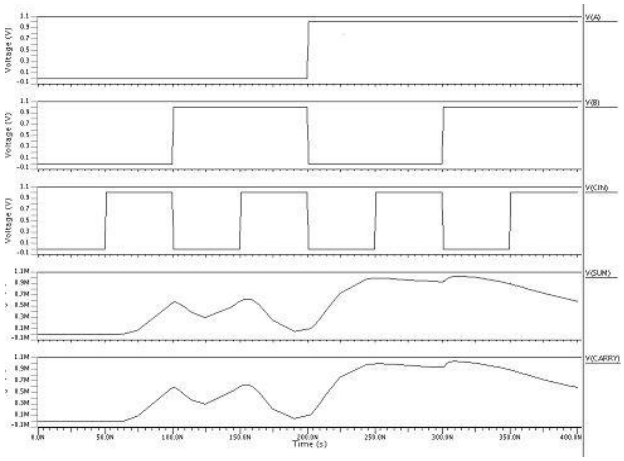

Figure 9: Post layout simulation of full

B. 4×4 BIT SRAM ARRAY

In a 4×4 bit SRAM array it requires a 2 to 4 decoder and 16 SRAM cells to perform write and read operation with better performance. A decoder implemented with mixed logic decreases the delay of the circuit compared to the conventional CMOS. A 2 to 4 decoder implemented using mixed logic is used in 4×4 bit SRAM array will provide better performance compared to the CMOS logic. Based on the input combination any one of the word line get selected and becomes high, then the data present in the bit line is written in to the SRAM cell. A 1 bit 6T SRAM cell is used as the main internal block in the memory array as shown in fig 10. Sense amplifier is the part of the read circuitry and this sense amplifier is used to read the data from the cell. For the input combination 00, first word line is selected and data written in the cell and it directly reads from the sense amplifier as represented in figure 11 and simulation wave forms are represented in figure 12.

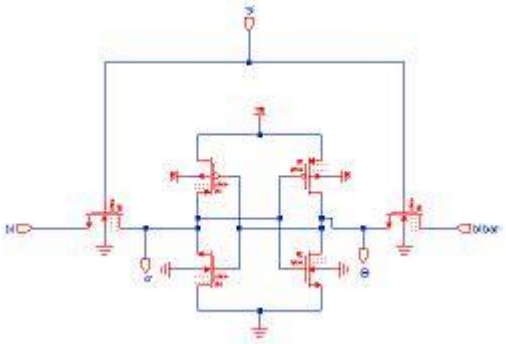

Figure 10: 6TSRAM cell

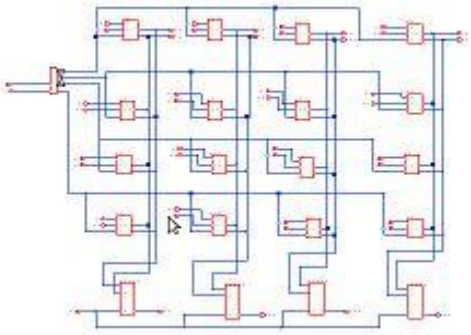

Figure 11: 4×4 bit SRAM array.

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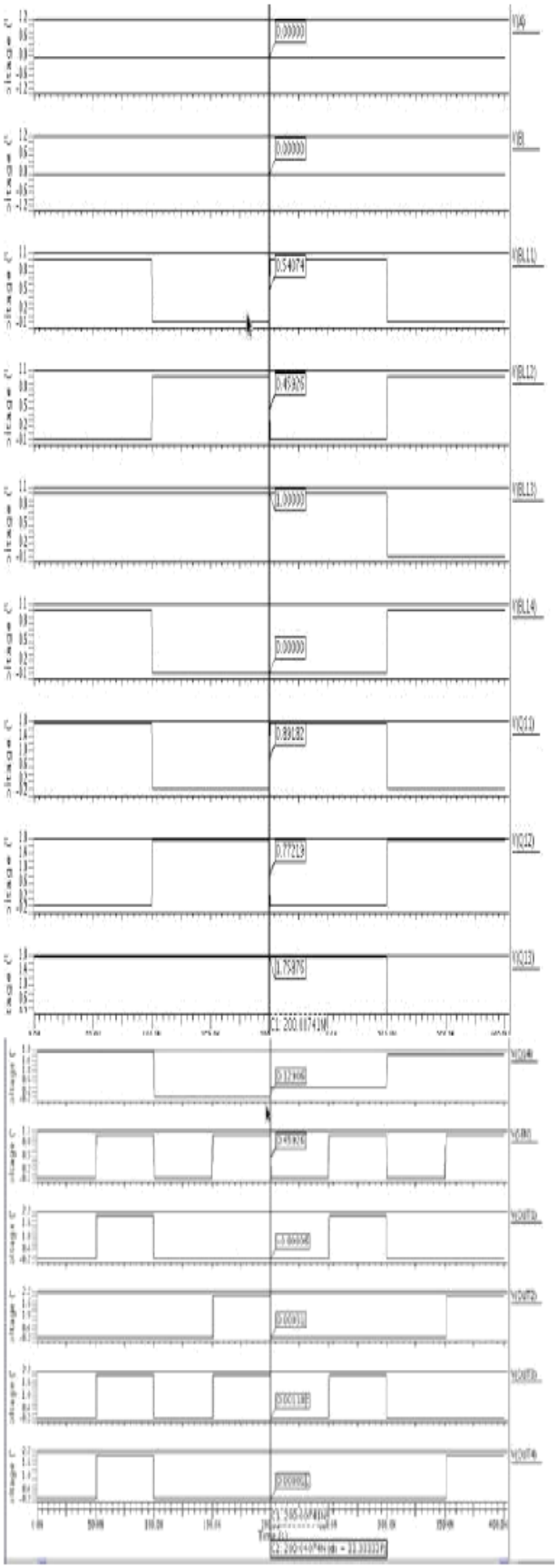

Figure 12: Simulation wave forms of 4×4 bit SRAM array

V. SIMULATION RESULTS

All the circuits are implemented using CMOS 130 nm technology and simulations are performed by mentor graphics tool. The below table states that the MGDI logic gives better performances and reduces power dissipation than the conventional CMOS technology.

Table 1.1 Comparison of CMOS circuits and mixed logic

S .No	SIZE OF DECODER	CMOS LOGIC			MIXED LOGC		
		POWER DISSIPATION	DELAY (sec)	NO.OF TRANSISTORS	POWER DISSIPATION (watts)	DELAY (sec)	NO. OF TRANSISTORS
1	2-4 DECODER	4.84 nw	132.3 ns	20	2.348 nw	52.3 ns	15
2	2-4 INVERTING DECODER	18.7 nw	99.7ns	20	4.828 nw	51.0 ns	15
3	4-16 DECODER	56.1 nw	50.8 ns	104	12.6 nw	142.8 ps	96
4	5-32 DECODER	1.80 uw	178.6 ps	679	18.8 nw	173.2 ps	679
5	4 BIT×4 BIT SRAM ARRAY	329.0 uw	357.1 ps	147	33.78 nw	33.3 ps	147
6	FULL ADDER	13.97nw	50.29 ns	48	11.93 nw	650.1 ps	36

VI. CONCLUSION

In this paper, the combination of MGDI, TGL, and static CMOS gives an efficient mixed logic design which is used for decoding circuits. By using above two techniques we have a new topology namely as 2–4 low power decoder and a 2–4 low power inverting decoders. By using above two techniques which reduces the number of transistors, decreases delay, power and increases the performance of the circuit than compared to the conventional CMOS decoders. By using mixed logic 2:4decoders as pre decoding circuits in conjunction with CMOS logic. Three new topologies were presented, namely 4–16 low power decoder, 4–16 low power inverting decoder, 5-32 bit decoder. These all technologies provides good driving capability. The efficient low power decoders are designed and implemented in mentor graphics tool by using 130- nm technology. The decoders are implemented in mixed logic reduces the power consumption by 50 % and delay 60% when compared to conventional CMOS decoder.

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