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Design of High Speed 5:2 Compressor for Fast Arithmetic Circuits

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Abstract: Multipliers are important components that dictate the overall arithmetic circuits' performance. The most critical components of multipliers are compressors. In this paper, a new 5:2 compressor architecture based on changing some internal equations is proposed. In addition, using an efficient full-adder (FA) block is considered to have a high-speed compressor. The proposed architecture is compared with the best existing designs presented in the state-of the-art literature in terms of power, delay and area.

Keywords: Full-Adder (FA), XOR-XNOR, Multiplexers.

I. INTRODUCTION

Multipliers are one of the most significant blocks in computer arithmetic and are generally used in different digital signal processors. There is growing demands for high speed multipliers in different applications of computing systems, such as computer graphics, scientific calculation and image processing and so on. Speed of multiplier determines how fast the processors will run and designers are now more focused on high speed with low power consumption. The multiplier architecture consists of a partial product generation stage, partial product reduction stage and the final addition stage. The partial product reduction stage is responsible for a significant portion of the total multiplication delay, power and area. Therefore in order to accumulate partial products, compressors usually implement this stage because they contribute to the reduction of the partial products and also contribute to reduce the critical path which is important to maintain the circuit's performance. Most computerized mathematic applications are executed utilizing digital logic circuits, in this manner working with a high degree of reliability and precision. In any case, numerous applications, for example, in multimedia and image processing can endure mistakes and imprecision in calculation and still produce important and helpful results. Exact and precise models and algorithm are not generally suitable or productive for use in these applications. The paradigm of inaccurate calculation depends on relaxing completely precise and totally deterministic building modules when for instance, planning energy efficient system. This permits uncertain calculation to divert the current design procedure of computerized circuits and systems by exploiting a reduction in multifaceted nature and expense with conceivably a potential increment in execution and force productivity.

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In exact (or vague) figuring depends on utilizing this property to design disentangled, yet inexact circuits working at higher execution and/or lower power utilization contrasted and exact (definite) logic circuits. Expansion and multiplication are broadly utilized operations as a part of computerized mathematic; for expansion adders and proposed a few new measurements for assessing rough and probabilistic adders as for brought together figures of legitimacy for outline appraisal for estimated processing applications. For every data to a circuit, the Error Distance(ED) is characterized as the mathematic separation between a mistaken yield and the right one. The Mean Error Distance (MED) and normalized error distance (NED) are proposed by considering the averaging impact of various inputs and the standardization of multiple-bit adders. The NED is almost invariant with the measure of an execution and is accordingly valuable in the unwavering quality evaluation of a particular configuration. The tradeoff in the middle of accuracy and force has additionally been quantitatively assessed in.

II. COMPRESSOR ARCHITECTURES

Compressors are building blocks used for accumulating partial products during the multiplication process. The basic idea in an n : 2 compressor is that n operands can be reduced to two, by doing the addition while keeping the carries and sums separate. This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two-output adder with a time delay that is independent of the size of its inputs. The full adder is the most primitive compressor and is often referred to as the 3 : 2 compressor since it compresses three operands into two. The sum and carry outputs are given by the following set of equations:

$$\text{Sum} = x_1 \oplus x_2 \oplus c_i$$
$$\text{Carry} = x_1x_2 + x_2c_i + x_1c_i$$

Where x1 and x2 are the input operands and ci is the carry from previous stage. This 3:2 compressor has a delay of two XOR gates, and is normally used in carry-save form to sum up the partial products in a multiplier tree. Though the addition used in this manner is much faster than that of a ripple carry adder, the interconnections are very irregular thereby making the structure more complex. The 4:2 compressor was initially designed by an intricate connection of two 3:2 compressors as shown in Fig 1. The structure has a delay of four XORs. The advantage of the structure lies in its carry free nature, whereby the carry from the previous stage is not propagated to the next stage.

A novel design of a 4:2 compressor with XORs and multiplexers (MUX) as building blocks is presented in [5].

This design is based on a modified set of equations for the sum and carry outputs as:

$$\text{Sum} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus c_i$$

$$\text{Carry} = (x_1 \oplus x_2 \oplus x_3 \oplus x_4)c_i + (\overline{x_1 \oplus x_2 \oplus x_3 \oplus x_4})x_4,$$

$$C_o = (x_1 \oplus x_2)x_3 + (\overline{x_1 \oplus x_2})x_1$$

A widely used compressor of significant importance is the 5:2 compressor. Its block diagram is shown in Fig. 2. It has seven inputs of which five are direct inputs and two are carry-in bits from a previous stage. Similarly, there are four outputs of which two are carry-out bits to the next stage and the other two are sum and carry bits. All the 5:2 compressors of different designs abide by the generic equation:

$$x_1 + x_2 + x_3 + x_4 + x_5 + c_{i1} + c_{i2} = \text{Sum} + 2(\text{Carry} + C_{o1} + C_{o2})$$

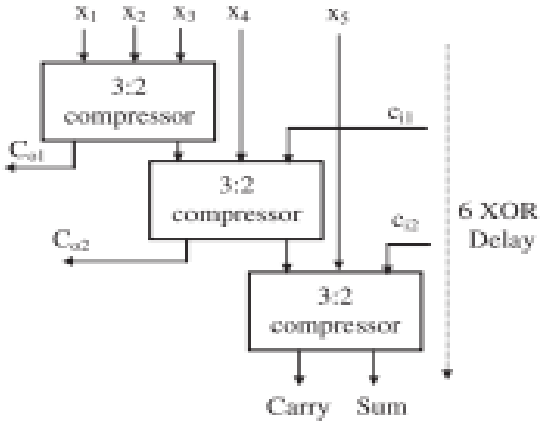

Fig 1: 5:2 Compressor Implementation using 3:2 compressors

In its simplest form, a 5:2 compressor can be designed by cascading three 3:2 compressors as shown in Fig 1. This structure has a delay of 6 XORs and is slower than the 6:2 compressor presented in [3], which has a delay of only five XORs. A faster implementation of the 5:2 compressor with 5 XOR delays is presented in [6].

III. PROPOSED OPTIMIZED 5:2 COMPRESSOR DESIGN

In this section the proposed architecture is introduced. Two improvement approaches are used to propose the new 5:2 compressor architecture. First, by a closer look at dashed box of Fig. 1, it represents the functionality of a conventional FA and can be replaced by variety of FAs presented in the literature. This replacement is expected to lead to considerable speed improvement, due to 34% faster operation of CMOS FA in comparison to two cascaded CMOS XOR gates, as it is explained in [14]. Therefore, the CMOS FA presented in [15] is used in our proposed 5:2 compressor architecture. To further improvement, we make some changes to internal equations of the 5:2 compressor to eliminate final Not gates of the CMOS FA. By doing so, we could have reduced power dissipation as well as improved operational speed. To achieve this goal, we have to use XNOR gates instead of XORs of the second stage of the architecture. Hence, we propose the architecture which is shown in Fig 2.

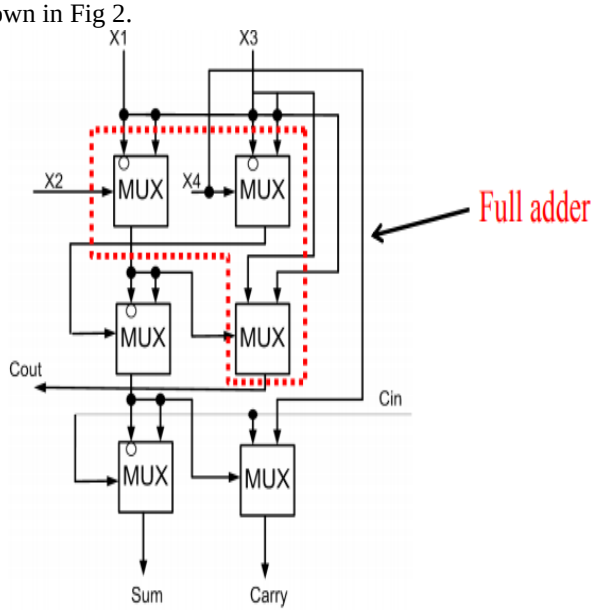

Fig 2: optimized design of 5:2 compressor

$$Sum = A \oplus B \oplus C = ABC + \overline{ABC} + \overline{A\overline{BC}} + \overline{AB\overline{C}}$$

$$Carry = AB + BC + AC$$

$$\overline{Carry} = \overline{AB} + \overline{BC} + \overline{AC}$$

By taking the NOT of Carry, we could use part of the circuit, which generates Sum signal, to generate Carry signal. Thus the higher performance of full adder could be achieved. Based on the above formulae, it is conjectured that lowering the critical path delay of the (5:2) compressor. However, it is very likely to explore different logic design styles at transistor level to achieve significantly improved low power and high-speed (52) compressor. However, in terms of power dissipation, Design 1 might be a better choice due to its use of MUX for implementing Co1, even though both circuits may have comparable values for power.

In this section, the impact of using the proposed compressors for multiplication is investigated. A fast (exact) multiplier is usually composed of three parts (or modules). In the design of a multiplier, the second module plays a pivotal role in terms of delay, power consumption and circuit complexity. Compressors have been widely used [9, 10] to speed up the CSA tree and decrease its power dissipation, so to achieve fast and low-power operation. The use of approximate compressors in the CSA tree of a multiplier results in an approximate multiplier.

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IV. SIMULATION RESULTS

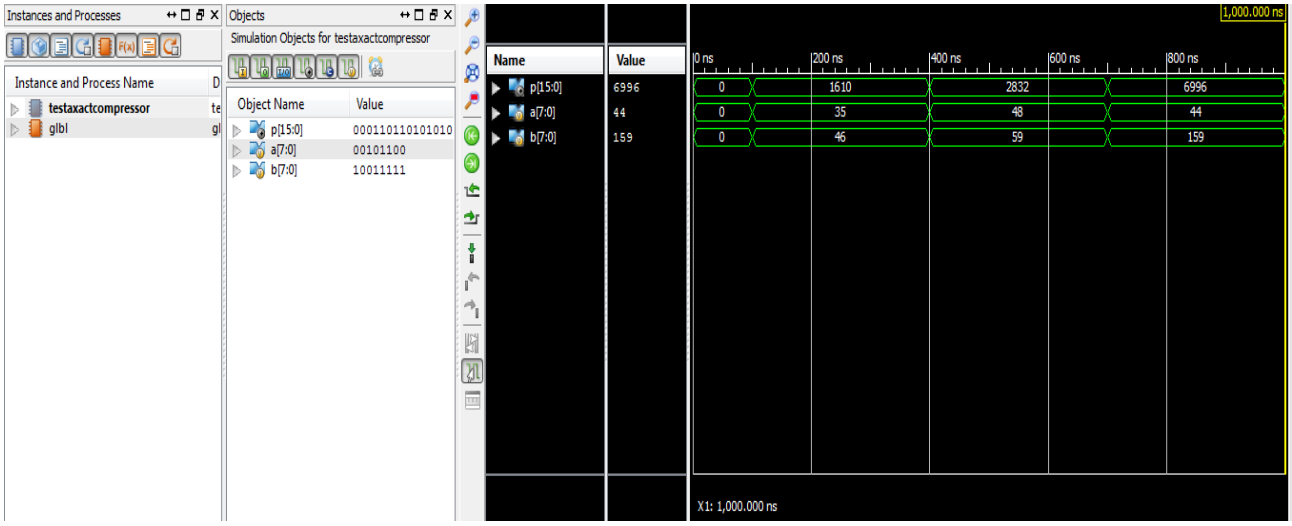

Fig 3: simulation result for the proposed dadda multiplier using optimized 5:2 compressor

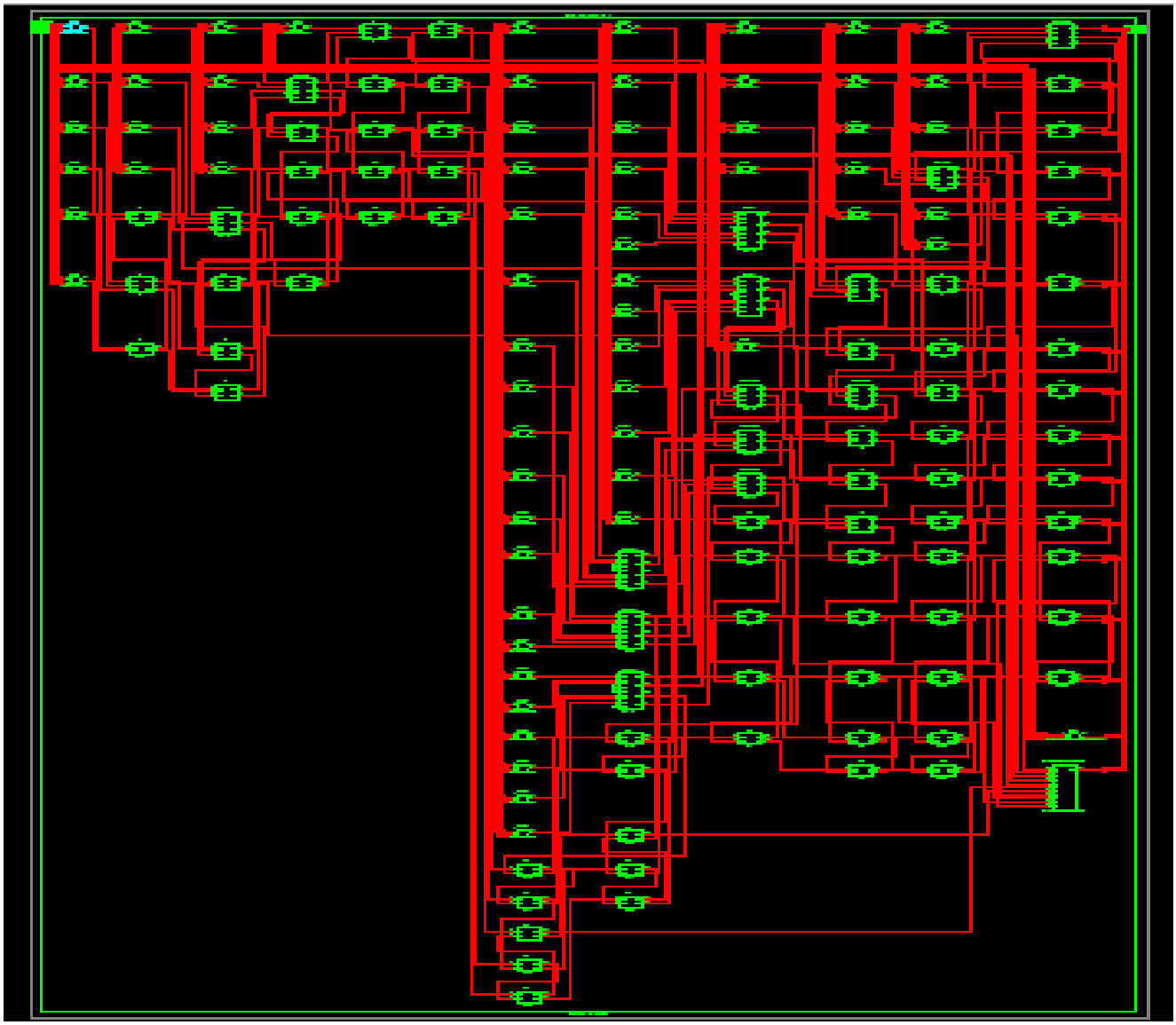

Fig 4: RTL of the proposed dadda multiplier using optimized 5:2 compressor

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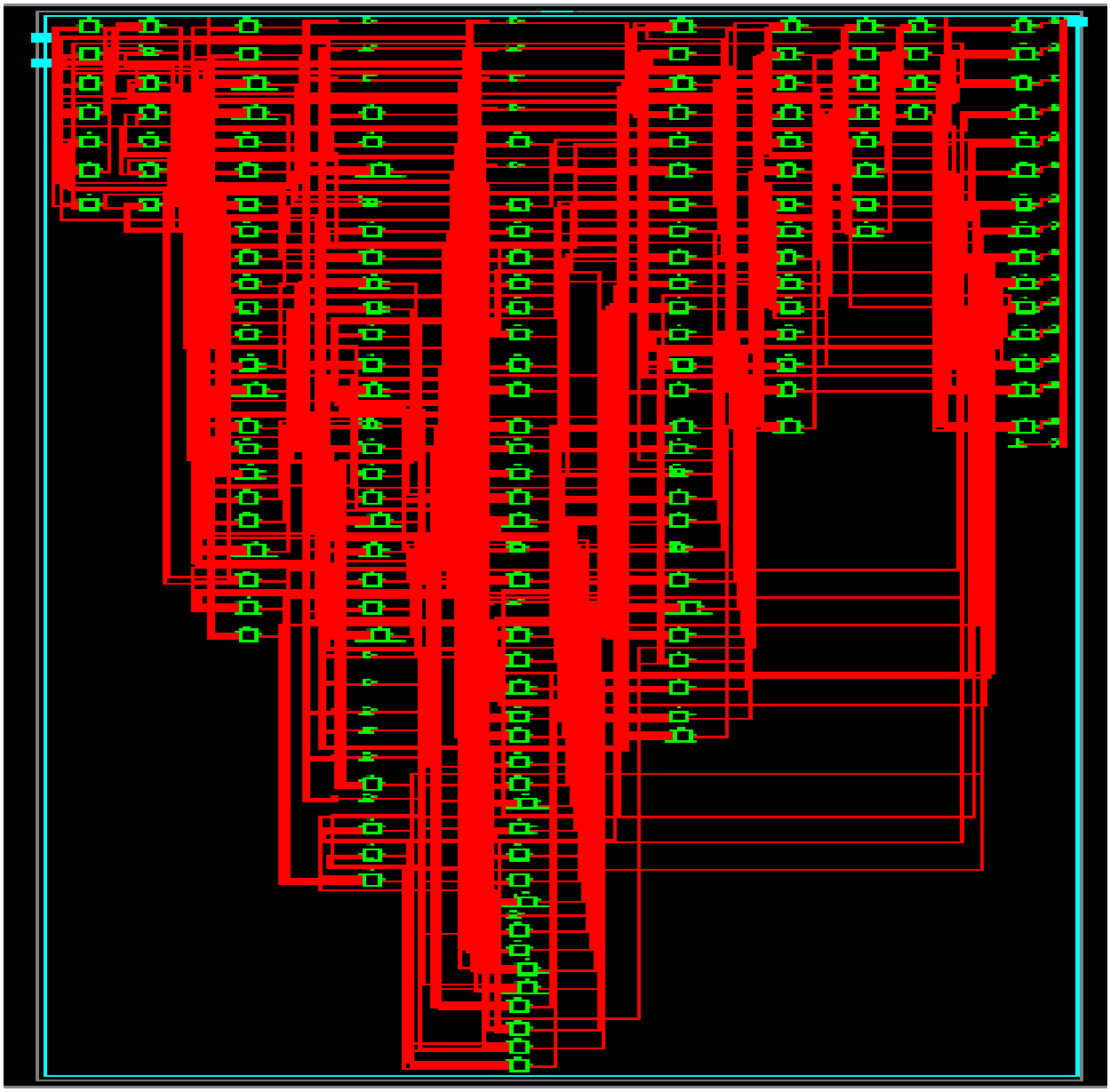

Fig 5: Technology schematic of the proposed dadda multiplier using optimized 5:2 compressor

exactmultiplication Project Status (06/28/2017 - 00:12:44)			
Project File:	jkl.xise	**Parser Errors:**	No Errors
Module Name:	exactmultiplication	**Implementation State:**	Synthesized
Target Device:	xa3s400-4pqg208	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	2 Warnings (0 new, 0 filtered)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	91	3584	2%
Number of 4 input LUTs	160	7168	2%
Number of bonded IOBs	32	141	22%

Fig 6: summary report for the proposed dadda multiplier using optimized 5:2 compressor

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V. CONCLUSION

In this paper we examined the various 5:2 compressors available in the literature and then proposed two new high-speed 5:2 compressor architectures. The new designs limit the carry propagation delay to a single compressor stage. They are then analysed for their critical delay paths and are found to be faster than the best one reported in the literature. It is concluded that the proposed architecture consumes the lowest power, operates faster and consequently is the most energy efficient one.

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