International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-6 Issue-4, April 2017

A Simplified Version of Multilevel Inverter with Minimal Number of Switches

Ch. Sankara Rao, K. Soujanya, T. Sudhakar Reddy

Abstract: ***Multilevel inverters have created a new wave of interest in industry and research. These multilevel inverters are generally used in medium voltage high power application. In this paper a eleven level inverter is proposed which has less number of switches compared to the conventional inverter. This inverter topology reduces the size and complexity of the system. The effectiveness of the proposed topology has been demonstrated and the results are validated by simulating the proposed topology in MATLAB.***

Index Terms: Multilevel Inverters, circuit topology, reduced device count.

I. INTRODUCTION

Now a day's many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multi-level inverter has been introduced since 1975 as alternative in high power and medium voltage situations. The Multi-level inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations.

Multilevel inverters continue to receive more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of Electro Magnetic Interference (EMI). The term multilevel starts with the three-level inverter introduced by Nabae et al (1981). Nowadays, multilevel inverters are becoming more popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference. Multi-level inverters can be classified to three types viz, Neutral Point Clamped (NPC), Flying Capacitor (FLC), and Cascade H-bridge. This type of inverter has advantage over the other two as it requires less number of components as compared to the other two types of inverters and so its overall weight and price is also less. This inverter can avoid extra clamping diodes or voltage balancing capacitors [3], [4]. A single phase m-level configuration of the cascaded multilevel inverter shown in the Fig.1. One of the demerits of cascade multilevel inverter is that as the number of level increases, the number of H-bridges also increases [5]. This makes the modulation strategy more.

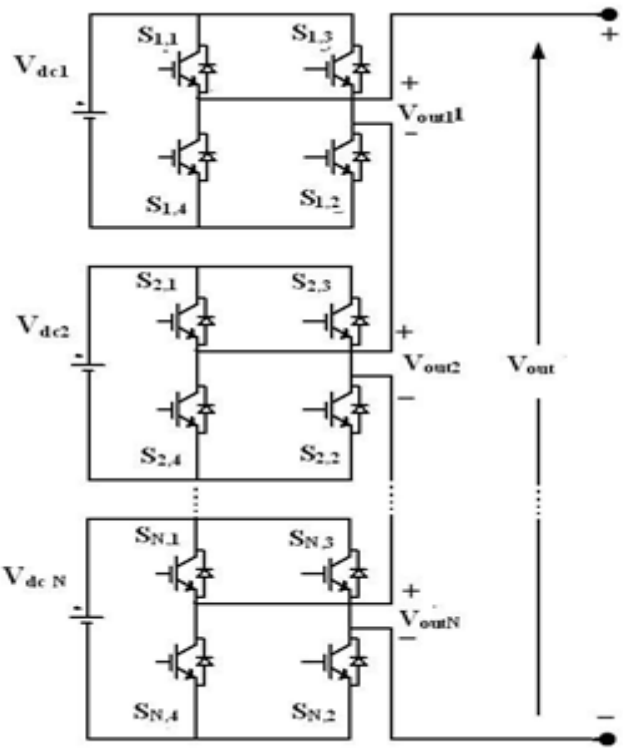

Fig.1.Conventional cascaded multilevel inverter

Multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency Pulse width Modulation (PWM). The most attractive features of a multilevel inverter are as follows:

1. They can generate output voltages with extremely low distortion and lower dv/dt.
2. They draw input current with very low distortion.
3. They generate smaller Common-Mode (CM) voltage.
4. They can operate with a lower switching frequency.

The main drawback of multilevel inverters is that the number of switches increases with the number of levels.
In spite of these drawbacks, introducing multilevel inverters will decrease switching losses occurred in the power device.

Manuscript published on 30 April 2017.
* Correspondence Author (s)
Mr.Ch Sankara Rao, Department of Electrical and Electronics Engineering, CMR College of Engineering & Technology, Hyderabad (Telangana), India. E-mail: sankarraoch@gmail.com
Mrs. K. Soujanya, Department of Electrical and Electronics Engineering, CMR College of Engineering & Technology, Hyderabad (Telangana), India. Email: itssoujis@gmail.com
Mr. T. Sudhakar Reddy, Department of Electrical and Electronics Engineering, CMR College of Engineering & Technology, Hyderabad (Telangana), India. E-mail: sudhakar.943@gmail.com

Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating.

II. TOPOLOGY OF MULTILEVEL INVERTERS

Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. There are three main types of multilevel inverters: diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors), and cascaded H-bridge inverter.

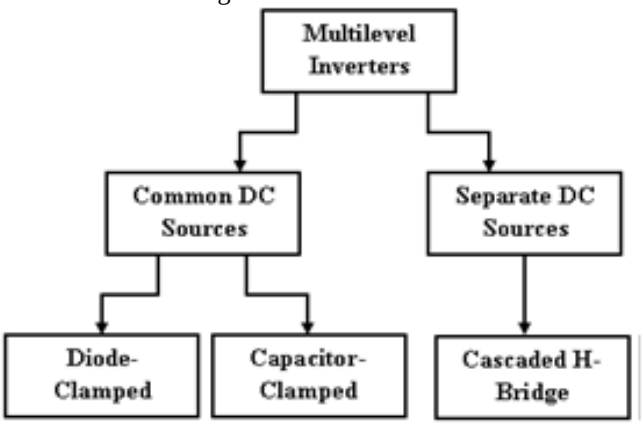

Fig.2.Topology of Multilevel Inverters

III. CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascaded Multilevel Inverter (CMLI) is built to synthesize a desired AC voltage from several levels of DC voltages. A cascaded multilevel inverter consists of a number of H-bridge inverter units with separate DC source from each unit and it is connected in cascade or series as shown in Fig.1.Each H-bridge can produce three different voltage levels $+V_{dc}$,0 and $-V_{dc}$.By connecting the DC source to AC output side by different combinations of four switches S_{11},S_{12},S_{13}&S_{14}.The AC outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs [9]. The number of output phase voltage levels m, in a cascaded inverter is defined as 'm=2s+1', where's' is the number of separate DC sources.

This paper presents a multilevel inverter, based on the study of different topologies in [9-11], with reduced number of switches as compared to conventional topologies. Hence it reduces the installation area, gate drivers needed, and consequently the cost of the whole setup [6]. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency [5] in this multilevel inverter and can be extended to any number of voltage levels. The simulation results of the proposed topology are also presented.

IV. PROPOSED MULTILEVEL INVERTER

The proposed multilevel topology is a simplified multilevel inverter and is shown in Fig.3. In this proposed topology of multilevel inverter the switches from S_1 to S_5 generates the required output levels and the switches S_6 to S_7 of the circuit (H-bridge inverter) decides about the polarity of the output voltage. The H-bridge is responsible for generating the polarity of the output voltage. H-bridge consisting of four switches which are operated at fundamental frequency. It requires 9 switches and five isolated sources of equal DC value.

A. General Description

The proposed system consists of a normal H bridge inverter and some auxiliary switches. The levels are generated by switching the switches from S_1 to $S_5$and according to how the sources are connected to the load. The circuit consists of an H bridge with switches S_6, S_7, S_8&S_9 which are switched at natural frequency to produce the positive and negative half cycles.

During positive half cycle, switches S_6 and $S_7$are turned on and during the negative half cycle, switches S_8 and S_9 are turned on. To obtain the first level, the dc source V_5 must be connected to the load. To generate the second level, both V_5 and V_4must be connected to the load. The rest of the sources are also connected in steps to the load in similar manner. The switches are controlled in such a way that respective sources are connected to the load during desired time intervals.

In the proposed topology the total switch count is 9 for an eleven level multilevel inverter, in case of a conventional cascaded multilevel inverter it is 20. Number of switches are reduced in this topology reducing the complexity and cost of the overall system.

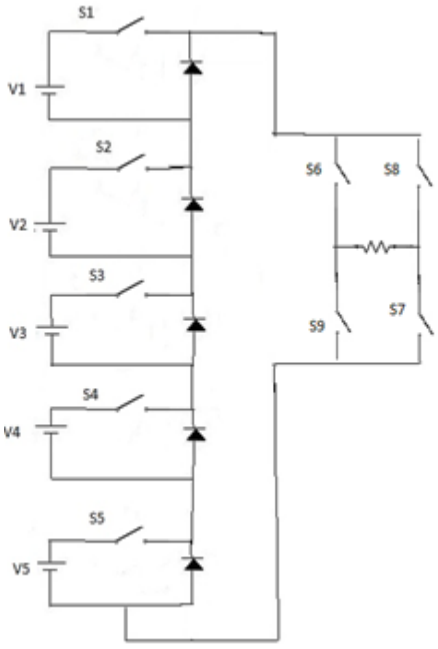

Fig. 3. Proposed Multilevel Inverter

B. Switching Sequence

Switching sequences in the proposed multilevel inverter are simpler as compared to conventional topologies. The control signals are generated based on the timing intervals without using any PWM technique.Table.1. shows the switching sequence of the proposed topology. Switches (S_1 to S_5) are used for the level generation

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

Table.1. Switching Table

Vo	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$5V_{dc}$	1	1	1	1	1	1	1	0	0
$4V_{dc}$	0	1	1	1	1	1	1	0	0
$3V_{dc}$	0	0	1	1	1	1	1	0	0
$2V_{dc}$	0	0	0	1	1	1	1	0	0
V_{dc}	0	0	0	0	1	1	1	0	0
0	0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	0	1	0	1
$-V_{dc}$	0	0	0	0	1	0	0	1	1
$-2V_{dc}$	0	0	0	1	1	0	0	1	1
$-3V_{dc}$	0	0	1	1	1	0	0	1	1
$-4V_{dc}$	0	1	1	1	1	0	0	1	1
$-5V_{dc}$	1	1	1	1	1	0	0	1	1

C. Simulation Results

The simulation has been carried out in MATLAB/Simulink to validate the result. Fig.4. shows the simulation model of the proposed topology. To generate the 11- level output voltage, 9 IGBTs and five DC power sources of 50Volts are used. Output voltage is shown in Fig.5 and the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

The 11 level inverter output is shown in Fig.5.and the switching pulses are shown in Fig.6. The output voltage has 11 levels of voltages in a half which resembles much more to a sine wave. As a result, the harmonic spectrum of the output will be improved. The FFT analysis of the output voltage waveform is carried out to find the THD of the output voltage

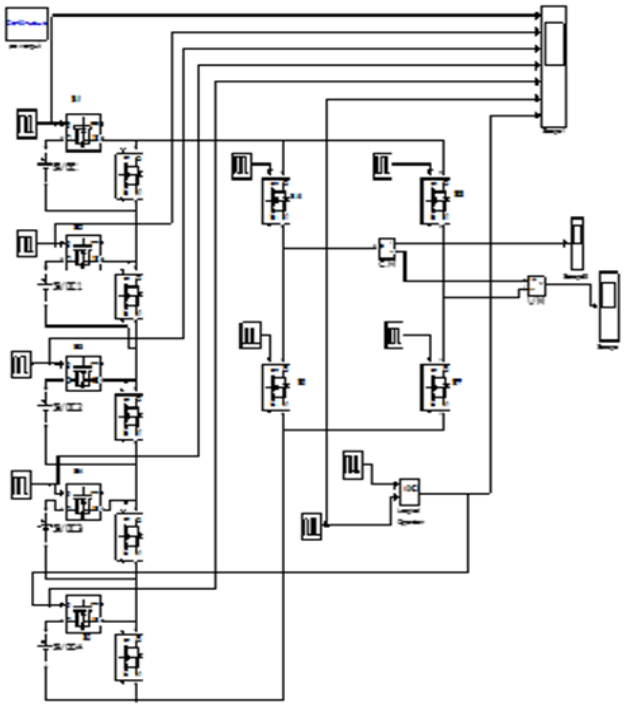

Fig.4.Simulation model of the proposed inverter

waveform shown in Fig.7. Table.2. shows the comparison with conventional cascaded multilevel inverter with proposed system. Total harmonic distortion (THD) of the proposed topology is 15.5%.

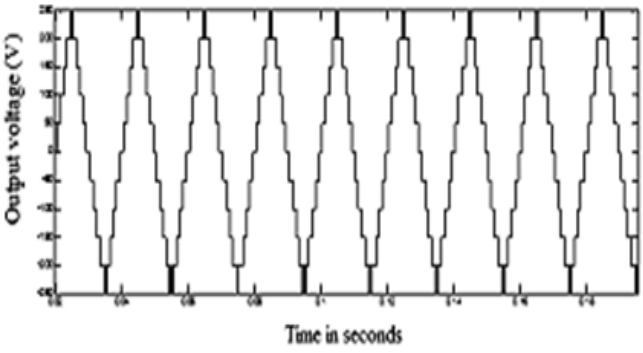

Fig.5.Output Voltage of proposed inverter

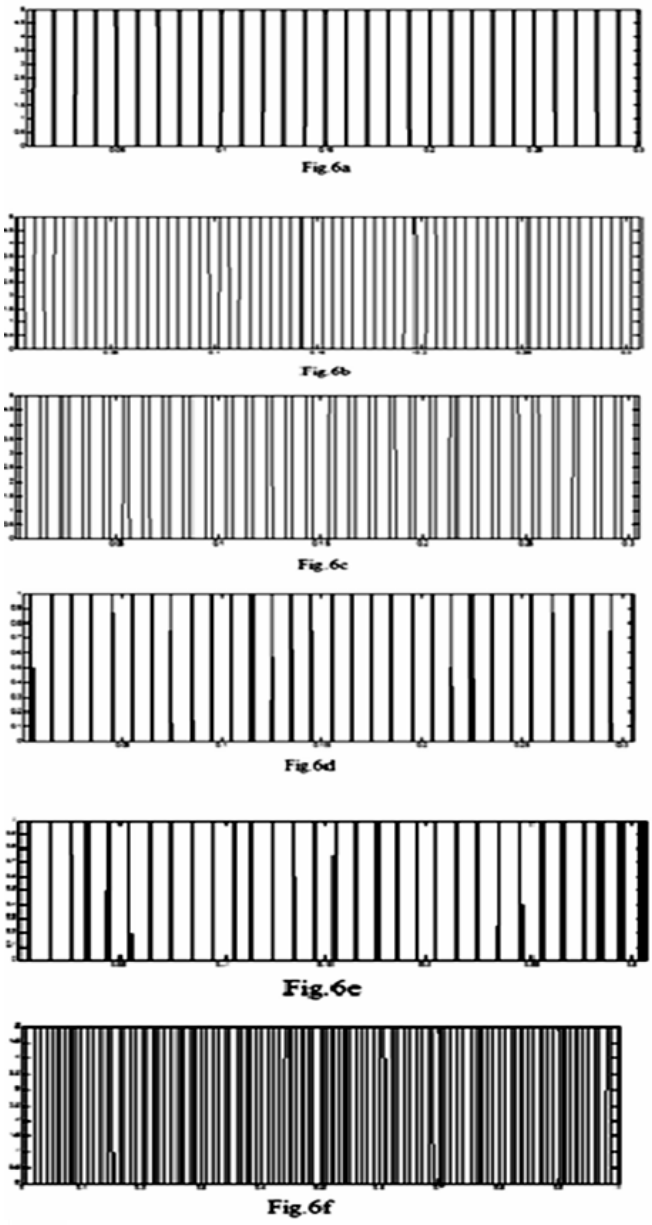

Fig.6.Switching pulses

(a) Switching pulses to S1(b)switching pulses to S2
(c) Switching pulses to S3 (d) switching pulses to S4
(e)Switching pulses to S5 (f) switching pulses to S6, S7
(g)Switching pulses to S8, S9

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

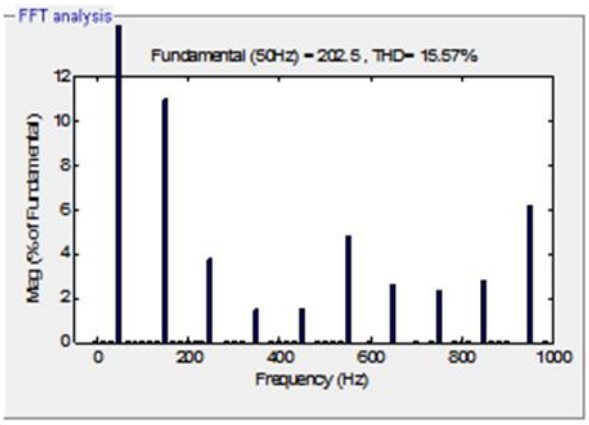

Fig.7. FFT analysis of output voltage

Table. 2. Comparison with Conventional Topology

Topology	Number of levels	Number of switches	THD
Cascaded Multilevel Inverter [16]	11	20	15.90%
Proposed Multilevel Inverter	11	9	15.57%

V. CONCLUSIONS

A simplified eleven level multilevel inverter topology with less number of switches is shown and simulated in MATLAB. This topology consists of 9 switches which reduces the overall size, cost and installation area of the system. Simulation results using MATLAB is also provided to validate the design.

The proposed topology can be extended in levels by increasing the number of switches and the DC input can be extracted by renewable energy sources. This multilevel inverter can be applicable for any single phase AC drives.

REFERENCES

1. Abdul Halim Mohamed Yatim, and Ehsan Najafi, "Design and Implementation of a New Multilevel Inverter Topology" IEEE transactions on industrial electronics, vol. 59, no. 11, November 2012.
2. A.Kirubakaran, Jacob James Nedumgatt, Vijayakumar D. Umashankar S, "A Multilevel Inverter with Reduced Number of Switches"2012, IEEE Students Conference on Electrical, Electronics and Computer Science.
3. Mariusz Malinowski,K. Gopakumar Jose Rodriguez, and Marcelo A. Pérez—A Survey on Cascaded Multilevel Inverters‖ IEEE Transactions On Industrial Electronics, Vol. 57, No. 7, July 2010.
4. José Rodríguez, Jih-Sheng Lai,, And Fang Zheng Peng, " Multilevel Inverters: A Survey Of Topologies, Controls, And Applications" IEEE Transactions On Industrial Electronics, Vol. 49, No. 4, August 2002.
5. Oscar Lopez, Remus Teodoreescu, "Multilevel transformerless topologies for single phase grid-connected converter", IEEE conference, 2006.
6. Johnson Uthayakumar R.1, Natarajan S.P.2, Bensraj R, "A Carrier Overlapping PWM Technique for Seven Level Asymmetrical Multilevel Inverter with various References" IOSR Journal of Engineering June. 2012.
7. N Booma, Nagisetty Sridhar, "Simulation of nine level cascaded H-bridge multilevel inverter DC-link inverter" IEEE Students Conference on Electrical, Electronics and Computer Science.2011.
8. Valsan K, Joseph K.D"A Reduced Switch Multilevel Inverter for Harmonic Reduction" IEEE Conference.2012.
9. Ahmed, R.A.; Mekhilef, S.; Hew Wooi Ping,"New multilevel inverter topology with minimum number of switches," 2010 IEEERegion 10 Conference (TENCON 2010),vol. no.2, pp.1862-1867, Nov. 2010.
10. Hulusi Karaca "A Novel Topology for Multilevel Inverter with Reduced Number of Switches", World Congress on Engineering and Computer Science, WCECS, 2013, SanFrancisco, USA, vol I, 23-25 October, 2013.
11. Ceglia, G., Guzman, V.; Sanchez, C.; Ibanez,F.; Walter, J.; Gimenez, M.I. "A New Simplified Multilevel Inverter Topology for DC & AC Conversion", IEEE Transactions on Power Electronics, vol.21, no.5, pp.1311-1319, Sept. 2006.
12. Arjun J. Jariwala, Nilesh V. Shah "A new Multilevel Inverter Topology with reduced number of switches" International Journal of Current Engineering and scientific Research (IJCESR) ISSN (PRINT): 2393-8374, (Online): 2394-0697, Volume-2, Issue-7, 2015
13. Ebrahim Babaei. "A Cascade Multilevel Converter Topology with Reduced Number of Switches". IEEE Trans. On Power electronics. 2008; 23(6): 2657-2664.
14. R Naveen Kumar. "Energy Management system for Hybrid RES with Hybrid Cascaded Multilevel inverter". International Journal of Electrical and Computer Engineering (IJECE). 2014; 4(1): 24~30.
15. Gnana Prakash M, Balamurugan M, Umashankar S"A New Multilevel Inverter with Reduced Number of Switches"International Journal of Power Electronics and Drive System (IJPEDS)Vol. 5, No. 1, July 2014, pp. 63~70ISSN: 2088-8694
16. Aditya Parasha "International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 International Conference on Emerging Trends in Mechanical and Electrical Engineering" (ICETMEE- 13th-14th March 2014)

Authors Profile

Mr. Ch.Sankar Rao received B.Tech Degree in Electrical and Electronics Engineering from Bapatla Engineering College in the year 2003 and M. Tech., Degree in Power Electronics from JNTU Hyderabad in the year 2010 .He is currently working as Associate Professor in CMR college of Engineering & Technology Hyderabad, Telangana. He has over 11 years of teaching experience in the field of Electrical Engineering. His areas of Interests include Power Electronics, Electric drives and HVDC &FACTS.

Mrs. K. Soujanya received B.Tech Degree in Electrical and Electronics Engineering from University College of Engineering, Kakatiya University in the year 2001 and M. Tech., Degree in Power Electronics from NIT Warangal in the year 2005.She is currently working as Associate Professor in CMR college of Engineering & Technology Hyderabad, Telangana. She has over 13 years of teaching experience in the field of Electrical Engineering. Her areas of Interests include Power Electronics, Electric drives and FACTS.

Mr. T. Sudhakar Reddy received B.Tech Degree inElectrical and Electronics Engineering from Kakatiya University in the year 2004 and M. Tech., Degree in Power Systems from Bharat University in the year 2007. He is currently working as Associate Professor in CMR college of Engineering & Technology Hyderabad, Telangana. He has over 11 years of teaching experience in the field of Electrical Engineering. His areas of Interests include Power Systems, Electric Circuits and Control Systems.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)