Design and Simulation of 16 Bit Arithmetic Unit using Gating Techniques in Cadence 45nm Technology

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Abstract: ***In any system ALU is the most important part of a processor as it is required for calculating the address of each memory location. It performs a particular arithmetic and logic operations on each set of operands, based upon the instructions given by the processor. In some processors ALU is split into two units, an Arithmetic unit (AU) and logic unit (LU). Some processors possess a couple of Arithmetic units – one for the fixed point operations and another for the floating point operations. As AU operates at a very high speed and it is accessed by the system frequently, it contributes to one of the highest power-density locations on the processor. Because of this reason, there exist thermal hotspots and sharp temperature gradients inside the execution core, thereby reducing the reliability as well as the battery life of the system. Therefore, there is a great need for the development of a power optimized AU design. This encourages powerfully for the design of a power optimized AU that satisfies the superior needs along with the reduction of average power consumption. This paper presents the various power optimized techniques for 16bit ALU like input gating, power gating in 45nm using cadence. Finally, comparison among all proposed techniques are represented.***

Index Terms: Arithmetic unit (AU), Power gating, Input Gating.

I. INTRODUCTION

An AU is an essential in most of the electronic devices and is designed in an order to perform the arithmetic operations, the operations performed by the AU includes addition, subtraction and multiplication. Since AU's are designed to carry out only the integer operations, they perform only the addition, subtraction and multiplication of any two integers, as their result is also an integer. Therefore, it does not handle division operation since its output may be a fraction. Division operations are handled by the Floating Point Unit (FPU). This FPU also handles all other non-integer calculations.

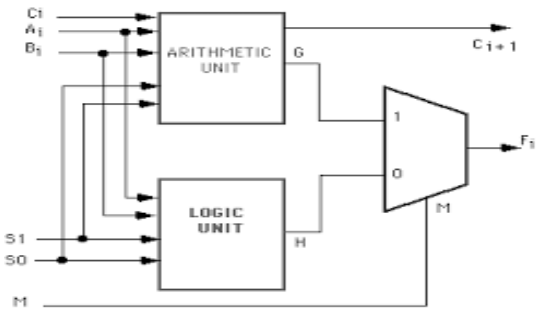

Figure1. Architecture of Arithmetic and Logical Unit

Figure1 shows generalized block diagram of ALU. It is divided two separate units to carry out arithmetic and logic operations. The unit used specifically for performing arithmetic operations is called as an Arithmetic Unit and the unit that builds Logic operations is called as Logic Unit. In this project first a traditional 8 bit AU is designed and then it is modified by applying the Power Gating and Input Gating [1] [2] techniques to build a power optimized 16 bit AU. The AU in this project is designed to perform the following arithmetic operations.

1.1. Addition

Among all the arithmetic operations addition is the most basic operation. The component that performs an addition operation is referred as an Adder. The function of this adder is to sum up two numbers of the same or different length into a single quantity. These two numbers are called as addends and augends, whereas the resulting single quantity is called as the summation. It is also possible to add array of numbers into a single quantity by means of repeated addition.

For example, 0010(decimal 2) + 0111 (decimal 7) = 1001 (decimal 9)

1.2. Subtraction

Another most basic arithmetic operation performed by an AU is Subtraction. It is quite opposite to that of the addition operation. Consider a binary number and then add any binary number to that after which subtract the same binary number that added then it will be left out with a single number that it started with. Usually subtraction is represented by a minus sign in infix notation.

For example, 0111(decimal 7) - 0010 (decimal 2) = 0101 (decimal 5)

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1.3. Multiplication

The third most important operation of an AU is multiplication. It considers two binary numbers as inputs and then produces a single quantity as output. These two inputs are referred as multiplier and multiplicand, sometimes both with no trouble referred as factors and their resulting output is called as the product. In this paper a 16bit bit Wallace tree multiplier is used because of its high performance applications. This Wallace tree multiplier consists of AND gates half adder and full adders and compressors

1.4. Logic Unit

There are mainly 7 types of logic gates [3] that are used in representing any Boolean expression. By combining them in different ways, will be able to implement all types of digital components. Each basic logic gate and their operations are explained below.

A Logic Gate is an elementary building block of digital circuits. Logic gate is a device which has the ability to produce one output level with the combinations of all input levels. There are generally seven basic types of logic gates are available and they are:

- AND GATE
- OR GATE
- NOT GATE
- NAND GATE
- NOR GATE
- EXCLUSIVE-OR GATE (X-OR) GATE
- EXCLUSIVE-NOR (X-NOR) GATE

The reason behind it is the computers are capable of performing complex operation and is possible with the help of interconnection of these gates. Generally, Logic gates are implemented with transistors, diodes, relays, optics and molecules or by several mechanical elements. The logic gates can be built up in a wide variety forms such as large-scale integrated circuits (LSI), very large-scale integrated circuits (VLSI) and also in small-scale integrated circuits (SSI). Here the inputs and output of all the logic gates of integrated devices can be accessible and also the external connections are made available to them.

Inputs and outputs of any logic gate are in two types, termed as Logic HIGH and Logic LOW, or TRUE and FALSE, or ON and OFF, or simply logic'1' and logic'0'. A table which list out the combination of inputs and the corresponding outputs is termed as "TRUTH TABLE". It explains how the logic circuit output responds to various combinations of inputs at different logic levels. Here the following level logic, in which the voltage levels are, represented as logic 1 and logic 0. Level logic is of two types such as positive logic or negative logic. In the positive logic system, the higher of the two voltage levels are represented as 1 and lower of the two voltage levels are represented as 0. But in the negative logic system, the higher of the two voltage levels are represented as 0 and lower levels are represented as 1.

II. METHODOLOGY

The Methodology in this paper includes two power reduction gating techniques. They are,

1. Power gating.
2. Input gating

2.1. Power Gating

In Power Gating technique[4][5], the power supply is controlled by feeding it through a pair of NMOS transistors, i.e., the VDD is fed through one NMOS transistor and GND is fed through another NMOS transistor. The gate terminal of both transistors are controlled by the ENABLE signal of that respective arithmetic module, thus power supply is provided only if the ENABLE signal is made HIGH otherwise the power supply is blocked for that module therefore, reducing the static power consumption of all the modules whose operation is not required. The schematic of an Arithmetic module with Power Gating is as shown in figure 2.1.

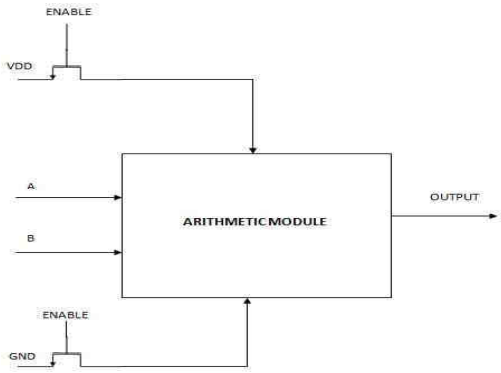

Figure 2.1 Power Gating

2.2 Power-Gating (PG) Parameters

To achieve long term leakage power reduction through an externally switched power supply is a very basic form of power gating. Internal power gating is suitable to shut off the block for small time intervals. Power can be controlled by power gating controllers, CMOS switches are used to provide power to the circuitry. The output block discharges slowly when power is gated. Therefore voltage levels of the output block spend more time in threshold voltage level (V_{TH}), hence it leads to larger short circuit current in the circuit. Low-leakage PMOS transistors can be used as header switches to shut off power supplies, the Power Gating parts of a design in the mode of sleep or standby. NMOS footer switches are also used as sleep transistors in the design of the power gating technique. These sleep transistors can be inserted to split the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells. By using of cell- or cluster-based (or fine grain) approach or a distributed coarse-grained approach Power Gating can be implemented.

For a successful implementation of this methodology the following parameters are needed to be considered and their values must be carefully chosen.

1. Size of the Power Gate: The size of the power gate denotes the amount of switching current at any point of given time. The gate must be chosen bigger such that there is no measurable voltage (IR) drop due to the gate. The size of the gate is selected to be approximately 3 times of the switching capacitance because as a Rule of Thumb [9]. The Designers can also chosen header (P-MOS) or footer (N-MOS) gate for the designing low power circuits. For the same switching current N-MOS footer gates are smaller in area. Switching current can be accurately measured by using of Dynamic

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power analysis tools & can predict the size for the Power Gate

2. Slew rate: The determination of power gating efficiency is an important parameter in power gating. It takes more time to switch off and switch-on the circuit when the slew rate is large; hence it is affected on the power gating efficiency also. The gate control signal is used to control the slew rate

3. Switching Capacitance: This is the most important constraint refers to that without affecting the power network integrity [6], the amount of the circuit can be switched simultaneously. If a large amount of the circuit is switched. The resulting "rush current" can be compromises the power network integrity. The circuit needs to switch in all the stages in order to prevent this.

4. Leakage of Power Gate: leakage reduction is an important consideration to maximize power savings this is achieved by using an active transistor while designing of power gates.

2.3. Fine Grain Power Gating (FGPG)

Sleep transistor is added to every cell when they turned off they imposes a large area & individually gating the power of every cluster of cells creates timing issues introduced by inter-cluster voltage variation, these are very difficult to resolve. FGPG summarize the switching transistor as a part of the standard cell logic in the design. The library IP vendor or standard cell the designer is used to design the Switching transistors [7]. Usually these cell designs can easily be handled by EDA tools for implementation & confined to the normal standard cell rules. The gate control size is designed and considering the worst case scenario that it will require the circuit to switch during every clock cycle, in a huge area impact on the result only for the low V_T cells some of the recent designs implement the FGPG selectively. If the multiple V_T libraries are allowed by the technology then in the design the use of low V_T devices (20%) is minimized, so the area can be reduced. If the next stage is a high V_T cell, then the output must be isolated in the low V_T cells by using of PG'S. When output goes to an unknown state due to power gating, it can cause the neighboring high V_T cell to have leaked [8].

Slew rate of Gate control constraint is achieved by having a buffer distribution. Buffers without the gate control signal are designed with high V_T cells (The buffers must be chosen from a set of always on buffers). When a cell switches off, it minimizes the rush current during the switch-off & switch-on. Usually the high V_T device is designed as a gating transistor. CGPG offers provides flexibility by optimizing the PG cells where there is low switching activity in the design. At the CG level, Leakage optimization had to be done with changing the high leakage cell with the low leakage cell. FGPG is a methodology resulting in leakage reduction up to 10 times compared with conventional. If the power reduction requirement is not satisfied by multiple V_T optimizations, this type of power reduction makes it captivating technique.

2.4 Coarse-Grain Power Gating (CGPG)

The CGPG Process implements with the grid style sleep transistors which drives cells through shared virtual power networks. This technique is in less IR-drop variation, introduces less sensitive to V_T variation & imposes a smaller area overhead than the implementations based on the cell- or cluster. In CGPG, the PG transistor is a part of the power distribution network rather than the standard cell. Implementation of a CG structure is in two ways those are

- **Based on Ring:** The power gates are placed around the perimeter of the module that is it formed as a Ring [10] when module is switched-off. To turn the power signals around the corners by using of special corner cells
- **Based on Column:** Within the module the power gates are inserted with the cells adjacent to each other in the form of columns. The switched power is in the lower layers, while the global power is the higher layers of metal. At any given time, overall switching current of the module depends on the Gate sizing [11]. Therefore only a fraction of circuits switch at any point of time, FG switches are larger as compared to the Power Gate sizes. By using of worst case vectors, can determine the worst case switching for the module and the size in dynamic power simulation. In the analysis the IR drop can also be factors. A major consideration in CGPG implementation is Simultaneous switching capacitance. By the simultaneous switching special counters can be used to selectively turn on blocks of switches & in order to limit simultaneous switching, gate control buffers can be daisy chained.

2.5 Input Gating

Similar to the Power Gating, in Input Gating[12][13] technique inputs are fed to only one block whose ENABLE signal is made HIGH. Otherwise the inputs for the modules are blocked i.e., not fed to the circuit, thereby reducing the power consumption resulting from the unnecessary switching in the other blocks. The ENABLE signal of a block is made HIGH if and only if its operation is required. The schematic of an Arithmetic module with Input Gating is shown in the figure 2.2

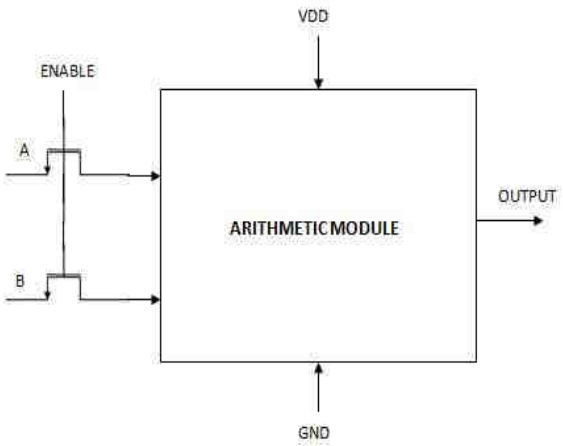

Figure 2.2 Input Gating

In Input Gating technique [14], add NMOS transistors to the inputs of the required module to design proposed Wallace tree multiplier and parallel adder and subtractor [15].

III. DESIGN AND SIMULATION

Full adder is a combination of two Half Adders and a OR gate. It has three inputs (i.e.) a, b and c_{in} and outputs are sum and

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carry. Here c_{in} is connected has input to second half adder.

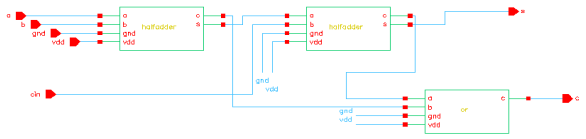


Figure 3.1 schematic of Full Adder

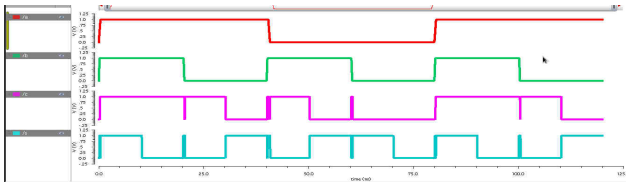


Figure 3.2 Output of Full Adder

With the help of above full adder implemented a 6 to 2 compressor. It is build by using five full adders. It has nine inputs (i.e.) i1, i2, i3, i4, i5, i6, i7, cino, cin1 and has four outputs sum, carry, cout0, cout1 figure 3.3 and figure 3.4 shows the schematic and simulation waveforms.

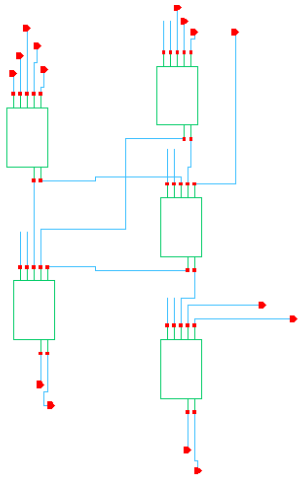


Figure 3.3 Schematic of 6to2 Compressor

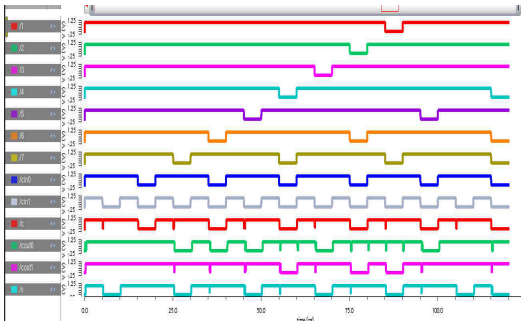


Figure 3.4 Output of 6to2 Compressor

The 4bit Wallace tree multiplier has eight inputs (i.e.) a_0 to a_4, b_0 to b_4 and eight outputs z_0 to z_7 here z_7 is carry. 4bit Wallace tree multiplier is built by using 5to2 compressors and 4to2 compressor and a half adder and full adder. Figure 3.5 and figure 3.6 shows the schematic and simulation waveforms.

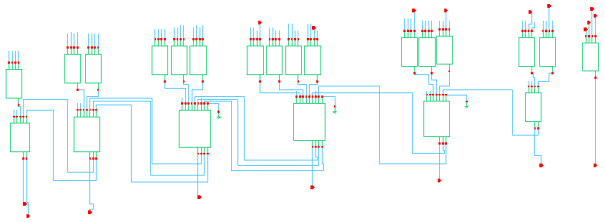


Figure 3.5 Schematic of 4 bit Wallace Tree Multiplier

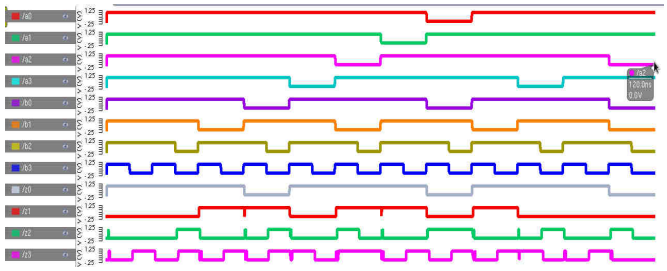


Figure 3.6 Output of 4 bit Wallace Tree Multiplier

The 16bit Wallace tree multiplier is designed by using compressors. It has 32 inputs i.e., a_0 to a_{31} and b_0 to b_{31} and Wallace tree multiplier has 32 outputs i.e., from z_0 to z_{31}.figure 3.7 and figure 3.8 shows the schematic and simulation waveforms.

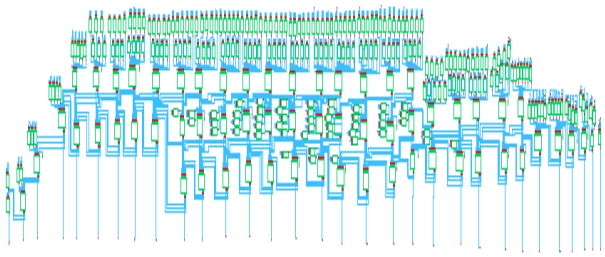


Figure 3.7 Schematic of 16bit Wallace Tree Multiplier

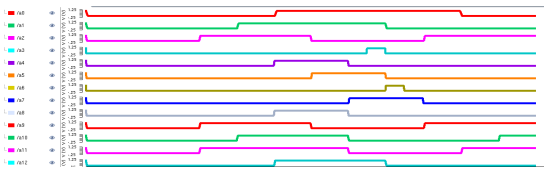
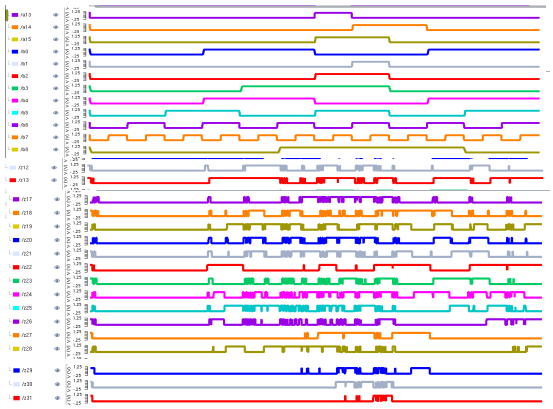


Figure 3.8 Output of 16 bit Wallace Tree Multiplier



Input gating of arithmetic unit has input gating of Wallace tree multiplier and input gating of parallel adder/ subtractor [16]. It consists of demux to route the enable signal. In demux if Enable is '0' and V_{IN} is '1' parallel adder and subtractor will

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be ON and if Enable is '1' and V_{IN} is '1' Wallace tree multiplier will be ON. Figure 3.9 and figure 3.10 shows the schematic and simulation waveforms.

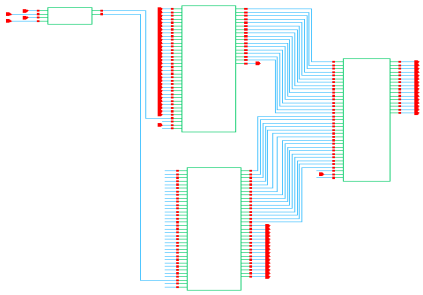

Figure 3.9 Schematic of 16 bit Arithmetic Unit Input Gating

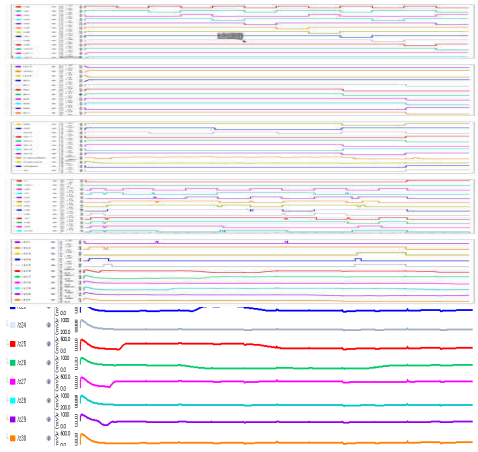

Figure 3.10 Output of 16 bit Arithmetic Unit Input Gating

Similarly ALU circuits are designed with different technologies such as power gating; power gating and input gating next chapter gives the comparison among various technologies in terms of Power and delay.

IV. RESULT

Use Power and delay calculations of, Arithmetic Unit and Arithmetic Unit with Input Gating, Power Gating and Combination of Power Gating and Input Gating are as follows.

Table 4.1 Comparison table

	Power Calculations (watts)	Delay Calculations (seconds)
16 bit Traditional Arithmetic Unit	1.77E-03	5.34E-09
16 bit AU With Power Gating and Input Gating	1.28E-04	6.02E-09
16 bit AU With Input Gating	1.54E-03	6.65E-10
16 bit AU With Power Gating	1.26E-04	2.84E-09

V. FUTURE SCOPE

In future this technique helpful for designing of 32 bit or 64 bit ALU with power consumption. These ALUs are used in processors, so that there will be less power consumed. In future using same technique with small modifications we can also reduce the leakage power.

VI. CONCLUSION

In this paper, 16-bit AUs with Power Gating, Input Gating and a combination of Power Gating and Input Gating have been proposed, designed, simulated and verified for their functionality using cadence virtuoso ADE spectre. A traditional 16 bit AU was designed; its power consumption and delay were compared to that of the proposed AU's. The power is measured from output waveforms of the AUs using Cadence XL Browser and XL calculator.

In traditional AU, Power consumption was 1.77mWatts and delay was 5.34nsec. By employing a combination of input and power gating, power consumption reduced to 128.2µWatts and the delay slightly increased to 6.02nsec. Power consumption and delay were further reduced by using power gating and input gating individually. When the only power gating technique is used the power consumption is reduced to 126.7µWatts and delay was 2.84nsec. When the Input gating technique is used the delay has been reduced to 665psec and power consumption is 1.54mWatts. When compared to the traditional AUs, obtained results show that power consumption can be reduced by the power gating technique and delay can be reduced by using the input gating technique.

Therefore, power gating technique is an effective method for reducing the static power dissipation in arithmetic circuits among all.

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