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ESD Induced Reliability Problems in Space Grade Devices

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Abstract: ***ESD induced reliability problems in an IC have been studied in detail. PEM (Photon Emission Microscopy) analysis has indicated characteristic emission spots at same location from all the failed devices. Reprocessing of the failed device reveals Gate oxide rupture as root cause of the failure. Protection circuits have been designed to prevent ESD induced damage to the devices. The devices are found to be safe till 4500 V stress after protection circuit is implemented.***

Keywords: ESD (Electro Static Discharge), HBM (Human Body Model), PEM (Photon Emission Microscope), BPSG (Boron Phosphorous silicate glass)

I. INTRODUCTION

Reliability of semiconductor devices used in space craft applications attains significant importance owing its impact on performance of sub systems and whole space craft. Reliability of devices for space craft applications is ensured thorough usage of Mil Grade devices and carrying out rigorous qualifications and screening tests at component level, card level and subsystem level. Objective of all these qualifications tests is to weed out devices having latent defects which otherwise might cause significant damage to subsystem at later stage.

The devices have been screened through rigorous qualifications tests which include Gamma Radiation Assurance test, Temperature cycling test, Particle Impact Noise Detection test, Static Burn in test, Dynamic Burn in test, Fine and Gross leak test etc. In spite of all these tests, one of the health monitoring cards is found to fail exhibiting excess channel current. This card contains four numbers of HS – 1840 RH devices. HS – 1840 RH is a Radiation hardened 16 channel CMOS analog multiplexer. Electrical performance test is conducted on couple of good devices (HS – 1840 RH) from different lots. All these devices meet the electrical specifications within the limit. These devices are tested for ESD stresses as per MIL standard 883 (3015.7). Many of these devices found to fail during ESD testing in HBM model. The increased leakage current after ESD stress have good correlation with increased leakage current observed at card level testing. Hence it is suspected that ESD induced failure could be cause for the card level failure.

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II. ESD INDUCED FAILURES

The good devices from different lots were subjected to ESD test with Human Body Model (HBM). Devices are tested with Electro Tech System (Model 910) with HBM configuration. The HBM configuration for ESD testing is shown in the Figure 1.

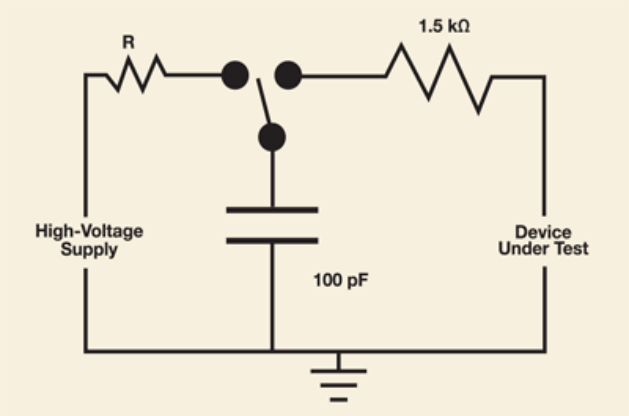

Figure 1: HBM configuration for ESD testing.

High voltage pulses of about 250 ns duration are applied to I/O pins and device is tested for any increase in leakage current. The acceptable leakage current is less than 1 micro A. After ESD testing, devices have exhibited leakage current in excess of 7000 micro A.
The ESD stress pulse is shown in the Figure 2.

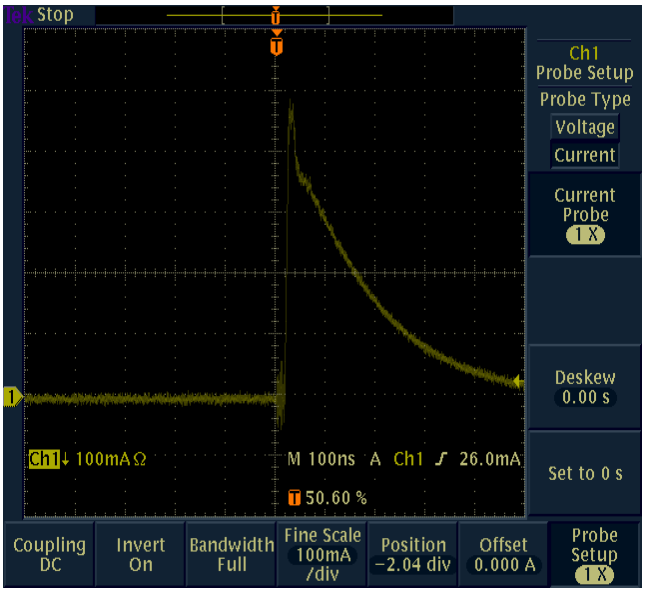

Figure 2: ESD Stress pulse

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III. ANALYSIS

The failed devices have been decamped and observed in optical microscope. No visible defects / damage are noticed near the I/O pads. Optical micrograph of failed device is shown in the Figure 2.

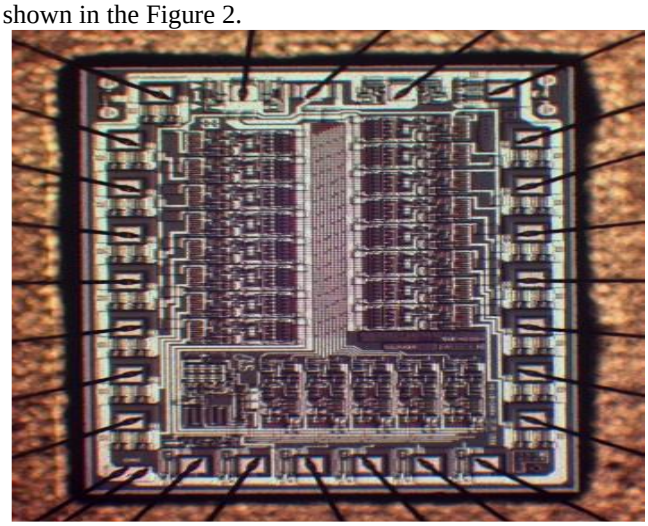

Figure 3: Optical micrograph showing no damage / visible defects near failed I/O pads

The failed devices were then studied in Photon Emission Microscope (PEM). Emission spots were noticed in failed devices as shown in the Figure 3.

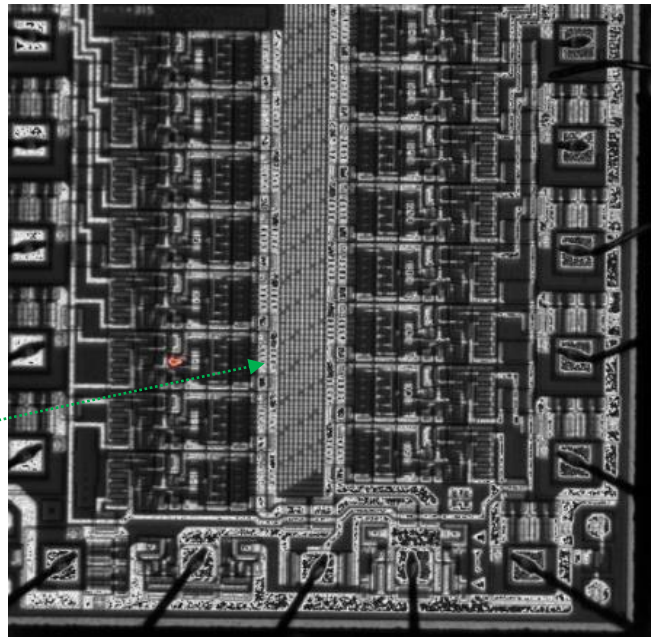

Figure 4: Emission spot displayed by PEM analysis.

All the failed devices have shown emission spot at same location. The emission spot is not exactly at I/O pad.

IV. ROOT CAUSE FINDING

Reprocessing of the device has been carried out and SEM analysis is done at each level. Reprocessing has been carried out as shown below to reach the gate level.

A. Removal of polyimide layer

The polyimide layer has been removed using RIE system. Following are the key process parameters used for removal of polyimide layer:

- RF power : 450 W
- Operating pressure : 80 m Torr
- Gas : Oxygen
- Etch time : 25 Minutes

B. Removal of metal (Aluminum)

Metal aluminium has been removed using wet etch with following process parameters:

Chemicals	:	30% HCl
Temperature	:	50 Degree C
Etch Time	:	40 Seconds
Rinse in DI water	:	60 Seconds

C. Removal of BPSG

BPSG Layer has been removed with wet etch. Following are the key process parameters:

Chemicals	:	5% HF
Temperature	:	30 degree C
Etch time	:	25 seconds

SEM analysis is carried out at gate level. Damage at gate level is clearly revealed as shown in Figure 4.

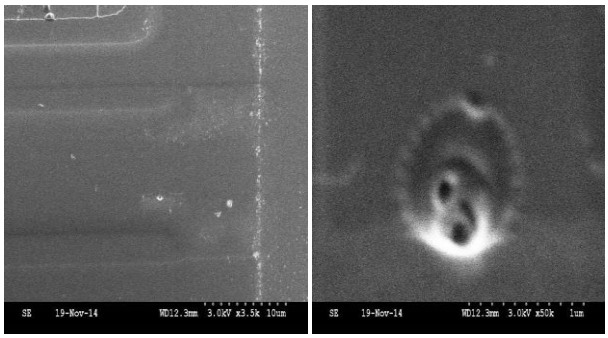

Figure 5: SEM image showing damage at gate level.

The above observation shows that damage at gate level due to ESD stress is responsible for increased leakage current in the device.

V. ESD PROTECTION

In order to improve reliability of devices and the module, ESD protection circuit has been designed as shown in the Figure 5.

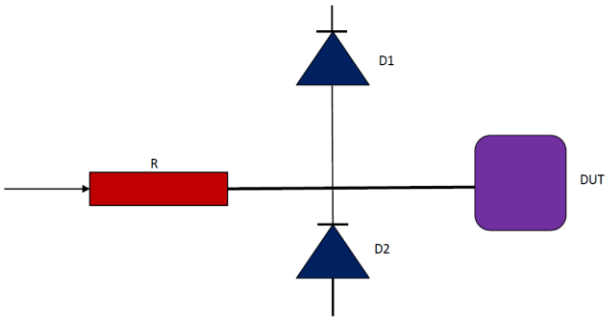

Figure 6: Protection circuit

Device Under Test (DUT) is subjected to ESD stress through the protection circuit. Diodes D1 and D2 play key role in the ESD protection circuit.

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ESD pulse is of the duration 200 nano seconds. Diodes D1 and D2 should be of fast switching type to absorb significant amount of stress energy. Value of R is designed to suit energy dissipation through the protection circuit. In this case D1 and D2 are chosen as 1N 918. Value of 220 ohm is chosen for R. The resistor R is chosen from metal film resistor to have minimum inductance associated with it. Experiments have been conducted to see impact of the protection circuit. The devices were tested using same ESD tester (Electro Tech System, Model: 910) and stress levels were increased up to 5000 Volts.

VI. RESULT

After incorporating the protection circuit, devices have been tested under the same tester. They found to withstand ESD stress till 4500 V. ESD failures have been observed only for stress level of 5000 V and above. The test results are shown in the table given below:

Device Number	ESD Stress Level	Protection Circuit	Acceptable Input Leakage Current	Measured Input Leakage Current
1	1500 V	Absent	1 micro A	7000 to 9650 micro A
2	1500 V	Absent	1 micro A	8000 to 10000 micro A
3	1500 V	Absent	1 micro A	7600 to 10000 micro A
4	2000 V	Present	1 micro A	< 1 micro A
5	2000 V	Present	1 micro A	< 1 micro A
6	2500 V	Present	1 micro A	< 1 micro A
7	3000 V	Present	1 micro A	< 1 micro A
8	3500 V	Present	1 micro A	< 1 micro A
9	4000 V	Present	1 micro A	< 1 micro A
10	4500 V	Present	1 micro A	< 1 micro A
11	5000 V	Present	1 micro A	8000 to 9600 micro A

VII. CONCLUSION

Electrical degradation observed in IC HS – 1840 RH has been traced due to ESD induced failures. The protection circuit designed is found to enhance devices to with stand ESD stress of 4500 V. For space applications, it is not desirable to use external protection circuits. These protection circuit need to be built in during fabrication of IC. Then only one can realize benefits of protection circuits. Methodology for implementation of protection circuits have been suggested to the device manufacturer.

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