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A Fast FPGA based Architecture Implementation for Reversible Image Watermarking

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Abstract: ***Now a day's different techniques are available for digital image watermarking including software and hardware implementation. Reversible contrast mapping (RCM) is one of the technique is used for embed secret information into the digital form. RCM algorithm is simple integer transform of the pixel pair and there LSB bits are used for data embedding. RCM offers high embedding rate, low mathematical calculation and good robustness. This paper focuses on implementation of Field Programmable Gate Array (FPGA) based fast image watermarking using RCM algorithm. The given architecture requires 52 slices, 52 number of flip-flop, 85 number of 4-input LUTs and transceiver data rate is up to 3.2Gbps with an operating crystal frequency is 100MHz. Given architecture is implemented with Xilinx 14.7 on Spartan-6 FPGA family. The given architecture is acceptable for various application areas such as digital cameras, medical and military applications, etc.***

Keywords: Image Processing, RCM, FPGA

I. INTRODUCTION

Digital watermarking is a technique to embed secret information into the digital form is called watermarking. The main purpose is for copyright protection, security, etc. Reversible watermarking is used for lossless data compression and it provide authentication of the original image. And it has most of the used in medical, military applications. Different RW techniques proposed with different type of algorithm and most popular techniques are i) Difference Expansion, ii) Discrete Cosine transform ,iii) Discrete wavelet transform, iv) Histogram bin shifting.[1]

However in this paper RCM-RW implemented technique is used, because of its low computational complexity and robustness. The goal of this proposed design is to achieve high speed hardware efficient VLSI architecture. The RCM algorithm was first implemented in Matlab to analyze the algorithm and various design parameters. After then desired architecture is established in FPGA (Spartan-6) using Xilinx.

II. PREVIOUS WORK

There are several software and hardware implementation algorithm are used a good number of research work is founded by in ICs and systems. Dinu coltue et al. [2] proposed very fast watermarking by RCM algorithm embedding information bit rate is high as compare to spatial Domain and this scheme does not need data compression. Mathematical calculation is also very complex. Gaurav Bhatnagar et al [3] proposed A new adjustable logo watermarking using FRWPT via SVD method. The feasibility of this method and robustness of images with different attacks are tested by computer simulation.

Ranganathan, N et al [4] implemented VLSI architecture for conventional watermarking using special domain algorithm. In hardware implementation inserted two image into original digital image using this technique. The IC chip with 0.35 µm technology implemented and consumes is 6.928mW.

Mohanty et al. [5] another proposed watermarking technique into digital image using DCT domain. The IC chip with 0.35 µm technology and consume power is 62.78 mw.

Maity et al. [6] specify New FWT based spared spectrum watermarking technique that can gives dual purpose verification in data transmission. Prototype design is used Xilinx Spartan-3 FPGA Board operating on 80MHZ frequency.

P Karthigaikumar el at [7] proposed 'Implementation of robust watermarking processor with low power' this technique requires 457 number of slices with low power and it can implemented on ASIC and FPGA both also.

Sugrev kaur et al [8] proposed a high speed low area FPGA implementation using DWT based image watermarking algorithm. It requires the 4708 slices and it work at 344MHZ frequency.

Hirak maity et al. [9] proposed FPGA based VLSI architecture for digital image using RCM algorithm' They proposed two architecture of block size 8x8 and block size 32x32, architecture required 9881 slices, 11291 number of 4-input LUTs,1.0395Mbps data rate and operating frequency 98.76MHz.

Sudip Ghosh et al. [10] proposed another RCM algorithm for Reversible watermarking scheme based on FPGA. The architecture is encoder and decoder based design for faster implementation, encoder required 528 4-input LUTs and 303 slice and decoder required 613 LUTs 347 slices with max clock frequency of decoder is 45MHz.

III. RCM-RW ALGORITHM

Let [0 L] be the gray image with image pixel intensity value between [0 255] Let [X,Y] be a pixel pair. The forward transform pixel pair is defined asX' = 2X-Y, Y'=2Y-X.The transform is to a sub domain DC⊂99[0, L] × [0, L] and it is noted as equations $0 \le (2x - y) \le 255$ and $0 \le (2y - x) \le 255$. Dc coefficient is the rhombic shape with its diagonals [0, L] × [0, L] is shown in fig 1. [9]

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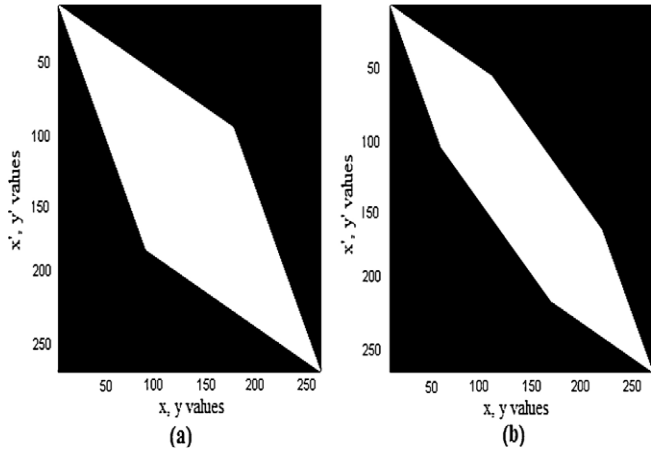

Fig 1.Transform domain D (a) without DCcoefficient and (b) with DC coefficient.

A. Image Watermark embedding

In RCM algorithm the original image is partitioned into 8x8 image block. Then each image block is partition into pixels pair and watermark bit is embeded into LSBs of transform pixels pairs which is (X' Y') where X' indicates pixel pair is transformed or not and Y' indicate watermark inserting. The flow diagram of embedding watermark is shown in fig 2.

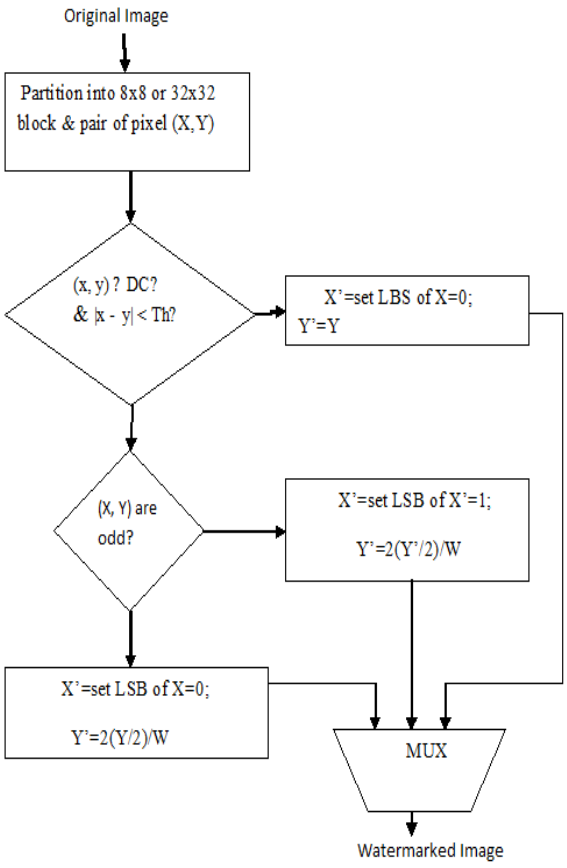

Fig 2 The Flow diagram of watermark embedding

B. Image Watermark extraction

Inverse transform is applied for watermark extraction. Watermarked image is again partitioned into 8x8 image block and pixel pair then checks two object conditions. The process is repeated again and again until covers all pixel pairs. The flow diagram of image extraction watermark is shown in fig 3.

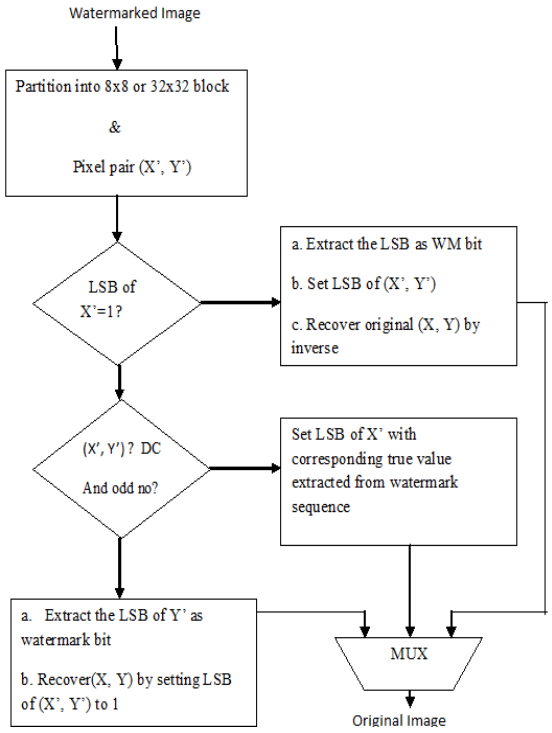

Fig 3.The flow diagram of watermark extraction

IV. VLSI ARCHTECTURE OF RCM

Implementation of the watermarking algorithm is done using the ISE Design suite of Xilinx 14.7 for Spartan 6FPGA family. FPGA because of its advantages like Reconfigurability, low cost, high speed & simpler design process is used for hardware implementation. Security level offered by the hardware based watermarking techniques is higher than the software based watermarking techniques. Watermark embedding and watermark extraction of original image is done through the RCM algorithm.

V. PROTOTYPE DESIGN OF FPGA

This design unit consist the two main parts one is watermark embedding and other is watermark extraction. Each part have separate functional block, Mux, address decoder, flip-flop, memory shift register etc. These blocks are tested and verified through Xilinx simulation. Once all parts are tested and verified, the different modules are connected in series together according to controller instructions.

A. FPGA architecture for image watermark embedding part

In watermark embedding part consist image partitioning unit, comparator unit memory unit. The original image and watermark image are received and stored in SBUF. Then original image with size 8x8 and watermark image with size 8x8 blocks are converted into the integer form (bits). Watermark embedding process is done, this is compression technique again the integer form is converted into (8x8) image block set and transmitted to PC. Experimental results are obtained on Matlab,

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For the data reading and writing purpose clock signal is required, here address decoder is used for generate clock. The block diagram of hardware architecture for image watermark embedding part is shown in fig 4.

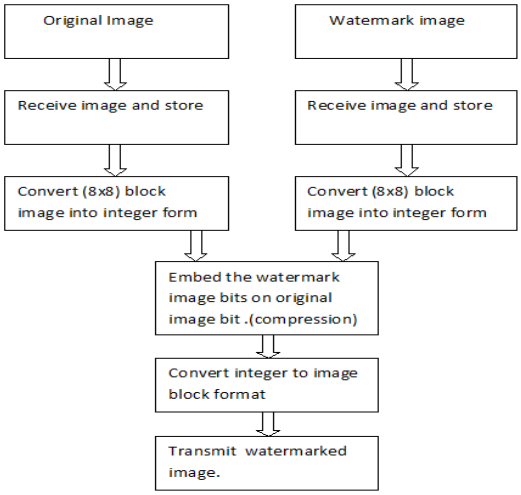

Fig 4. Block diagram of hardware architecture of image watermark embedding part.

B. FPGA architecture for image watermark extraction unit:

In watermark extraction unit is similar to watermark embedding unit. Here watermarked image is received and stored in SBUF And Converted size of 8x8 image block into integer form (bits) and applied inverse transform. After then again converted integer form to 8x8 image block, and is transmitted to PC. Result obtained two extracted images one is watermark image and other is original image. The block diagram of hardware architecture for image watermark extraction part is shown in fig 6.

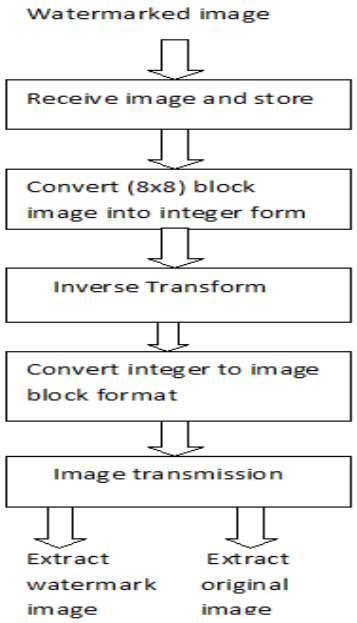

Fig 5. Block diagram of hardware architecture of image watermark extraction part.

VI. EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed technique is tested and verified on different images. Original image (Lena) with size 128x128 and watermark image (Beam) with size 64x64 applied proposed algorithm on this images and resulted watermarked image (embedding) is shown in fig 10. Again apply the inverse transform of the proposed algorithm extracted image is shown in fig 11. Proposed scheme is evaluated using objective parameters such as Peak Signal to noise ratio (PSNR), Mean square error (MSE) and structural similarity index measure (SSIM) for checked quality of image. Watermarked image is obtained after embedding bit rate is 0.45bpp.

Fig 6. Original Image

Fig 7. B plane Image

Fig 8. Watermark image

Fig 9. B Plane Image

Fig 10. Watermarked Image

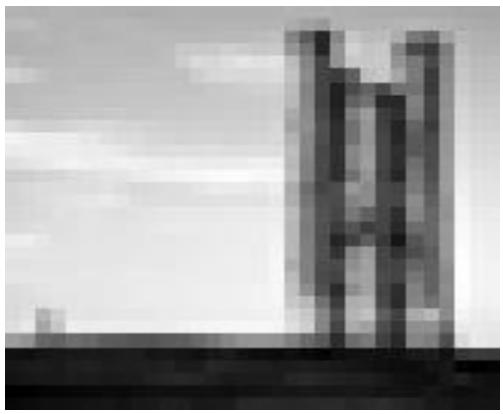

Fig 11. Extracted Image

Table no. 1

Image	PSNR(dB)	MSE	SSIM
Lena	30.16	30.08	0.89
Beam	30.34	30.04	0.87

To find out the robustness of image using proposed method, the watermarked image and extracted image is modified by different attacks like Median filter, standard deviation filter, average filter, motion blur, sharpen, disk blurred and salt & pepper. [4] Correlation Coefficient of experimental images is given table no 2.

Table no 2.

Attacks	Lena	Football	Beam	Fabric
Median filter	0.9961	0.9977	0.9986	0.9868
Standard deviation filter	0.1746	0.4220	0.3410	0.3800
Average filter	0.8669	0.8159	0.8376	0.8199
Motion blur	0.9531	0.9705	0.9372	0.7401
Salt& pepper	0.9242	0.8707	0.9846	0.9235
Disk blurred	0.9299	0.9604	0.9257	0.6707
Sharpened	0.9565	0.9757	0.9152	0.8982

Correlation Coefficient of Watermarked image & Extracted image is given in table no 3.

Table no 3.

Attacks	Watermarked Image	Extracted Image
Median filter	0.9616	0.9993
Standard deviation filter	0.1924	0.0919
Average filter	0.8104	0.8561
Motion blur	0.8604	0.9749
Salt& pepper	0.9044	0.9044
Disk blurred	0.8348	0.8348
Sharpened	0.9149	0.9149

The Synthesis watermark embedding & extraction is done on Xilinx (ISE version 14.7) spratan-6 (XC6SLX45) FPGA family. The device is used for implementation using VHDL language. The power required for this device is low and it is calculated through Xilinx 14.7, which is near about 0.91mw and operating frequency is used of this system is 25MHz.The synthesis results and device utilization summary is given in table no 4.

Table no 4.

Logic device Utilization	Used no of device	Total Available device	Utilization factor
Total no of slices	52	54576	1%
Total Number of Slice Flip Flops	52	54576	1%
Total Number of 4 input LUTs	85	27288	1%
Total Number of Bonded IOBs	12	208	5%
Total Number of MUXCYs used	24	13644	1

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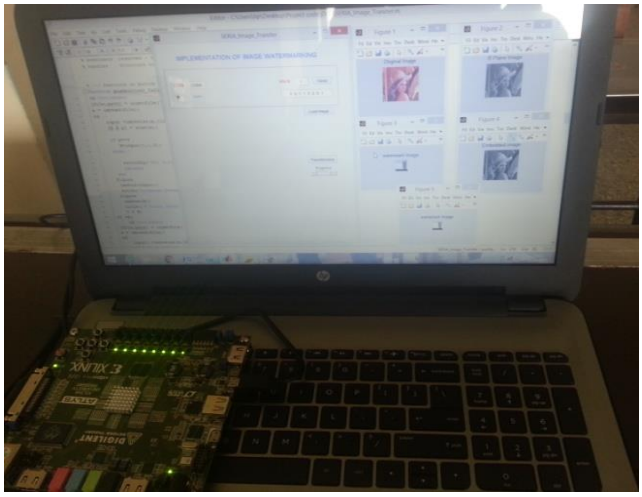

Fig. 12 Hardware Implementation

VII. CONCLUSION

This paper focuses on a fast FPGA based image watermarking using RCM algorithm. Because of its low computational complexity, simplicity and easily implemented on hardware. Implementation on hardware is very simple, fast and it required less number resources only 52 no. of slices, 52 no. of flip flops and 85 4-input LUTs and transceiver data rate up to 3.2Gbps with operating 100MHz crystal frequency. The proposed architecture is acceptable for various application areas such as digital cameras, medical and military applications, etc.

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