Design and Hardware Implementation of Sun Sensor based Sun Re-Acquisition on Safe Mode Detection in Satellites

Dhanyashree T S, Sangeetha B G, Gayatri Malhotra

Abstract— Satellite/spacecraft enter into Safe Mode in case of contingency when the solar panel is not rotated towards Sun in order to provide full solar array power. The transition from safe mode to sun pointing mode, carried out automatically by Sun acquisition logic. In sun acquisition logic selected yaw and roll errors are used as inputs to controller whose outputs are routed to thruster selection logic. On Safe Mode enable condition, based on the safe mode pulse from on board computer (OBC) thruster block reconfiguration is done. This initiates thruster selection logic (TSL), whose outputs are routed to thruster drivers to fire the thrusters in satellites/spacecraft to change the spacecraft orientation. The eclipse condition is also detected from 4PI pitch output on safe mode.

Index Terms— Pitch, yaw, roll, safe mode detection, loop-on pulse generation, long pulse detection, thruster selection, sun pointing mode.

I. INTRODUCTION

An essential part of all satellites is an onboard computer system to control and monitor the different systems [1]. The purpose of On Board Computer (OBC) system is to integrate and miniaturize Spacecraft Electronics to match the global trend and meet the requirements of Autonomous spacecraft operations. Cost-effective spacecraft engineering is achieved by integrating the various elements of the spacecraft bus that realize the functions of command processing, Data acquisition and processing, Attitude and Orbit control, Telemetry and Housekeeping and Thermal Management into a single OBC. The MIL STD 1553B protocol is used for interfacing with various sub-systems of the spacecraft. The OBC interfaces with sensors (attitude and temperature), actuators, power, thermal control elements like heaters and Solar Array Drive Assembly through special interfaces, TTC (RF) for command and housekeeping TM[2][3]. For all these operations a functionally redundant OBC is present. In case of failure or contingency in main and redundant OBC, a separate package is configured, which houses 4Pi Sun Sensor based Hardware based Safe Mode detection and Sun Acquisition and Contingency Telemetry logics. This paper describes the implementation of this package on a FPGA. The design implemented is synthesized and tested for various values of 4Pi sun sensor's output voltages given, where results show the detection of safe mode and thruster controls for sun acquisition.

The organization of the paper is as follows: Section II presents design methodology of safe mode detection and sun acquisition. Section III briefs the hardware implementation which consists of review of use of FPGA and testbed setup along with testing steps. Section IV presents our results validating the correct working of our design. Section V is of conclusion and future work.

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II. METHODOLOGY

A. Terminology

Safe mode is an operating mode of a modern spacecraft during which all non-essential systems such as science instruments are shut down and only essential functions such as thermal management, radio reception and attitude control are active. Safe mode is entered automatically upon the detection of sun absence. The spacecraft attempts to maintain orientation with respect to the Sun for illumination of solar panels and for thermal management. The spacecraft then awaits radio commands from its mission control center monitoring for signals on its low-gain omnidirectional antenna[4].

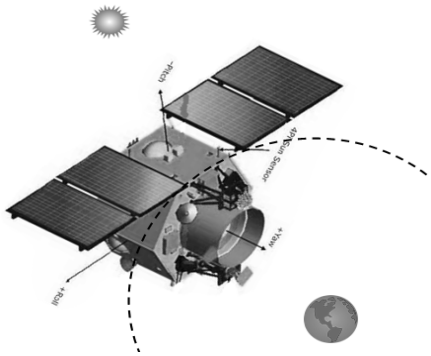

Fig 1. Satellite's position w.r.t.to the Earth and the Sun

This system uses coordinates that maintain their orientation relative to the earth as spacecraft moves in orbit. These coordinates are known as roll, pitch, and yaw or RPY, and are illustrated in figure 1. In this system, the yaw axis is directed toward the nadir (i.e., toward the center of the Earth), the pitch axis is directed toward the negative orbit normal, and the roll axis is perpendicular to the other. Thus, in a circular orbit, the roll axis will be along the velocity vector[6].

B. Implementation overview

Safe mode detection, Sun acquisition and telemetry

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interfacing are the three basic logics designed and implemented as shown in figure 2. Safe mode detection logic produces safe mode initiation status. After which thrusters are controlled by sun acquisition logic. The status of the signals used and manipulated in these two logics is sent to telemetry(TM) subsystem after interfacing with TM interface logic.

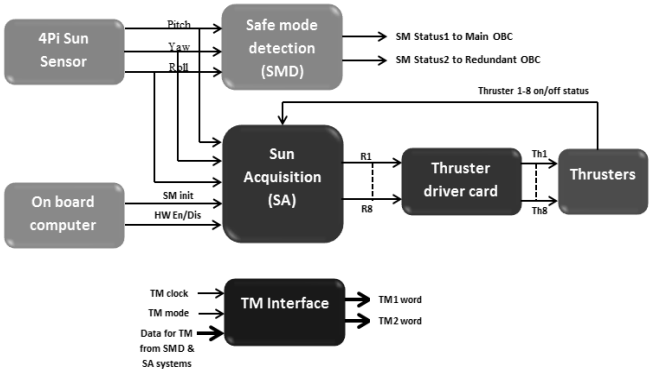

Fig 2. Package overview

C. *Safe mode detection*

Safe mode detection logic shown in figure 3 is based on 4Pi sun sensors pitch, yaw and roll signals errors. Selected sensor outputs are compared with respect to threshold set to detect errors in sensors signals. The Sun will be on negative pitch axis, when the solar panels are normal to the Sun. The 4pi pitch output magnitude will be high when the Sun is directly looking at the pitch cells. So when the Sun is on negative pitch side, the pitch output will be -5.0 volts that is high in magnitude[5].

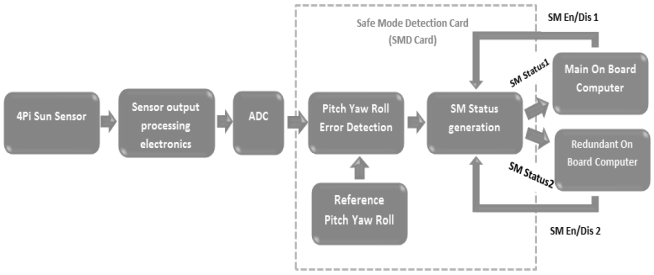

Fig 3. Safe Mode Detection System

The presence of error is verified by the following conditions.

1. If 4pi pitch output greater than the threshold (for example, 1.5 volts is greater than 1.0 volts). This check is to say that the Sun is away from the body negative pitch axis.
2. If absolute values of 4pi yaw or roll outputs (magnitudes alone) are beyond certain threshold (say, 1.5 volts). This check is to ensure that the Sun is beyond the cone of 45° about the negative pitch axis.

The second condition supports the 4pi pitch output checking. The check also supports logic validity during eclipse. Checking could have been either yaw or roll, but checking together may be more robust.

D. *Sun Acquisition*

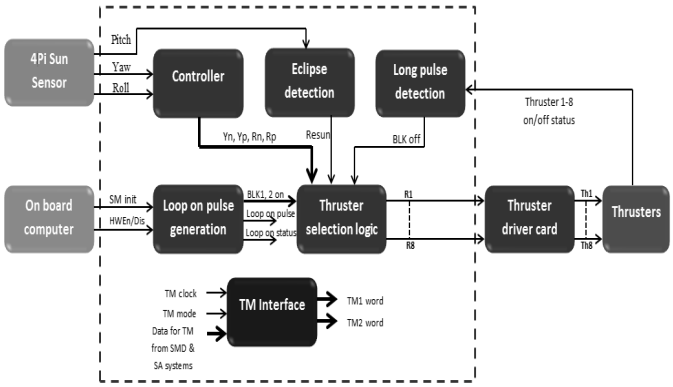

Fig 4. Sun Acquisition system

In sun acquisition logic selected pitch, yaw and roll errors are used as inputs to controller whose outputs are routed to thruster selection logic. The sun acquisition system is shown in figure 4.

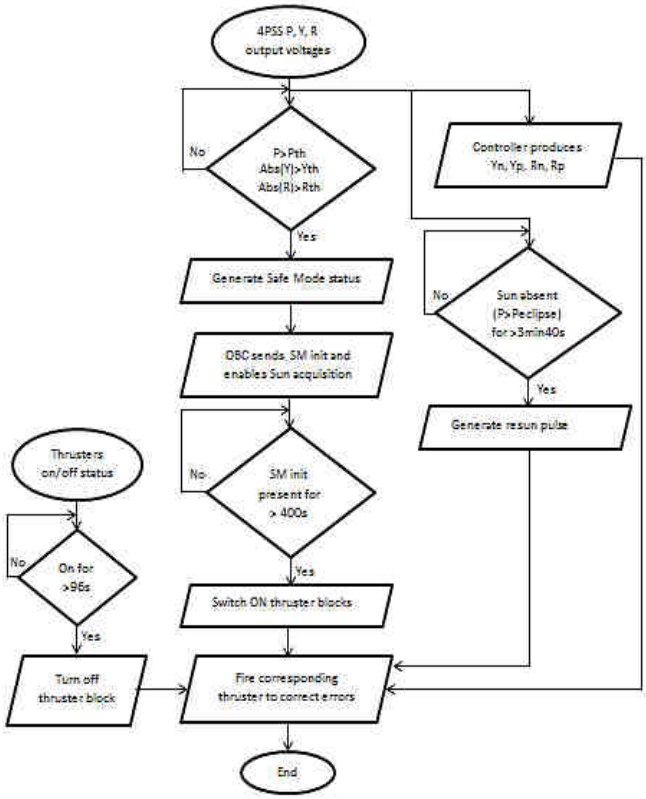

Fig 5. Flowchart depicting the operation in Safe mode detection and Sun acquisition logics

On Safe Mode enable condition, the SM pulse from OBC initiates a 400sec timer whose outputs do thruster block reconfiguration. Thruster selection logic (TSL) is initiated after obtaining assertions from block reconfiguration logic. The TSL outputs are routed to thruster drivers. The thruster outputs in turn change the spacecraft orientation. The sensor data will sense it and controller (closed loop) will change the thruster firing duration accordingly. The eclipse condition is detected from 4PI pitch on safe mode condition. If eclipse is detected, sun acquisition is initiated on end of eclipse. The duration of eclipse is based on mission / orbit. Long pulse

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detection logic makes thrusters block off, if any of the thrusters is firing for more than 96 sec. The flow diagram depicting the operation sequence of safe mode detection and sun acquisition is shown in figure 5.

E. TM Interface

When in Safe mode, the satellites rejects on-board stored commands and relies on the ground for the transition back to normal mode. To support ground investigation and recovery actions, the observability is ensured through telemetry, which provides sensors acquisition data, status of essential signals of safe mode detection and sun acquisition logics.

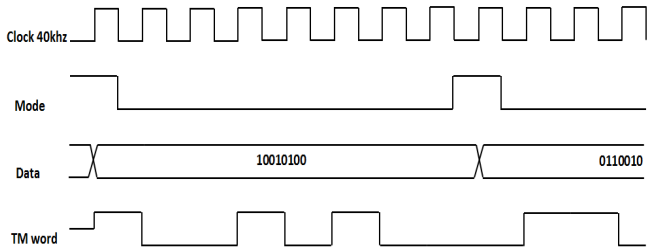

Fig 6. TM interface operational seguence

The TM word to be sent is provided by TM interface logic. The operational sequence of this logic is represented in figure 6. The clock rate at which TM interface is done is 40Khz. With the telemetry mode pulse, status of signals is latched into an 8 bit register and is serially interfaced to TM subsystem.

III. HARDWARE IMPLEMENTATION

A. FPGA Implementation

FPGA (Field Programmable Gate Array) is a programmable logic device where the user can configure the hardware in the chip to perform many logical functions. The cost of FPGA- based design is much cheaper than ASIC design (provided we are not talking about large production in millions of units). The time to market is also much faster for FPGA-based design. These factors combined with the ease of re-configurability made FPGA-based design a very attractive solution for design that are not manufactured in very large numbers, and that is certainly the case for satellite hardware sun acquisition.

In satellite control FPGA-based systems are widely used since the market is very small (compared to consumer electronics for example) and small reconfigurable systems saves a lot of weight and power consumptions which are very important criteria for satellite depending on solar panels for power and very limited space and weight requirement.

B. Testing

The design is implemented using Spartan family FPGA. Xilinx ISE design suite software tool is used for synthesis on FPGA and analysis of HDL designs. For testing purpose the outputs of 4Pi sun sensor are provided using voltage sources. These analog outputs are fed to ADC to get the digitized values before inputting to FPGA. ADC used for testing purpose is of Analog device's AD7891 family ADC. Possible range of pitch, yaw and roll voltages are fed to verify the correctness of design. The signals from OBC to be used in the design are given externally by a voltage source for testing through buffer card to the FPGA. After processing inputs from ADC and buffer card, the outputs from FPGA are taken through buffer card are given to digital oscilloscope to view the outputs.

IV. RESULTS

The Safe mode detection and Sun acquisition logic is designed using VHDL code and is synthesized on Spartan family FPGA[7][8]. The synthesized design is simulated for different test cases. The design coded using editor in Xilinx ISE design suite is simulated using the Xilinx ISE simulator (version 12.1). The results of the simulation are shown in the waveform.

Results of Safe Mode Detection logic is shown in figure 7. For given pitch, yaw and roll voltage, as the error is present, the design detects the error and safe mode is initiated by SM Status signal transition from low to high logic. This shows that SM detection logic detects the sun absence.

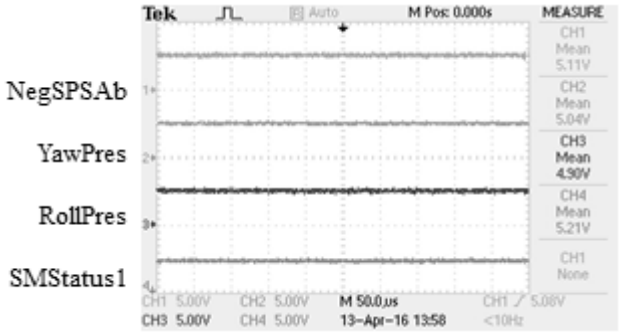

Fig 7. Result of safe mode detection logic

Figure 8 show the loop on pulse and status generated for the test values. The results show whether the thruster blocks will be turned on or off with the BLK on signals. Loop On Status=1, as SMinit and HW_PWPFM_En is high (5V) for more than 400s, BLK1_on=1, as BLK1_2sel is 0V.

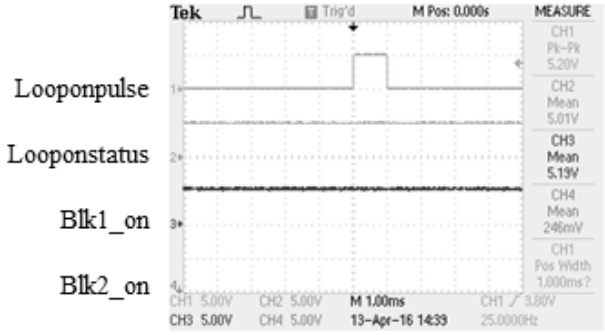

Fig 8. Results of Loop on pulse generation logic

As one of the thruster statuses is held high for more than 96s for testing purpose, the BLK off pulse is generated, as seen on results of long pulse detection in figure 9.

Figure 10a shows the outputs of thruster selection logic, where firing pulses are continuously given to thruster 4, based on the yp, yn, rp, rn signals. Pulse width increase and thruster 3 turning on along with thruster 4 can be seen when resun pulse is generated detecting eclipse in figure 10b.

Result of TM interface logic is shown in figure 11, where the operational sequence is generated and TM data words are serially transmitted.

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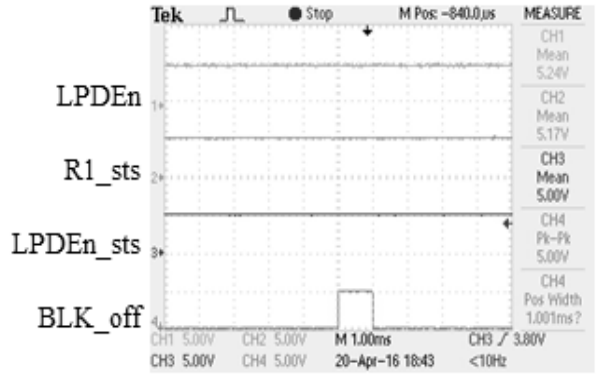

Fig 9. Results of long pulse detection logic

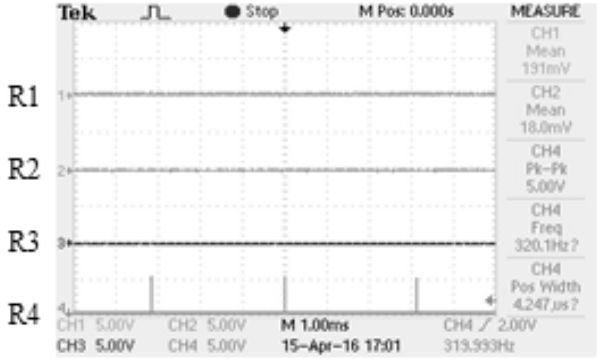

Fig 10a. When yp=rp=1, then thruster R4 is made ON by generating 3us pulses

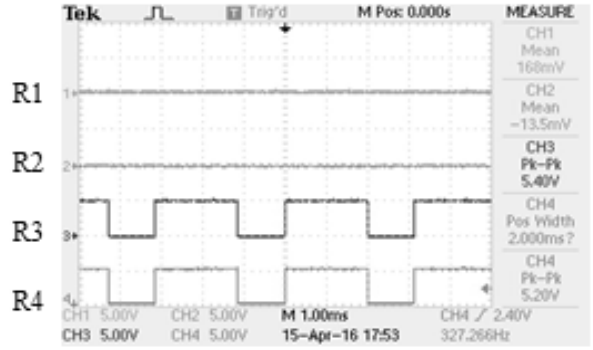

Fig 10b. When resun=1, then thruster R3 & R4 are made ON by generating 2ms pulses

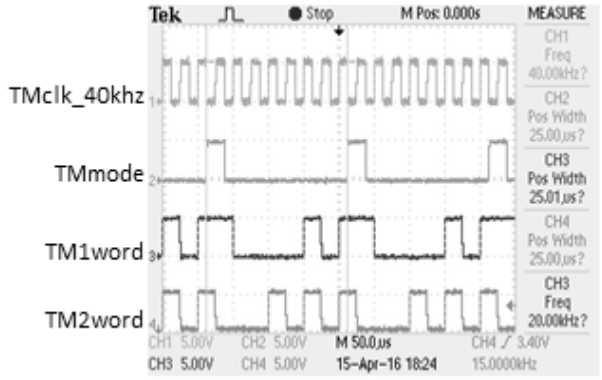

Fig 11. TM interface logic result

V. CONCLUSION

Through this work, the architecture and function of the package consisting safe mode detection, Sun acquisition and TM interfacing, have been implemented on FPGA. Safe mode is detected based on the 4Pi sun sensor outputs, which indicates the loss of sun presence. This is followed by transition, from safe mode to sun pointing mode, carried out by sun acquisition logic which controls thrusters to orient solar arrays to point to sun. The scope of the future development is since the design is implemented using VHDL code, it is easy to add new features and design is target independent. The design can be targeted on to any family of FPGA/ASIC.

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