Analysis and Study of V-I Characteristics by Replacing Low-K Dielectric (HfO$_2$) with High-K Dielectric (La$_2$O$_3$) in MOSFET

Anurekha Mukherjee, Sohini Mondal

Abstract—This project journal paper presents the analysis and study of Lanthanum oxide La$_2$O$_3$, one of the promising high-k dielectric films used in the MOSFET over hafnium dioxide, HfO$_2$. Capacitance-Voltage measurements were carried out to investigate properties such as oxide charges and interface trap charges that exist in the dielectric La$_2$O$_3$, an inorganic compound containing the rare earth element lanthanum and oxygen. The investigation has been carried out by experiment and modeling. With the advent of semiconductor technology in VLSI era, the channel length of a metal oxide semiconductor has drastically gone down. DIBL (Drain Induced Barrier Lowering) is one of the short channel effects which degrade the performance of a MOSFET with its down scaling. To understand this effect the study of the nature of surface potential and energy is very important. In this project an analytical model for threshold voltage of short channel MOSFETs is presented. For such devices, the depletion regions due to source/drain junctions occupy a large portion of the channel, and hence are very important for accurate modeling. The proposed threshold voltage model is based on a realistic physically – based model for the depletion layer depth along the channel that takes into account its variation due to the source and drain junctions. With this, the unrealistic assumption of a constant depletion layer depth has been removed, resulting in an accurate prediction of the threshold voltage. The graphs between different parameters of HfO$_2$ and La$_2$O$_3$ are verified against the simulator MATLAB and the comparative analysis of the features of the graph of both the oxides has been done.

Index Terms—Channel Length, DIBL, Pocket doping, Threshold Voltage

I. INTRODUCTION

Demand for larger scale integration of MOS circuits on a single chip urged of miniaturization of MOS devices. As the channel length shrinks, many short-channel effects were observed mainly reduction of threshold voltage, increased off-state leakage current and Drain-induced barrier lowering. Charge sharing model have been used to model the short-channel effects (SCEs). The charge sharing model assumptions of constant surface potential and no divergence of electric field lines in the gate oxide are invalid for high drain and substrate biases. On the other hand, two-dimensional analysis has accurately predicted the values of threshold voltage of short channel MOSFET’s and breakdown voltage. We have derived the analytical relations for surface potential, threshold voltage and longitudinal field. Without any assumption, we have proposed a model for short channel factor which shows the dependence on the channel width and drain voltage. The effect of charge carrier density is to raise the threshold voltage of submicron devices operating at any drain voltage. It is observed from our analysis that short-channel effect is more dominant in the submicron devices with thinner gate oxide. Our study also predicts that SCE in short channel device is more effective in presence of charge carrier density. It is also observed that the short channel factor shows a weak dependence on the substrate doping due to the inclusion of carrier charge density.

The continuing miniaturization of feature sizes in integrated circuits (ICs) has led to improvement of device performance and higher packing densities. The aim of scaling is to reduce total size and to increase overall functional density. As the channel length shrinks, many short-channel effects are introduced. The short channel effect can be reduced or can be reversed (reverse short channel effect; RSCE), by locally raising the channel doping near source and drain junctions. Not only this but also using La$_2$O$_3$ (a high K dielectric) instead of HfO$_2$ is done for allowing further miniaturization.

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion layer widths of the source and drain junction. As the channel length is reduced to increase both the operation speed and the number of components per chip, the so-called short channel effects arise. So, the objectives of the project is to find out the threshold voltages for different channel lengths by constructing a threshold voltage shifting profile and observing the changes in current and threshold voltage by reducing the thickness of the insulating layer.

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Analysis And Study of V-I Characteristics by Replacing Low-K Dielectric (SiO$_2$) With High-K Dielectric (La$_2$O$_3$) in MOSFET

A. Figures

Vth vs L Graphs for HfO$_2$ & La$_2$O$_3$ Without Varying Pocket Doping

Threshold Voltage(Vth) versus L graphs For HfO$_2$ & La$_2$O$_3$, By Varying Pocket Doping
Graph Between $\text{La}_2\text{O}_3$ And $\text{HfO}_2$:

Fig 5. $I_d$ vs $t_{ox}$ For (HfO$_2$)

Fig 6. $I_d$ vs $t_{ox}$ For (La$_2$O$_3$)

Graph Between $I_d$ versus $t_{ox}$ Graph For La$_2$O$_3$ And HfO$_2$:

Fig 7. $V_t$ vs $t_{ox}$ For (HfO$_2$)

Fig 8. $V_t$ vs $t_{ox}$ For (La$_2$O$_3$)
Analysis And Study of V-I Characteristics by Replacing Low-K Dielectric (SiO₂) With High-K Dielectric (La₂O₃) in MOSFET

B. Figures and Tables

Vth vs L Graphs for HfO₂ and La₂O₃ without Varying Pocket Doping

Table 1. Comparison of Vth vs L Graph for HfO₂ and La₂O₃ without Varying Pocket Doping

<table>
<thead>
<tr>
<th>Channel Length (L in μm)</th>
<th>Vt(V)</th>
<th>ΔVto</th>
<th>Vth=Vt-ΔVto</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0.0219</td>
<td>0.0165</td>
<td>0.005159</td>
</tr>
<tr>
<td>0.7</td>
<td>0.0220</td>
<td>0.0191</td>
<td>0.0029</td>
</tr>
<tr>
<td>0.6</td>
<td>0.0222</td>
<td>0.0223</td>
<td>-0.00004</td>
</tr>
<tr>
<td>0.5</td>
<td>0.0225</td>
<td>0.0268</td>
<td>-0.0042</td>
</tr>
<tr>
<td>0.4</td>
<td>0.0229</td>
<td>0.0335</td>
<td>-0.0105</td>
</tr>
<tr>
<td>0.35</td>
<td>0.0232</td>
<td>0.0382</td>
<td>-0.0150</td>
</tr>
<tr>
<td>0.3</td>
<td>0.0236</td>
<td>0.04666</td>
<td>-0.02105</td>
</tr>
<tr>
<td>0.2</td>
<td>0.0249</td>
<td>0.067</td>
<td>-0.042091</td>
</tr>
<tr>
<td>0.1</td>
<td>0.0285</td>
<td>0.134</td>
<td>-0.1054</td>
</tr>
</tbody>
</table>

Table 2. Threshold voltage values for different Channel length (HfO₂) By Varying the Pocket Doping

<table>
<thead>
<tr>
<th>Channel Length (L in μm)</th>
<th>Vt(V)</th>
<th>ΔVto(V)</th>
<th>Vth=Vt-ΔVto</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0.7779</td>
<td>0.01353</td>
<td>0.7643</td>
</tr>
<tr>
<td>0.7</td>
<td>0.7832</td>
<td>0.01547</td>
<td>0.7677</td>
</tr>
<tr>
<td>0.6</td>
<td>0.7903</td>
<td>0.01805</td>
<td>0.7723</td>
</tr>
<tr>
<td>0.5</td>
<td>0.8002</td>
<td>0.02166</td>
<td>0.7785</td>
</tr>
<tr>
<td>0.4</td>
<td>0.8150</td>
<td>0.0270</td>
<td>0.7879</td>
</tr>
<tr>
<td>0.35</td>
<td>0.8254</td>
<td>0.03094</td>
<td>0.7944</td>
</tr>
<tr>
<td>0.3</td>
<td>0.8391</td>
<td>0.0361</td>
<td>0.80306</td>
</tr>
</tbody>
</table>

Table 3. Threshold voltage values for different Channel length (La₂O₃) By Varying the Pocket Doping

<table>
<thead>
<tr>
<th>Channel Length (L in μm)</th>
<th>Vt(V)</th>
<th>ΔVto(V)</th>
<th>Vth=Vt-ΔVto</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0.7779</td>
<td>0.01353</td>
<td>0.7643</td>
</tr>
<tr>
<td>0.7</td>
<td>0.7832</td>
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<tr>
<td>0.3</td>
<td>0.8391</td>
<td>0.0361</td>
<td>0.80306</td>
</tr>
</tbody>
</table>

As the dielectric constant is more than SiO₂ (i.e. 19.6) therefore the threshold voltage reduces more as compared to SiO₂ for shorter channel lengths and hence DIBL effect reduces to a greater extent as compared to SiO₂.

The dielectric constant for La₂O₃ is 27 which is more as compared to SiO₂ and HfO₂ therefore the DIBL effect reduces more as compared to SiO₂ and HfO₂ for shorter channel length the threshold voltage reduces to a greater extent.

Off state leakage current is decreased to a greater extent because the dielectric constant is more as compared to SiO₂. Thus charge sharing effect between source, drain region and channel (DIBL) effect is reduced as compared to SiO₂.

The dielectric constant is more for La₂O₃ as compared to SiO₂ and HfO₂ due to which charge sharing effect between drain, source and Channel (DIBL) reduces to a greater extent.
Table 4. Comparison of Vth vs L Graph Varying Pocket Doping for HfO$_2$ and La$_2$O$_3$

<table>
<thead>
<tr>
<th></th>
<th>HfO$_2$</th>
<th>La$_2$O$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Length till</td>
<td>0.44um</td>
<td>0.1um</td>
</tr>
</tbody>
</table>

Threshold Voltage versus channel length graphs of HfO$_2$ & La$_2$O$_3$ By Varying Pocket Doping

Fig 3. Vth vs L (HfO$_2$) Varying Pocket Doping

Fig 4. Vth vs L For La$_2$O$_3$

Fig 5. Id vs tox (HfO$_2$)

Fig 6. Id vs tox (La$_2$O$_3$)
Analysis And Study of V-I Characteristics by Replacing Low-K Dielectric (SiO$_2$) With High-K Dielectric (La$_2$O$_3$) in MOSFET

Table 5. Comparison of Id vs tox Graphs for HfO$_2$ & La$_2$O$_3$

<table>
<thead>
<tr>
<th>HfO$_2$</th>
<th>La$_2$O$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>As $C = \frac{K \varepsilon_0 A}{d}$ and the value of the dielectric constant is more for HfO$_2$ as compared to SiO$_2$ therefore, the capacitance increases more for HfO$_2$ and the drain current increases more as compared to silicon dioxide. As the value of the dielectric constant is more as compared to La$_2$O$_3$, so the drain current is less hence the mobility of the electrons to reach from source to drain decreases and device current increases.</td>
<td>Value of the dielectric constant is more as compared to HfO$_2$, so the drain current is less hence the mobility of the electrons to reach from source to drain decreases and drain current increases.</td>
</tr>
</tbody>
</table>

Lesser gate voltage is required for the formation of the channel as compared to HfO$_2$. Thus, oppositely charged ions are induced and the channel formation takes place more easily as the dielectric constant value is more for HfO$_2$. Less gate voltage is required for the formation of the channel and for less gate voltage, more opposite charges are induced and the channel formation is done more easily.

Vt versus tox Graph For La$_2$O$_3$ And HfO$_2$:

Table 6. Comparison of Vth vs tox Graph for HfO$_2$ & La$_2$O$_3$

<table>
<thead>
<tr>
<th>HfO$_2$</th>
<th>La$_2$O$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage is reduced to a greater extent as compared to HfO$_2$. Thus, oppositely charged ions are induced and the channel formation is done more easily.</td>
<td>Oxide capacitance is more as compared to La$_2$O$_3$, hence the on-state current is less and device speed is less as compared to HfO$_2$.</td>
</tr>
</tbody>
</table>

C. Equations

Numerical Analysis For Plotting The Variation Of The Threshold Voltage $V_T$ As A Function Of The Channel Length:

Expression of the Threshold voltage For La$_2$O$_3$:

$$V_{TO} = \Phi_{GC} - 2\Phi_F (\text{sub}) - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}}$$

Calculation of $\Phi_{GC}$:

$$\Phi_{GC} = \Phi_F (\text{sub}) - \Phi_F (\text{gate}) = -0.35\text{V} - 0.55\text{V}$$

Calculation of depletion region charge:

$$Q_{BO} = \sqrt{2q\varepsilon_{La}N_d |2\Phi_F|}$$

$$Q_{BO} = \sqrt{2 \times 1.6 \times 10^{-19} \times 1.5 \times 10^{13} \times 27 \times 8.85 \times 10^{-14} \times 2 \times 0.3}$$

$$Q_{BO} = -0.25242 \times 10^{-8} \text{C/cm}^2$$

The oxide-interface charge is:

$$Q_{OX} = qN_{ox} = 1.6 \times 10^{-19} \times 4 \times 10^8 = 6.4 \times 10^{-11} \text{C/cm}^2$$

The oxide capacitance is given by:

We can combine all the components and calculate the threshold voltage:

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The oxide capacitance is given by:

\[ C_{OX} = \frac{e_{ox}}{t_{ox}} = \frac{27 \times 8.85 \times 10^{-14}}{2.5 \times 10^{-4}} = 0.693 \times 10^{-8} \text{ F/cm} \]

The threshold voltage can be calculated as:

\[ V_{TO} = \Phi_{GC} - 2\Phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} \]

\[ Q_{BO} = -0.262 \times 10^{-8} \]

\[ Q_{OX} = 6.6959 \times 10^{-3} \]

\[ V_{TO} = 0.0674V \]

The source and drain junction built-in voltage is:

\[ \Phi_o = \frac{KT}{q} \ln \frac{N_A N_D}{n_i^2} = 0.026 \ln \frac{10^{33}}{2.304 \times 10^{21}} = 0.6967V \]

The source and drain junction built-in voltage is:

\[ \Phi_o = \frac{KT}{q} \ln \frac{N_A N_D}{n_i^2} = 0.026 \ln \frac{10^{34}}{2.304 \times 10^{21}} = 0.7565V \]

The oxide-interface charge is:

\[ Q_{OX} = qN_{ox} = 1.6 \times 10^{-19} \times 4 \times 10^8 = 6.4 \times 10^{-11} \text{ C/cm}^2 \]

**Pocket Implant or Pocket Dose:**

The pocket implantation, which causes the RSCE, is done by adding impurity atoms both from the source and drain edges. It is assumed that the peak pocket doping concentration \( N_{p} \) gradually decreases linearly towards the substrate level concentration \( N_{ox} \) with a pocket length \( L_{p} \) from both the source and drain edges. The basis of the model of the pocket is to assume two laterally linear doping profiles from both the source and drain edges across the channel.

**Depths of source and drain junction depletion region can be found as:**

\[ X_{sd} = X_{ds} = \sqrt{\frac{2e_{ox} \Phi_o}{qN_A}} = 0.1177 \times 10^{-4} \text{ cm} \]

**Depths of source and drain junction depletion region can be found as:**

\[ X_{sd} = X_{ds} = \sqrt{\frac{2e_{ox} \Phi_o}{qN_A}} = 0.1057 \times 10^{-4} \text{ cm} \]

**Expression of the Threshold voltage For HfO2:**

\[ V_{TO} = \Phi_{GC} - 2\Phi_F (sub) - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} \]

**Calculation of \( \Phi_{GC} \):**

\[ \Phi_{GC} = \Phi_F (sub) \times \Phi_F (gate) = -0.35V \times 0.55V = -0.19V \]

**Calculation of depletion region charge:**

\[ Q_{BO} = \sqrt{2e_{ox} N_A 2\Phi_F} \]

\[ = \sqrt{2 \times 1.6 \times 10^{-19} \times 1.5 \times 10^{13} \times 25 \times 8.85 \times 10^{-14}} \]

\[ = -0.25242 \times 10^{-8} \text{ C/cm}^2 \]
The pocket parameters, \(N_{pm}\) and \(L_p\), play important role in determining the RSCE. At the source side, the pocket profile is given as
\[
N_s(x) = -\frac{N_{pm} - N_{sub}}{L_p} x + N_{pm}
\]
Equation (1)

At the drain side, the pocket profile is given as
\[
N_d(x) = \frac{N_{pm} - N_{sub}}{L_p} [x - (L - L_p)] + N_{sub}
\]
\[
N_d(x) = N_{sub}(\frac{L}{L_p} - 1) + N_{pm}(1 - \frac{L}{L_p} + \frac{1}{L_p}) x
\]
Equation (2)

where \(x\) represents the distance across the channel. Since these pile-up profiles are due to the direct pocket implantation at the source and drain sides, the pocket profiles are assumed symmetric at both sides.

\[
N_{eff} = \frac{1}{L} \int_0^L [N_s(x) + N_d(x) + N_{sub}] dx
\]
Equation (3)

Putting the expressions of \(N_s(x)\) and \(N_d(x)\) from equations (1) and (2) in equation (3) the effective doping concentration is obtained in equation (4). This effective doping concentration expression is then used in deriving the surface potential model by applying Gauss’s law. This surface potential model is used to find the inversion layer charges and other parameters for determining the effective inversion layer mobility. When \(L_p \ll L\) for long channel device then the pocket profile has very little effect on uniform substrate concentration at the surface, but when \(L_p\) is comparable with \(L\) then the pocket profile parameters affects the substrate doping concentration at the surface of the n-MOSFET. This causes the surface potential, threshold voltage and hence effective mobility to change due to RSCE. Because of the pocket implantation, effective doping concentration increases with decreasing channel lengths. This becomes stronger when both peak pocket concentration and/or pocket length increases.

**Electron Current Density:**

From the sub threshold current model, according to the drift-diffusion equation, \(J_n\) is written as:
\[
J_n = q(-n\mu_{n,eff} \frac{d\Psi_s}{dx} + D_n \frac{dn}{dx}) = qDn(-n\frac{d\Psi_s}{dx} + \frac{dn}{dx})
\]
Equation (5)

\[
\Psi_s(x) = \text{surface potential}
\]
\[
n = \text{electron density}
\]
\[
D_n = \text{diffusion coefficient}
\]
\[
q = \text{electronic charge}
\]

\[\Phi_{th}\] is given as:
\[
\Phi_{th} = \frac{KT}{q} = \frac{Dn}{\mu_{n,eff}}
\]
Equation (6)

Multiplying equation 5 and 6 by an integrating \(\frac{1}{\Phi_{th}}\) factor to the RHS of equation 5 can be transformed into an exact derivative. Then using the surface potential model the electron density equation 7 can be found.

\[
J_n = -qDnN_{eff} \exp(-\frac{\Phi_{th} - V_{bs}}{\Phi_{th}}) (1 - \exp(-\frac{\Phi_{th} - V_{bs}}{\Phi_{th}})) \int_0^x \exp(-\frac{\Psi_s}{\Phi_{th}}) dx
\]
Equation (7)

Finally, the sub threshold drain current, \(I_{sub}\) in the channel is obtained by multiplying the electron current density \(J_n\) and the channel cross-sectional area (which is the multiplication of the effective channel thickness, \(t_{ch}\) and the channel width, \(W\)) as:
\[
I_{sub} = J_n W t_{ch}
\]
Equation (8)

The effective channel thickness is:
\[
t_{ch} = V_T \left(\frac{\varepsilon_S}{2qN_{eff}(2\Phi_F - V_{bs} - \frac{V_{GT}}{\theta})}\right)^{1/2}
\]
\[
t_{ch} = \frac{2qN_{eff}(2\Phi_F - V_{bs} - \frac{V_{GT}}{\theta})}{\varepsilon_S}\]

Where,
\[
V_{GT} = V_{GS} - V_T
\]
\[
\theta = \text{sub threshold ideality factor}
\]
\[
\Phi_F = \text{Fermi potential due to pocket implantation given as:}
\]
We know that $V_{TH} = V_T - \Delta V_{TO}$

Here,

$$\Delta V_{TO} = \frac{1}{C_{ox}} \sqrt{2q\varepsilon e_{ox} N_A \frac{\Phi_f}{\varepsilon_f}} - 2\Phi_f \left( \frac{X_f}{L} \right) \left[ 1 + \frac{2XdS}{X_f} - 1 \right] = -0.262 \times 10^{-8} \left[ 1 + \frac{2 \times 2.1777}{0.01} - 1 \right] = 0.955 \times 10^{-8} \left[ 1 + \frac{2 \times 2.1777}{0.01} - 1 \right] = 2.7411 \times 23.65 \times 10^{-3} = 0.01083 \left[ \frac{Q}{V} \right]$$

$$\Delta V_{TO} = 0.01083 \left[ \frac{Q}{V} \right]$$

$$\Delta V_{TO} = \frac{0.01083}{V}$$

$$\Delta V_{TO} = \frac{0.01083}{V}$$

For $HfO_2$

$$\Delta V_{TO} = \frac{0.0134}{V}$$

$$\Delta V_{TO} = \frac{0.0134}{V}$$

Where, $X_f$(juncture depth) = 0.01um

$C_{ox}$(oxide thickness) = $2.5 \times 10^{-7}$ cm

$N_{ox}$(surface doping concentration) $La_{ox} = 5 \times 10^{15}$ cm$^{-3}$

$N_{ox}$(peak pocket doping concentration) $La_{ox} = 1.8 \times 10^{13}$ cm$^{-3}$

$L_{ox}$(source or drain doping concentration) = $9 \times 10^{20}$ cm$^{-3}$

$N_{ox}$(source or drain doping concentration) = 5x10$^{12}$

$N_{ox}$(peak pocket doping concentration) for $HfO_2$ = $1.7 \times 10^{13}$ cm$^{-3}$

Conventional MOSFET Theory Based On Classical Mechanics for $V_T$

The threshold voltage of a MOS capacitor is defined as the gate voltage required to cause strong inversion or to make the band bending equal to 2$\Phi$. The equation for threshold voltage is written as shown in equation 1. The threshold Voltage is calculated theoretically as follows:

$$V_{T} = V_{ox} + \Phi_s$$

Equation (1)

Threshold voltage

where

Threshold voltage $V_{th} = V_{ox} + \Phi_s$  Equation (2)

Surface potential $\Phi_s = 2 \Phi_f$  Equation (3)

Fermi potential $\Phi_f = V_T - \frac{N_d}{N_A}$  Equation (4)

Oxide voltage $V_{ox} = \frac{3qN_c}{2 \varepsilon_f \Phi_s}$  Equation (5)

Depletion width $W_d$ (max) =

$$\frac{2e\varepsilon_f \Phi_s}{qNa}$$

Equation (6)

Oxide capacitance $C_{ox} = \frac{e_{ox}E_{ox}}{\varepsilon_{ox}}$

Main formula to calculate $V_T$ is: $V_T = V_{T_{mos}} + V_{fb}$

Where,

$V_{T_{mos}}$ = ideal threshold voltage (no work function difference between the gate and substrate)

$V_{fb}$ = flat band voltage

The ideal threshold voltage is: $V_{T_{mos}} = 2\Phi_f + Q_{ox}/C_{ox}$

Where,

$C_{ox} = e_{ox}/\varepsilon_{ox}$

The junction built in voltage: $\Phi_f = kT/q \ln(N_a/n_i)$

Depletion region charge density: $Q_{ox} = \sqrt{2e\varepsilon_f N_A(2\Phi_f + |V_{fb}|)}$

Where

the substrate bias $V_{th} = 0$

Thus, the ideal threshold voltage will be:

$V_{T_{mos}}$ is positive for nMOS:

$V_{T_{mos}} = 2kT/q \ln(N_a/n_i) + \sqrt{2e\varepsilon_f N_A 2\Phi_f - 1}/\varepsilon_{ox}$

Where

$V_{fb} = \Phi_ms - Q_{ox}/C_{ox}$

$\Phi_ms$ = work function difference between gate and wafer

$Q_{ox}$ = fixed charge for surface states (given)

$\Phi_ms = -(\frac{E_g}{2} + \Phi_f)$

$E_g$ = the band gap energy of silicon = 1.1eV

For silicon band gap energy at room temperature:

So, complete flat band formula: $E_g = 1.16 - 0.704 \times 10^{-3} \left( \frac{T^2}{T + 1108} \right)$

The entire threshold voltage ($V_T$) formula:

$$V_{fb} = \left( \frac{1.16 - 0.704 \times 10^{-3} \left( \frac{T^2}{T + 1108} \right)}{2} + \frac{kT}{q} \ln(N_A/n_i) - \frac{Q_{ox}}{C_{ox}} \frac{\varepsilon_{ox}}{\phi_{fb}} \right) \frac{1}{\varepsilon_{ox}}$$

Equation (7)

Derivation of Drain Current W.R.T The Thickness Of Dielectric Layer Of $SiO_2$:

The relation between capacitance, charge and voltage: $C = Q/V$

Gate oxide capacitance per unit area: $C_{ox} = e_{ox}/\varepsilon_{ox}$

Capacitance per unit length of the oxide: $C = W.C_{ox}$

![Fig2. Voltages of Different Operating Regions](image-url)
The equations for the transistor are obtained in all modes (cut off, triode, and saturation)

Although the voltage applied across the oxide is Vgs, charge does not start collecting at the substrate until inversion occurs, just as in a MOS capacitor. Inversion only occurs when Vgs>Vth, therefore, the charge at the silicon-oxide interface can be described as: Q=W.Cox(Vgs-Vth). During normal operation, a transistor will have an applied voltage difference between the source and drain, VDS.

As a result, the voltage between the gate and the oxide decreases towards the positive x direction. The reason is the drain is at a higher potential than the source, thus the potential difference between the gate and the oxide decreases from source to the drain. Thus, charge equation is now:

\[ Q = W \times Cox \times (V_{GS} - V(x) - V_{TH}) \]

An accurate description of the charge at the silicon-oxide interface as a function of x, the current equation is:

\[ I = Q \nu \]

\[ V = -\mu.\xi \]

\[ V = \mu_n \frac{dv}{dx} \]

\[ I_d = W \times Cox \times (V_{GS} - V(x) - V_{TH}) \mu_n \frac{dv(x)}{dx} \]

To solve the differential equation both sides integration is done:

\[ \int_{x=L}^{x=0} I_d(x) = \int_{V_{ GS} = 0}^{V_{ GS} = V_{ TH}} W \times Cox(V_{ GS} - V(x) - V_{ TH}) \mu_n dV \]

\[ I_d = \frac{1}{2} \mu_n Cox \frac{W}{L} (2(V_{ GS} - V_{ TH})V_{ DS} - V_{ DS}^2) \]

The maximum current achievable is:

\[ I_{d,max} = \frac{1}{2} \mu_n Cox \frac{W}{L} (V_{ GS} - V_{ TH})^2 \]

Regions of operation: when, VDS ≤ VGS-VTH and VGS ≥ VTH, the transistor is said to be in triode.

\[ I_{d,triode} = \frac{1}{2} \mu_n Cox \frac{W}{L} (V_{ GS} - V_{ TH} - \frac{V_{ DS}}{2})V_{ DS} \]

VDS ≤ VGS-VTH and VGS ≥ VTH, the transistor is said to be in saturation.

\[ I_{d,sat} = \frac{1}{2} \mu_n Cox \frac{W}{L} (V_{ GS} - V_{ TH})^2 \]

When VGS ≤ VTH, the substrate is not inverted and no current can flow, I0=0.

As per the above equation the drain current is dependent on the mobility, thickness of the oxide layer and the aspect ratio (W/L). If the width of the channel length is increased, the resistivity decreases, drain current increases. Mobility of the electrons is directly proportional to the drain current. If the mobility increases, the time taken by the electron to reach from source to drain decreases. As a result the drain current increases due to rapid movements of electrons.

II. CONCLUSION

In this project aim is to plot graphs between different parameters of La2O3 and HfO2 and comparative analysis of the features of the graph of both the oxides. The threshold voltage was at first varied with the channel length by keeping the pocket dose constant, then threshold voltage and channel length is varied by changing the pocket dose (doping). Pocket doping varied with channel length. So, the detail study of the pocket doping profile is needed to construct an appropriate modeling of the threshold voltage. For further miniaturization of the device the thickness of the oxide layers were varied with respect to the threshold voltage and drain current and the graph is obtained between these parameters through MATLAB. The silicon dioxide shows larger leakage current, lesser capacitance which leads to lower device current and lesser circuit speed. On the contrary the high – K dielectric material shows lesser leakage current and increased device performance by higher capacitance which enhances device current and speed. La2O3 shows that the channel is formed much faster as the charges are induced more easily for small threshold voltage when the oxide thickness is increased and almost constant charges flows from source to drain thus causing larger capacitance. The comparative study shows that the power consumption is reduced to a great extent and device performance is enhanced for La2O3 (High K dielectric material) output current also increases.

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ABBREVIATIONS AND ACRONYMS

\( Q_{GC} \) = work function difference between gate and channel
\( Q_{BO} \) = depletion region charge density (body bias at ground potential)
\( Q_{OX} \) = oxide interface charge
\( C_{ox} \) = oxide capacitance per unit area
\( \Phi_s (sub) \) = Fermi potential for (p-type) substrate
\( \Phi_{g} (gate) \) = Fermi potential for gate
q = unit electron charge = 1.6 X10^-19 coulomb
\[ N_A = \text{acceptor doping concentration} \]
\[ \varepsilon_S = \text{permittivity of silicon} = 11.7 \times 8.85 \times 10^{-14} \text{F/cm} \]
\[ \varepsilon_{ox} = \text{permittivity of oxide} = 3.97 \times 8.85 \times 10^{-14} \text{F/cm} \]
\[ \varepsilon_{HfO2} = \text{permittivity of hafnium oxide} = 19.6 \times 8.85 \times 10^{14} \text{F/cm} \]
\[ t_{ox} = \text{thickness of the oxide} \]
\[ N_{int} = \text{oxide interface charge density} \]
\[ V_{to} = \text{zero-bias threshold voltage calculated using the conventional long-channel formula} \]
\[ \Delta V_t = \text{reduced threshold voltage due to short-channel effect} \]
\[ X_{ds} = \text{depth of the p-n junction depletion region associated with the source} \]
\[ X_{dp} = \text{depth of the p-n junction depletion region associated with the drain} \]
\[ \Delta L_s = \text{lateral extent of the depletion regions associated with the source junctions} \]
\[ \Delta L_p = \text{lateral extent of the depletion regions associated with the drain junctions} \]
\[ X_j = \text{metallurgical junction depth} \]
\[ K = \text{Boltzmann constant} = 1.38 \times 10^{-23} \text{J/K} \]
\[ T = \text{Temperature in Kelvin} \]
\[ N_{sub} = \text{substrate doping concentration} \]
\[ N_{pe} = \text{peak pocket doping concentration} \]
\[ N_{pe} = \text{effective pocket doping concentration} \]
\[ L_p = \text{pocket length} \]
\[ N_a = \text{source or drain doping concentration} \]
\[ X = \text{distance across the channel from source to drain} \]
\[ \Psi_s = \text{surface potential} \]
\[ n = \text{electron density} \]
\[ D_n = \text{diffusion coefficient} \]
\[ W = \text{channel width} \]
\[ T_{ch} = \text{effective channel thickness} \]
\[ \Phi_w = \text{work function difference between gate and wafer} \]
\[ V_{t, \text{mos}} = \text{ideal threshold voltage} \]
\[ V_{fb} = \text{flatband voltage} \]
\[ \mu = \text{mobility of electrons} \]
\[ KT/q = 0.26 \text{mV at room temperature (300K)} \]
\[ K = 1.38 \times 10^{-23} \text{J/K} = \text{Boltzmann’s constant} \]
\[ N_{int} = \text{carriers in intrinsic silicon} = 1.45 \times 10^{10} \text{cm}^3 \]
\[ \Phi_f = 0.341 \text{V} = \text{work function difference between the intrinsic potential and Fermi potential} \]
\[ \text{Cox} = \text{gate oxide capacitance per unit area} \]
\[ N_{sub}(\text{substrate doping concentration})L_{ox} = 5.2 \times 10^{-12} \text{cm}^{-3} \]
\[ N_{pe}(\text{peak pocket doping concentration})L_{ox} = 1.8 \times 10^{-13} \text{cm}^{-3} \]

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