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Analysis and Study of V-I Characteristics by Replacing Low-K Dielectric (HfO_2) with High-K Dielectric (La_2O_3) in MOSFET

Anurekha Mukherjee, Sohini Mondal

Abstract*— This project journal paper presents the analysis and study of Lanthanum oxide La_2O_3, one of the promising high-k dielectric films used in the MOSFET over hafnium dioxide, HfO_2. Capacitance-Voltage measurements were carried out to investigate properties such as oxide charges and interface trap charges that exist in the dielectric La_2O_3, an inorganic compound containing the rare earth element lanthanum and oxygen . The investigation has been carried out by experiment and modeling. With the advent of semiconductor technology in VLSI era, the channel length of a metal oxide semiconductor has drastically gone down. DIBL (Drain Induced Barrier Lowering) is one of the short channel effects which degrade the performance of a MOSFET with its down scaling. To understand this effect the study of the nature of surface potential and energy is very important. In this project an analytical model for threshold voltage of short channel MOSFETs is presented. For such devices, the depletion regions due to source/ drain junctions occupy a large portion of the channel, and hence are very important for accurate modeling. The proposed threshold voltage model is based on a realistic physically – based model for the depletion layer depth along the channel that takes into account its variation due to the source and drain junctions .With this, the unrealistic assumption of a constant depletion layer depth has been removed , resulting in an accurate prediction of the threshold voltage. The graphs between different parameters of HfO_2 and La_2O3 are verified against the simulator MATLAB and the comparative analysis of the features of the graph of both the oxides has been done.

***Index Terms*—Channel Length, DIBL, Pocket doping, Threshold Voltage**

I. INTRODUCTION

Demand for larger scale integration of MOS circuits on a single chip urged of miniaturization of MOS devices. As the channel length shrinks, many short –channel effects were observed mainly reduction of threshold voltage, increased off-state leakage current and Drain-induced barrier lowering. Charge sharing model have been used to model the short-channel effects (SCEs). The charge sharing model assumptions of constant surface potential and no divergence of electric field lines in the gate oxide are invalid for high drain and substrate biases. On the other hand, two-dimensional analysis has accurately predicted the values of threshold voltage of short channel MOSFET's and breakdown voltage. We have derived the analytical relations for surface potential, threshold voltage and longitudinal field. Without any assumption, we have proposed a model for short channel factor which shows the dependence on the channel width and drain voltage. The effect of charge carrier density is to raise the threshold voltage of submicron devices operating at any drain voltage. It is observed from our analysis that short-channel effect is more dominant in the submicron devices with thinner gate oxide. Our study also predicts that SCE in short channel device is more effective in presence of charge carrier density. It is also observed that the short channel factor shows a weak dependence on the substrate doping due to the inclusion of carrier charge density.

The continuing miniaturization of feature sizes in integrated circuits(ICs) has led to improvement of device performance and higher packing densities .The aim of scaling is to reduce total size and to increase overall functional density. As the channel length shrinks, many short-channel effects are introduced. The short channel effect can be reduced or can be reversed (reverse short channel effect; RSCE), by locally raising the channel doping near source and drain junctions. Not only this but also using La_2O_3 (a high K dielectric) instead of HfO_2 is done for allowing further miniaturization.

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion layer widths of the source and drain junction. As the channel length is reduced to increase both the operation speed and the number of components per chip, the so-called short channel effects arise. So , the objectives of the project is to find out the threshold voltages for different channel lengths by constructing a threshold voltage shifting profile and observing the changes in current and threshold voltage by reducing the thickness of the insulating layer.

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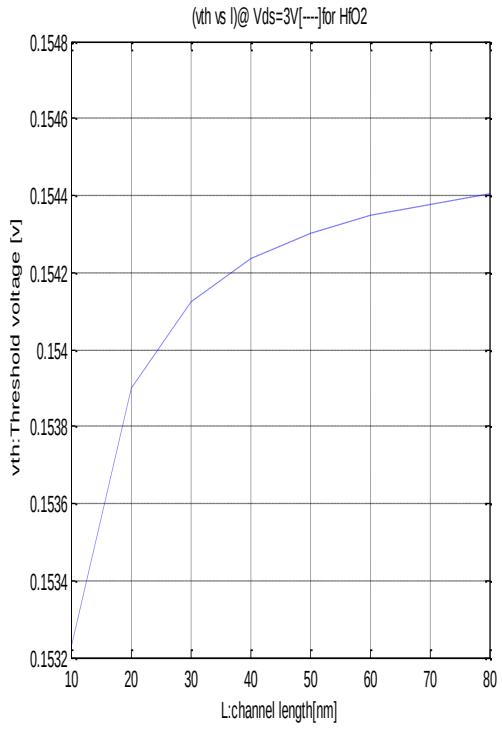
A. *Figures*

Vth vs L Graphs for HfO_2 & La_2O_3 Without Varying Pocket Doping



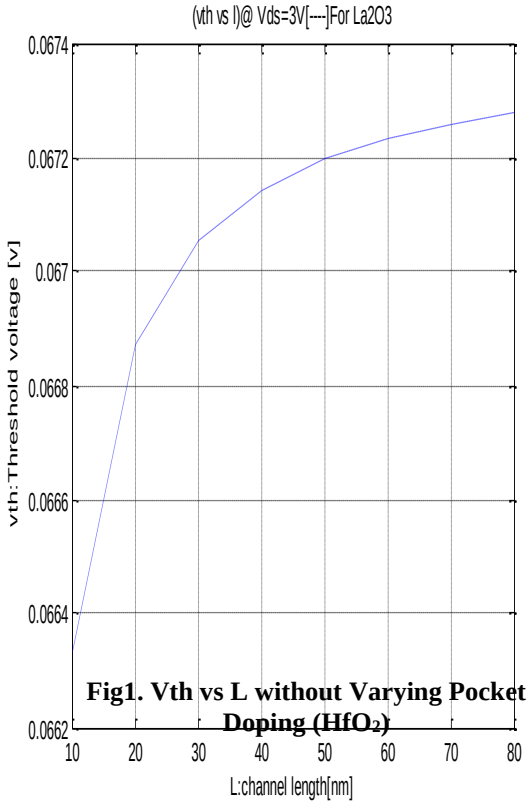


Fig1. Vth vs L without Varying Pocket Doping (HfO_2)

Fig2. Fig1. Vth vs L without Varying Pocket Doping (La_2O_3)

Threshold Voltage(Vth) versus L graphs For HfO_2 & La_2O_3 By Varying Pocket Doping

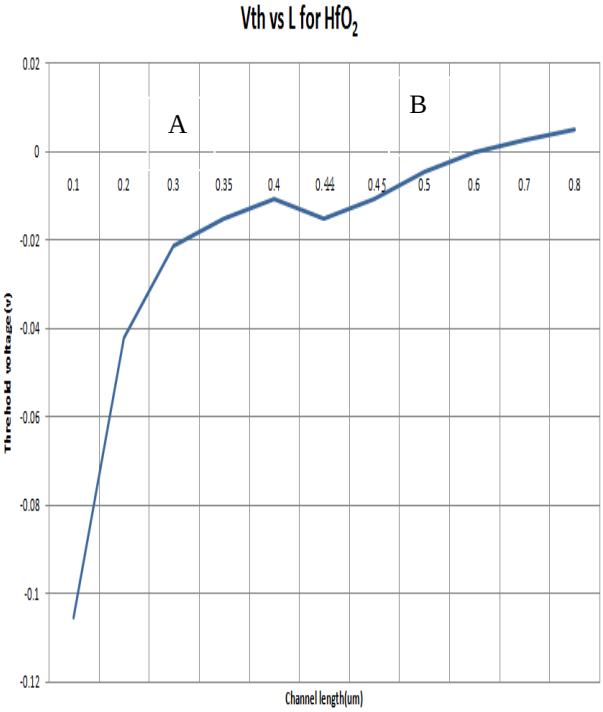


Fig3. Vth vs L by Varying Pocket Doping (HfO_2)

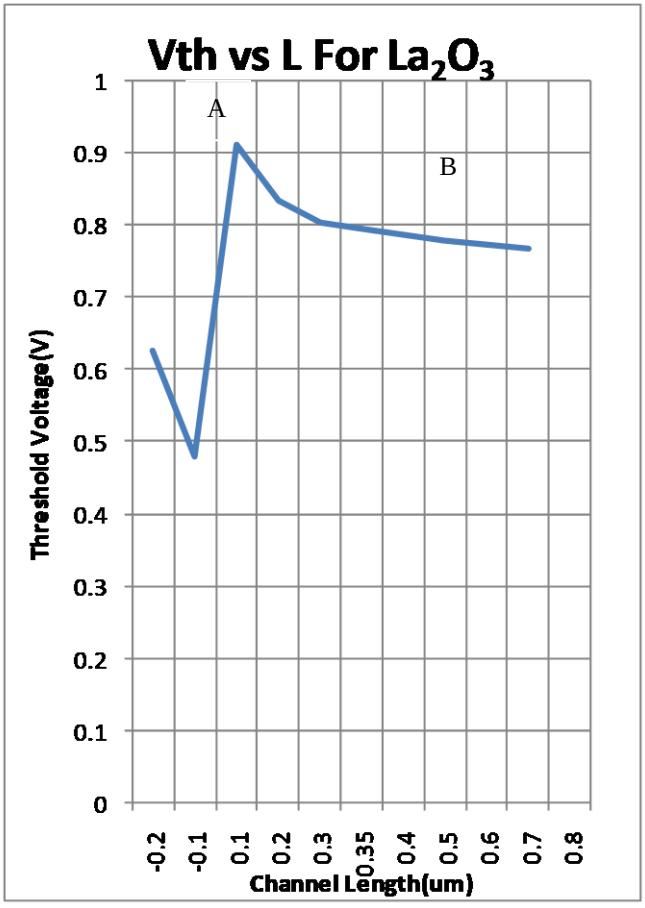


Fig4. Vth vs L Varying Pocket Doping (La_2O_3)

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Graph Between La_2O_3 And HfO_2:

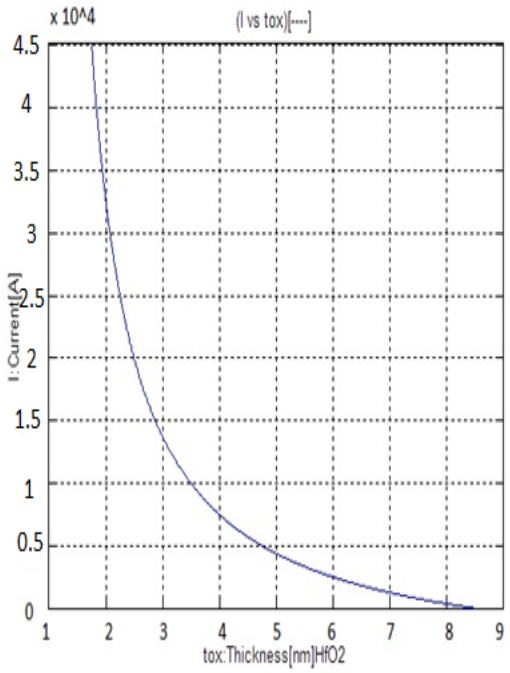

Fig5. Id vs tox For (HfO_2)

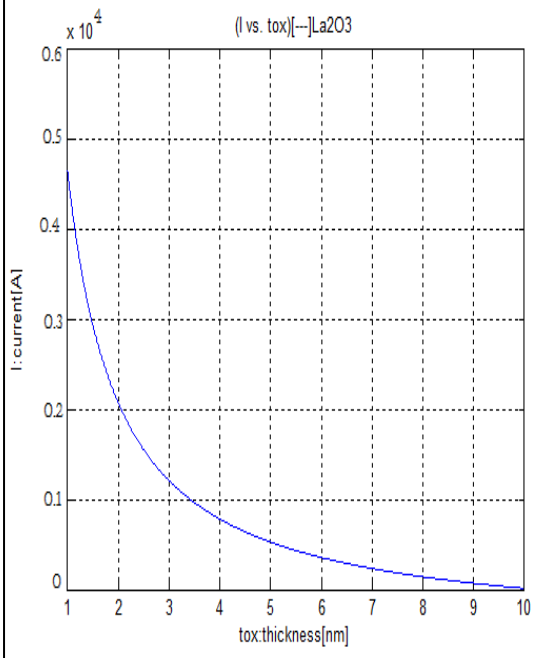

Fig6. Id vs tox For (La_2O_3)

Graph Between I_d versus t_{ox} Graph For La_2O_3 And HfO_2:

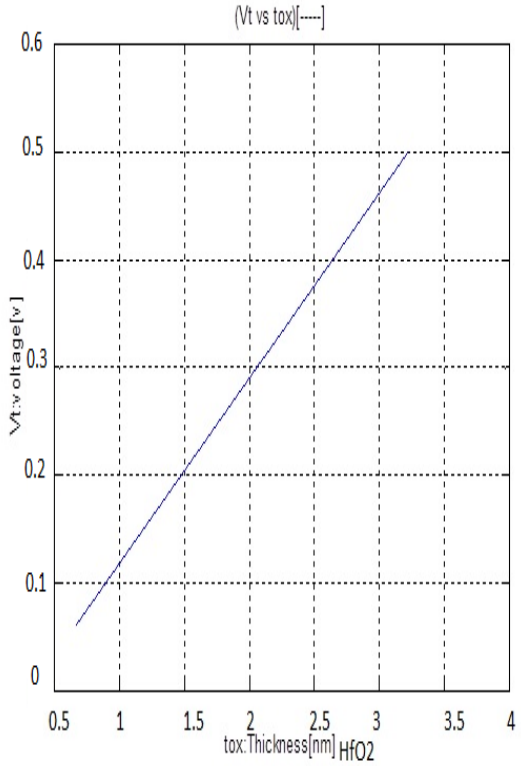

Fig7. Vt vs tox For (HfO_2)

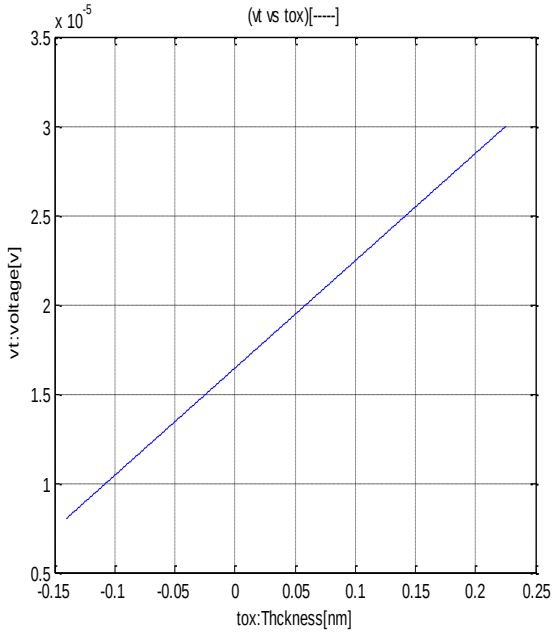

Fig8. Vt vs tox For (La_2O_3)

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B. *Figures and Tables*

Vth vs L Graphs for HfO2 and La2O3 without Varying Pocket Doping

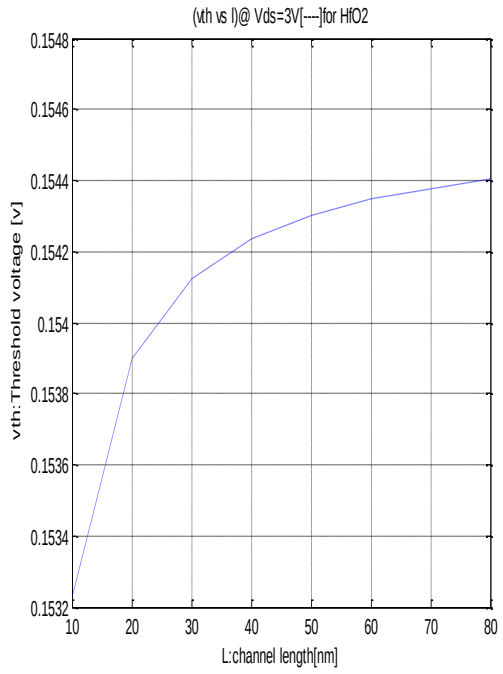

Fig1. Vth vs L without Varying Pocket Doping (HfO_2)

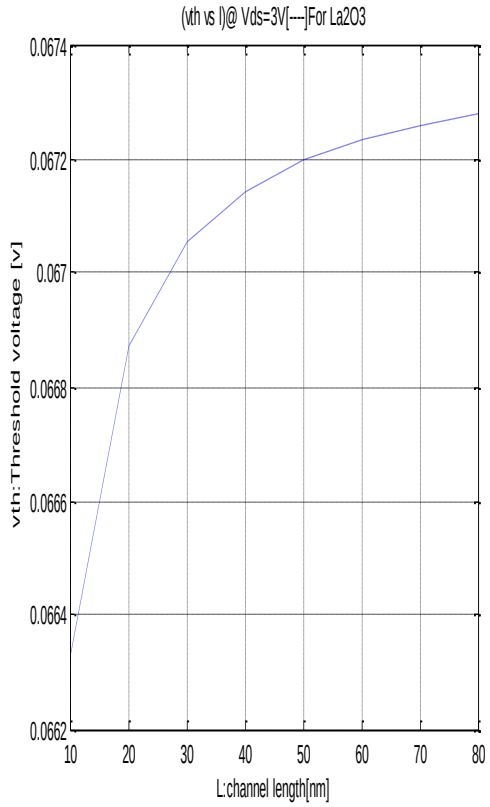

Fig2. Vth vs L (La_2O_3) Without varying Pocket Doping

Table1. Comparison of Vth vs L Graph for HfO2 and La2O3 without Varying Pocket Doping

HfO_2	La_2O_3
As the dielectric constant is more than SiO_2 (i.e. 19.6) therefore the threshold voltage reduces more as compared to SiO_2 for shorter channel lengths and hence DIBL effect reduces to a greater extent as compared to SiO_2	The dielectric constant for La_2O_3 is 27 which is more as compared to SiO_2 and HfO_2 therefore the DIBL effect reduces more as compared to SiO_2 and HfO_2 for shorter channel length the threshold voltage reduces to a greater extent
Off state leakage current is decreased to a greater extent because the dielectric constant is more as compared to SiO_2. Thus charge sharing effect between source, drain region and channel (DIBL) effect is reduced as compared to SiO_2.	The dielectric constant is more for La_2O_3 as compared to SiO_2 and HfO_2 due to which charge sharing effect between drain, source and Channel (DIBL) reduces to a greater extent.

Table2. Threshold voltage values For different Channel length (HfO_2)By Varying The Pocket Doping

Channel length L(um)	Vt(V)	ΔVto	Vth=Vt- ΔVto
0.8	0.0219	0.0165	0.005159
0.7	0.0220	0.0191	0.0029
0.6	0.0222	0.0223	-0.00004
0.5	0.0225	0.0268	-0.0042
0.4	0.0229	0.0335	-0.0105
0.35	0.0232	0.0382	-0.0150
0.3	0.0236	0.044666	-0.02105
0.2	0.0249	0.067	-0.042091
0.1	0.0285	0.134	-0.1054

Table3. Threshold voltage values for different Channel length (La_2O_3) By Varying the Pocket Doping

Channel Length(L in um)	Vt(V)	ΔVto(V)	Vth=Vt-Vto
0.8	0.7779	0.01353	0.7643
0.7	0.7832	0.01547	0.7677
0.6	0.7903	0.01805	0.7723
0.5	0.8002	0.02166	0.7785
0.4	0.8150	0.0270	0.7879

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0.35	0.8254	0.03094	0.7944
0.3	0.8391	0.0361	0.80306
0.2	0.8862	0.0541	0.8320
0.1	1.0189	0.1083	0.91067
-0.1	0.3701	-0.1083	0.47841
-0.2	0.5725	-0.0541	0.6266

Threshold Voltage versus channel length graphs of HfO_2 & La_2O3 By Varying Pocket Doping

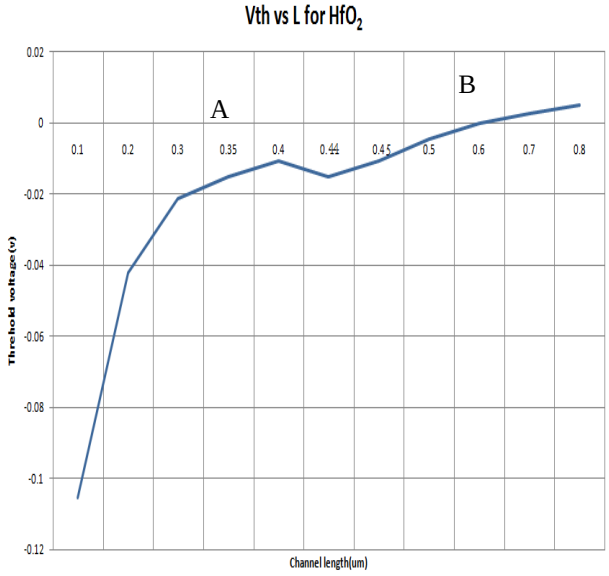

Fig3. Vth vs L (HfO_2) Varying Pocket Doping

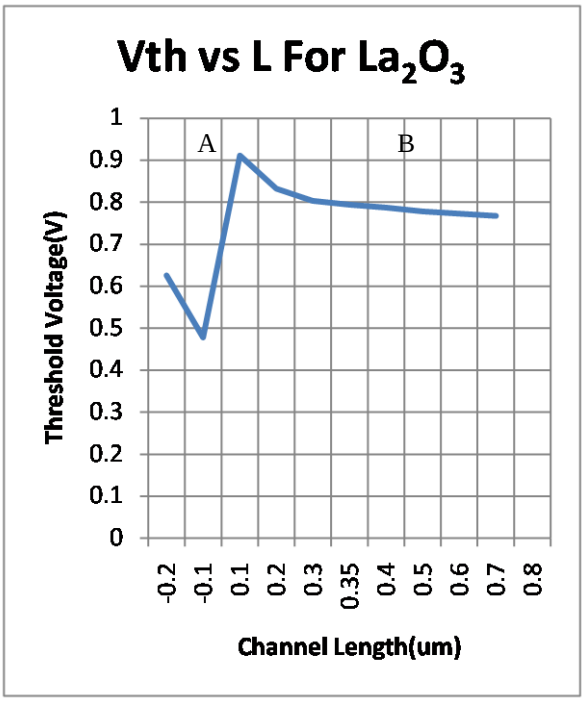

Fig4. Vth vs L (La_2O_3) Varying Pocket Doping

Table4. Comparison of Vth vs L Graph Varying Pocket Doping for HfO_2 and La_2O_3

HfO_2	La_2O_3
We can reduce the channel length till 0.44um	We can reduce the channel length till 0.1um

I_d vs tox Graph Of La_2O_3 And HfO_2:

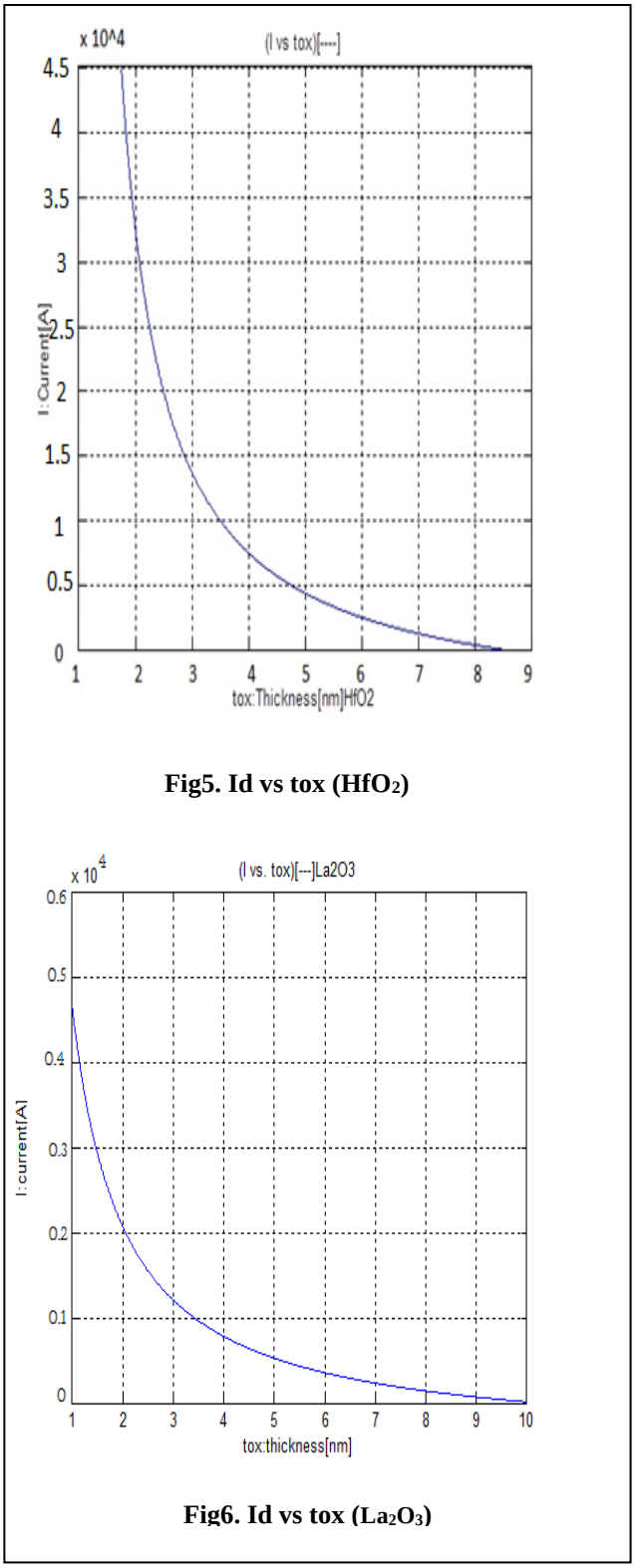

Fig5. Id vs tox (HfO_2)

Fig6. Id vs tox (La_2O_3)

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Table5. Comparison of Id vs tox Graphs for HfO_2 & La_2O_3

HfO_2	La_2O_3
As $C=\frac{K\varepsilon_0 A}{d}$ and the value of the dielectric constant is more for HfO_2 as compared to SiO_2 therefore the capacitance increases more for HfO_2 and the drain current increases more as compared to silicon dioxide	As $C=\frac{K\varepsilon_0 A}{d}$ and K=27 for lanthanum oxide capacitance is more as compared to HfO_2 and SiO_2 so the drain current increases more for reducing the thickness of the oxide layer
As the value of the dielectric constant is more as compared La_2O_3 so the drain current is less hence the mobility of the electrons to reach from source to drain decreases and device current increases.	Value of the dielectric constant is more as compared to HfO2 therefore the mobility of the electrons to reach from source to drain increases and drain current increases.
As the threshold voltage is lesser for HfO_2 for reduction of channel length, less gate voltage is required for the formation of the channel and for less gate voltage more opposite charges are induced and the channel formation takes place more easily as the dielectric constant value is more for HfO_2.	Lesser gate voltage is required for the formation of the channel as compared to HfO_2.Thus opposite charges is induced more easily and channel formation. Thus for lesser thickness of oxide layer channel formation is done more easily.

Vt versus t_{ox} Graph For La_2O3 And HfO_2:

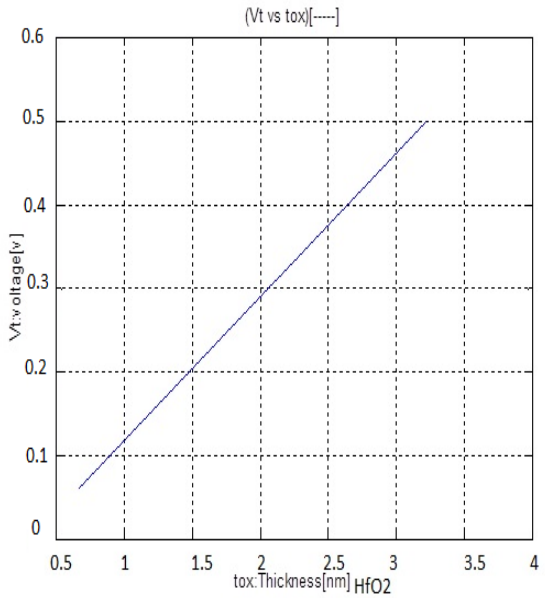

Fig7. Vth vs tox for HfO_2

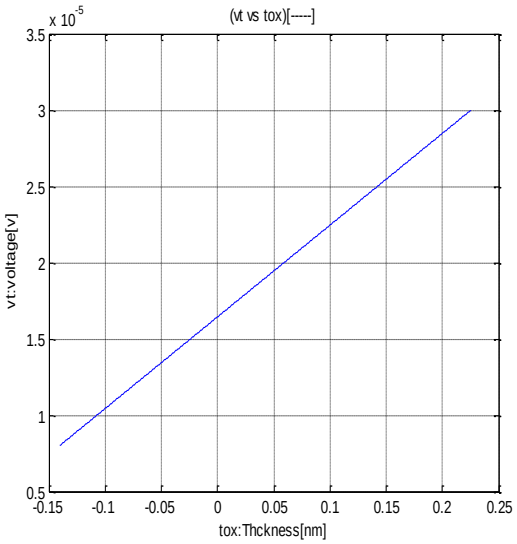

Fig8. Vth vs tox Graph for La_2O_3

Table6. Comparison of Vth vs tox Graph for HfO_2 & La_2O_3

HfO_2	La_2O_3
Threshold voltage is reduced to a greater extent as compared for shorter thickness of the oxide layer so the channel is started to form at this threshold voltage.	Threshold voltage is reduced more as compared to and HfO_2 thus for shorter thickness of the oxide layer channel formation becomes more easier for La_2O_3 as compared to and HfO_2.
Oxide capacitance is more as compared to La_2O_3hence the on state current is less and device speed is less as compared to La_2O_3.	Oxide capacitance is more as compared to HfO2 hence the on state current is more and device speed is more as compared to HfO_2.

C. Equations

Numerical Analysis For Plotting The Variation Of The Threshold Voltage V_T As A Function Of The Channel Length:

Expression of the Threshold voltage For La_2O_3

$$V_{TO} = \Phi_{GC} - 2\Phi_F(sub) - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{Ox}}{C_{OX}}$$

Calculation of ϕ_{GC}

$\phi_{GC} = \phi_F$ (sub)- ϕ_F (gate)= -0.35v- 0.55 v=0.90V

Calculation of depletion region charge:

$$Q_{BO} = \sqrt{2q\varepsilon_{La}N_A\,|2\Phi_F|}$$

$$= \sqrt{2\times1.6\times10^{-19}\times1.5\times10^{13}\times27\times8.85\times10^{-14}(|-2\times0.3|)}$$

$$= -0.25242\times10^{-8}\,C/cm^2$$

The oxide-interface charge is:

$$Qox = qNox = 1.6\times10^{-19}\times4\times10^{8} = 6.4\times10^{-11}C/cm^2$$

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The oxide capacitance is given by:

We can combine all the components and calculate the threshold voltage:

$$Cox = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{27 \times 8.85 \times 10^{-14}}{2.5 \times 10^{-4}} = 0.693 \times 10^{-8} F/cm$$

$$V_{TO} = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}}$$

$$\frac{Q_{BO}}{C_{OX}} = \frac{-0.262 \times 10^{-8}}{0.955 \times 10^{-8}} = -0.2741$$

$$\frac{Q_{OX}}{C_{OX}} = 6.6959 \times 10^{-3}$$

$$V_{TO} = 0.0674V$$

The source and drain junction built-in voltage is:

$$\Phi_o = \frac{KT}{q} \ln \frac{N_A N_D}{ni^2} = 0.026 \ln \frac{10^{33}}{2.304 \times 10^{21}} = 0.6967V$$

The source and drain junction built-in voltage is:

$$\Phi_o = \frac{KT}{q} \ln \frac{N_A N_D}{ni^2} = 0.026 \ln \frac{10^{34}}{2.304 \times 10^{21}} = 0.7565V$$

Junction built-in voltage is lesser than HfO_2

Depths of source and drain junction depletion region can be found as:

$$X_{dD} = X_{dS} = \sqrt{\frac{2\varepsilon_{La}\Phi o}{qN_A}} = 0.1177 \times 10^{-4} cm$$

The threshold voltage shift can be calculated as:

$$\Delta V_{TO} = \frac{1}{C_{OX}} \sqrt{2q\varepsilon_{Hf} N_A 2\Phi_F} \frac{Xj}{2L} [(Xj\sqrt{1+\frac{2XdD}{Xj}} - 1) + Xj\sqrt{1+\frac{2XdS}{Xj}} - 1]$$

$$= \frac{-0.262 \times 10^{-8}}{0.9558 \times 10^{-8}} \times \frac{0.01}{L} [\sqrt{1+\frac{2 \times 0.1177}{0.01}} - 1]$$

$$= 2.7411 \times \frac{10^{-3}}{L} [\sqrt{1+21.14} - 1]$$

$$= \frac{0.01083}{L} V$$

Expression of the Threshold voltage For HfO_2

$$V_{TO} = \Phi_{GC} - 2\Phi_F(sub) - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{Ox}}{C_{OX}}$$

Calculation of ϕ_{GC}

ϕ_{GC} = ϕ_F (sub)- ϕ_F (gate)= -0.35v- 0.55 v=0.90V

Calculation of depletion region charge:

$$Q_{BO} = \sqrt{2q\varepsilon_{Hf} N_A |2\Phi_F|}$$

$$= \sqrt{2 \times 1.6 \times 10^{-19} \times 1.5 \times 10^{13} \times 25 \times 8.85 \times 10^{-14} (|-2 \times 0.3|)}$$

$$= -0.25242 \times 10^{-8} C/cm^2$$

The oxide-interface charge is:

$$Qox = qNox = 1.6 \times 10^{-19} \times 4 \times 10^{8} = 6.4 \times 10^{-11} C/cm^2$$

The oxide capacitance is given by:

We can combine all the components and calculate the threshold voltage:

$$Cox = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{19.6 \times 8.85 \times 10^{-14}}{2.5 \times 10^{-4}} = 0.693 \times 10^{-8} F/cm$$

$$V_{TO} = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}}$$

$$\frac{Q_{BO}}{C_{OX}} = \frac{-0.25242 \times 10^{-8}}{0.69384 \times 10^{-8}} = -0.3638$$

$$\frac{Q_{OX}}{C_{OX}} = 9.224 \times 10^{-3}$$

$$V_{TO} = 0.15475V$$

The source and drain junction built-in voltage is:

$$\Phi_o = \frac{KT}{q} \ln \frac{N_A N_D}{ni^2} = 0.026 \ln \frac{10^{33}}{2.304 \times 10^{21}} = 0.6067V$$

The source and drain junction built-in voltage is:

$$\Phi_o = \frac{KT}{q} \ln \frac{N_A N_D}{ni^2} = 0.026 \ln \frac{10^{34}}{2.304 \times 10^{21}} = 0.7565V$$

Depths of source and drain junction depletion region can be found as:

$$X_{dD} = X_{dS} = \sqrt{\frac{2\varepsilon_{Hf}\Phi o}{qN_A}} = 0.1057 \times 10^{-4} cm$$

The threshold voltage shift can be calculated as:

$$\Delta V_{TO} = \frac{1}{C_{OX}} \sqrt{2q\varepsilon_{Hf} N_A 2\Phi_F} \frac{Xj}{2L} [(Xj\sqrt{1+\frac{2XdD}{Xj}} - 1) + Xj\sqrt{1+\frac{2XdS}{Xj}} - 1]$$

$$= \frac{0.25242 \times 10^{-8}}{0.69384 \times 10^{-8}} \times \frac{0.01}{L} [\sqrt{1+\frac{2 \times 0.1057}{0.01}} - 1]$$

$$= 0.3638 \times \frac{0.01}{L} [\sqrt{1+21.14} - 1]$$

$$= \frac{0.0134}{L} V$$

Pocket Implant or Pocket Dose:

The pocket implantation, which causes the RSCE, is done by adding impurity atoms both from the source and drain edges. It is assumed that the peak pocket doping concentration (N_{pm}) gradually decreases linearly towards the substrate level concentration (N_{sub}) with a pocket length (L_p) from both the source and drain edges. The basis of the model of the pocket is to assume two laterally linear doping profiles from both the source and drain edges across the channel.

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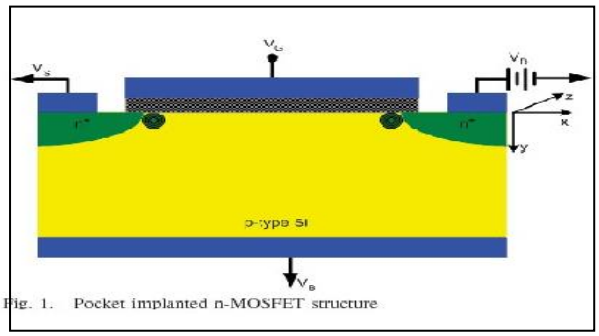

Fig. 1. Pocket implanted n-MOSFET structure

The pocket parameters, N_{pm} and L_p, play important role in determining the RSCE. At the source side, the pocket profile is given as

$$Ns(x) = -\frac{Npm - Nsub}{Lp}x + Npm$$

$$Ns(x) = Nsub\frac{x}{Lp} + Npm(1 - \frac{1}{Lp}x)$$

Equation(1

At the drain side, the pocket profile is given as Equation(2)

$$Nd(x) = \frac{Npm - Nsub}{Lp}[x - (L - Lp)] + Nsub$$

$$Nd(x) = Nsub(\frac{L}{Lp} - \frac{1}{Lp}) + Npm(1 - \frac{L}{Lp} + \frac{1}{Lp}x)$$

,where x represents the distance across the channel. Since these pile-up profiles are due to the direct pocket implantation at the source and drain sides, the pocket profiles are assumed symmetric at both sides

$$N_{eff} = \frac{1}{L}\int_0^L [Ns(x) + Nd(x) + Nsub]dx$$

Equation(3)

With these two conceptual pocket profiles of equations (1) and (2), the profiles are integrated mathematically along the channel length from the source side to the drain side and then the integration result is divided by the channel length (L) to derive an average effective doping concentration (Neff) as shown in equation (3)

.

$$N_{eff} = Nsub(1 - \frac{Lp}{L}) + \frac{Npm \times Lp}{L}$$

Equation(4

Putting the expressions of Ns(x) and N_d(x) from equations (1) and (2) in equation (3) the effective doping concentration is obtained in equation (4). This effective doping concentration expression is then used in deriving the surface potential model by applying Gauss's law. This surface potential model is used to find the inversion layer charges and other parameters for determining the effective inversion layer mobility. When L_p<<L for long channel device then the pocket profile has very little effect on uniform substrate concentration at the surface, but when L_p is comparable with L then the pocket profile parameters affects the substrate doping concentration at the surface of the n-MOSFET. This causes the surface potential, threshold voltage and hence effective mobility to change due to RSCE. Because of the pocket implantation, effective doping concentration increases with decreasing channel lengths. This becomes stronger when both peak pocket concentration and/or pocket length increases.

Electron Current Density:

From the sub threshold current model, according to the drift-diffusion equation, Jn is written as:

$$Jn = q(-n\mu_{n,eff}\frac{d\Psi s}{dx} + Dn\frac{dn}{dx})$$

$$= qDn(-\frac{n}{\Phi_{th}}\frac{d\Psi s}{dx} + \frac{dn}{dx})$$

Equation (5)

$\Psi s(x)$ = surface potential
n =electron density
D_n =diffusion coefficient
q =electronic charge

Φ_{th} is given as:

$$\Phi th = \frac{KT}{q} = \frac{Dn}{\mu_{n,eff}}$$

Equation (6)

Multiplying equation 5 and 6 by an integrating $e^{\frac{\Psi s}{\Phi th}}$ factor to the RHS of equation 5 can be transformed into an exact derivative .Then using the surface potential model the electron density equation 7 can be found.

$$Jn = -qDnNeff\exp(-\frac{\Phi_{bi} - V_{BS}}{\Phi th})\frac{(1 - \exp(\frac{-V_{DS}}{\Phi th}))}{\int_0^L \exp(-\frac{\Psi s}{\Phi th})dx}$$

Equation (7)

Finally , the sub threshold drain current , I_{sub} in the channel is obtained by multiplying the electron current density ,J_n and the channel cross-sectional area(which is the multiplication of the effective channel thickness, t_{ch} and the channel width ,W)as: $I_{sub}=J_n.W.t_{ch}$ Equation (8)

The effective channel thickness is:

$$tch = V_T(\frac{\varepsilon_{Si}}{2qNeff(2\Phi_F - V_{BS} - \frac{V_{GT}}{\theta})})^{1/2}$$

$$=> V_T = tch(\frac{2qNeff(2\Phi_F - V_{BS} - \frac{V_{GT}}{\theta})}{\varepsilon_{Si}})^{1/2}$$

Where, $V_{GT} = V_{GS} - V_T$

Θ = sub threshold ideality factor

ΦF = Fermi potential due to pocket implantation given as:

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We know that $V_{TH}=V_T-\Delta V_{TO}$

Here,

$$\Delta V_{TO}=\frac{1}{C_{ox}}\sqrt{2q\varepsilon_{La}N_A|2\Phi_F|}\frac{Xj}{L}[\sqrt{1+\frac{2XdS}{Xj}}-1]$$

$$=\frac{-0.262\times10^{-8}}{0.955\times10^{-8}}[\sqrt{1+\frac{2\times0.1177}{0.01}}-1]\frac{0.01}{L}$$

$$=\frac{2.7411\times23.65\times10^{-3}}{L}$$

$$=\frac{0.01083}{L}V$$

$$\boxed{\Delta V_{TO}=\frac{0.01083}{L}V}$$

$$\Delta V_{TO}=\frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Hf}N_A|2\Phi_F|}\frac{Xj}{L}[\sqrt{1+\frac{2XdS}{Xj}}-1]$$

$$=\frac{-0.25242\times10^{-8}}{0.6938\times10^{-8}}[\sqrt{1+\frac{2\times2.57}{0.01}}-1]\frac{0.01}{L}$$

$$=\frac{0.3638\times3.7053\times0.01}{L}$$

$$=\frac{0.0134}{L}V$$

$$\Delta V_{TO}=\frac{0.0134}{L}VForHfO_2$$

Where, X_j(junction depth)=0.01um

t_{ox}(oxide thickness)= $2.5\times10^{-7}cm$

N_{sub}(substrate doping concentration)$La_2O_3=5\times10^{12}cm^{-3}$

N_{pm}(peak pocket doping concentration) $La_2O_3=1.8\times10^{13}cm^{-3}$

L_p(pocket length)= $25\times10^{-7}cm$

N_{sd}(source or drain doping concentration)= $9\times10^{20}cm^{-3}$

N_{sub}(substrate doping concentration) for HfO_2=5x10^{12}

N_{pm}(peak pocket doping concentration) for HfO_2 =$1.7\times10^{13}cm^{-3}$

Conventional MOSFET Theory Based On Classical Mechanics for VT:

The threshold voltage of a MOS capacitor is defined as the gate voltage required to cause strong inversion or to make the band bending equal to 2Φf. The equation for threshold voltage is written as shown in equation 1. The threshold Voltage is calculated theoretically as follows:

Equation (1)

Threshold voltage

where

Threshold voltage $V_{th}=V_{ox}+\Phi_s$ Equation (2)

Surface potential $\Phi_s=2\Phi_f$ Equation (3)

Fermi potential $\Phi_f=V_t\ln(\frac{Na}{ni})$ Equation (4)

Oxide voltage $Vox=\frac{qNa\ Wd(max)}{Cox}$ Equation (5)

Depletion width Wd(max)=

$$\sqrt{\frac{2\varepsilon s\varepsilon o\Phi s}{qNa}}$$ Equation (6)

Oxide capacitance $Cox=\frac{\varepsilon OX\varepsilon O}{Tox}$

Main formula to calculate Vt is: $V_t=V_{t\text{-}mos}+V_{fb}$

Where,

$V_{t\text{-}mos}$=ideal threshold voltage (no work function difference between the gate and substrate)

V_{fb}= flat band voltage

The ideal threshold voltage is: $V_{t\text{-}mos}=2\Phi_b+Q_b/C_{ox}$

Where,

$Cox=\varepsilon ox/t_{ox}$

The junction built in voltage: $\Phi b=KT/q\ \ln(Na/n_i)$

Depletion region charge density: $Q_b=\sqrt{2\varepsilon_{Si}qN_A(2\Phi_b+|V_{sb}|)}$

Where,

the substrate bias V_{sb}=0

Thus, the ideal threshold voltage will be:

$V_{t\text{-}mos}$ is positive for nMOS. $V_{t-mos}=2\frac{KT}{q}\ln\frac{N_A}{ni}+\sqrt{2\varepsilon_{Si}N_A2\Phi_b}\frac{1}{\varepsilon_{ox}/t_{ox}}$

The flat band formulas:

Where $\boxed{V_{fb}=\Phi ms-\frac{Q_{fc}}{C_{ox}}}$,

$$\Phi_F=\frac{KT}{q}\ln\frac{Neff}{ni}$$

Φms=work function difference between gate and wafer

Q_{fc}=fixed charge for surface states (given)

$$\Phi ms=-(\frac{Eg}{2}+\Phi b)$$

E_g is the band gap energy of silicon=1.1eV

For silicon band gap energy at room temperature:

So, complete flat band formula: $Eg=1.16-0.704\times10^{-3}(\frac{T^2}{T+1108})$

The entire threshold voltage (V_t) formula:

$$V_{fb}=-(\frac{(1.16-0.704\times10^{-3}(\frac{T^2}{T+1108}))}{2}\pm\frac{KT}{q}\ln\frac{N_A}{ni})-\frac{Qfc}{\varepsilon_{ox}/tox}$$

$$Vt=2\frac{KT}{q}\ln(\frac{N_A}{ni})+\frac{\sqrt{2\varepsilon_{Si}qN_A2\Phi b}}{\varepsilon_{ox}/tox}-(\frac{(1.16-0.704\times10^{-3}(\frac{T^2}{T+1108}))}{2}\pm\frac{KT}{q}\ln(\frac{N_A}{ni}))-\frac{Qfc}{\varepsilon_{ox}/tox}$$

$$\boxed{Vt=Vfb+2\Phi f+\frac{\sqrt{2\varepsilon_{Si}qN_A2\Phi_b}}{\varepsilon_{ox}/tox}}$$

Derivation of Drain Current W.R.T The Thickness Of Dielectric Layer Of SiO_2:

The relation between capacitance, charge and voltage: C=Q/V

Gate oxide capacitance per unit area : $Cox=\varepsilon ox/t_{ox}$

Capacitance per unit length of the oxide : $C=W.C_{ox}$

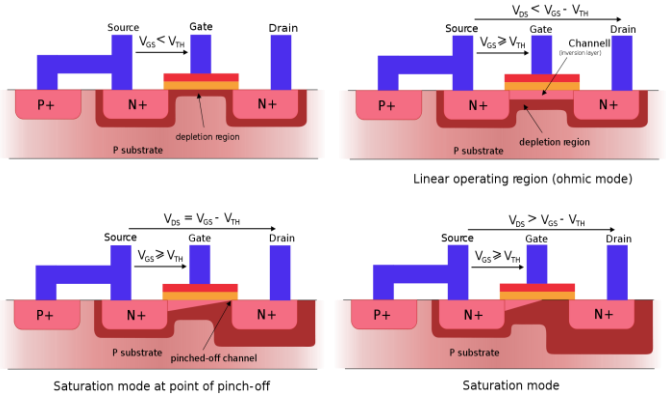

Fig2. Voltages of Different Operating Regions

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The equations for the transistor are obtained in all modes(cut off , triode, and saturation)

Although the voltage applied across the oxide is Vgs, charge does not start collecting at the substrate until inversion occurs , just as in a MOS capacitor. Inversion only occurs when $V_{gs}>V_{th}$, therefore, the charge at the silicon-oxide interface can be described as: $Q=W.C_{ox}.(V_{gs} -V_{th})$.During normal operation, a transistor will have an applied voltage difference between the source and drain ,VDS.

As a result, the voltage between the gate and the oxide decreases towards the positive x direction .The reason is the drain is at a higher potential than the source, thus the potential difference between the gate and the oxide decreases from source to the drain. Thus, charge equation is now:

$$Q = W \times Cox \times (V_{GS} - V(x) - V_{TH})$$

An accurate description of the charge at the silicon-oxide interface as a function of x, the current equation is:

$$I = Qv$$

$$V = -\mu_n E$$

$$V = \mu_n \frac{dv}{dx}$$

$$I_d = W \times C_{ox} \times (V_{GS} - V(x) - V_{TH})\mu_n \frac{dv(x)}{dx}$$

To solve the differential equation both sides integration is done:

$$\int_{x=L}^{x=0} I_d d(x) = \int_{V(x)=0}^{V(x)=Vds} W \times Cox(V_{GS} - V(x) - V_{TH})\mu_n dV$$

$$I_d = \frac{1}{2}\mu_n Cox \frac{W}{L}(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^{\ 2})$$

The maximum current achievable is:

$$I_{d,\max} = \frac{1}{2}\mu_n Cox \frac{W}{L}(V_{GS} - V_{TH})^2$$

Regions of operation: when,

$V_{DS} \le V_{GS} - V_{TH}$ and $V_{GS} \ge V_{TH}$,the transistor is said to be in triode.

$$I_{d,triode} = \frac{1}{2}\mu_n Cox \frac{W}{L}(V_{GS} - V_{TH} - \frac{V_{DS}}{2})V_{DS}$$

$V_{DS} \ge V_{GS} - V_{TH}$ and $V_{GS} \ge V_{TH}$,the transistor is said to be in saturation.

$$I_{d,sat} = \frac{1}{2}\mu_n Cox \frac{W}{L}(V_{GS} - V_{TH})^2$$

When $V_{GS} \le V_{TH}$,the substrate is not inverted and no current can flow,

$I_D=0$.

As per the above equation the drain current is dependent on the mobility, thickness of the oxide layer and the aspect ratio (W/L).If the width of the channel length is increased, the resistivity decreases, drain current increases .Mobility of the electrons is directly proportional to the drain current .If the mobility increases, the time taken by the electron to reach from source to drain decreases. As a result the drain current increases due to rapid movements of electrons.

II. CONCLUSION

In this project aim is to plot graphs between different parameters of La_2O_3 and $HfO_2$and comparative analysis of the features of the graph of both the oxides. The threshold voltage was at first varied with the channel length by keeping the pocket dose constant, then threshold voltage and channel length is varied by changing the pocket dose (doping). Pocket doping varied with channel length .So, the detail study of the pocket doping profile is needed to construct an appropriate modeling of the threshold voltage. For further miniaturization of the device the thickness of the oxide layers were varied with respect to the threshold voltage and drain current and the graph is obtained between these parameters through MATLAB. The silicon dioxide shows larger leakage current, lesser capacitance which leads to lower device current and lesser circuit speed. On the contrary the high –K dielectric material shows lesser leakage current and increased device performance by higher capacitance which enhances device current and speed. La_2O_3 shows that the channel is formed much faster as the charges are induced more easily for small threshold voltage when the oxide thickness is increased and almost constant charges flows from source to drain thus causing larger capacitance .The comparative study shows that the power consumption is reduced to a great extent and device performance is enhanced for La_2O_3 (High K dielectric material) output current also increases.

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ABBREVIATIONS AND ACRONYMS

Q_{GC}= work function difference between gate and channel

Q_{BO}= depletion region charge density (body bias at ground potential)

Q_{OX}= oxide interface charge

C_{ox}=oxide capacitance per unit area

Φ_f(sub)= Fermi potential for (p-type) substrate

Φ_f(gate)= Fermi potential for gate

q=unit electron charge= 1.6 $X10^{-19}$coulomb

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N_A=acceptor doping concentration
ε_{Si}=permittivity of silicon= 11.7 X 8.85 X 10^{-14}F/cm
ε_{ox}=permittivity of oxide=3.97 x 8.85 x10^{14}F/cm
ε_{HfO2}=permittivity of hafnium oxide=19.6 x 8.85 x10^{14}F/cm
t_{ox}=thickness of the oxide
N_{ox}=oxide interface charge density
V_{TO}=zero-bias threshold voltage calculated using the conventional long-channel formula
ΔVto =reduced threshold voltage due to short – channel effect
X_{ds}=depth of the p-n junction depletion region associated with the source
X_{dD}= depth of the p-n junction depletion region associated with the drain
ΔLs =lateral extent of the depletion regions associated with the source junctions
ΔL_D= lateral extent of the depletion regions associated with the drain junctions
X_j=metallurgical junction depth
K= Boltzmann constant=1.38 x10^{-23}J/K
T=Temperature in Kelvin
N_{sub}=substrate doping concentration
N_{pm}=peak pocket doping concentration
N_{eff}=effective pocket doping concentration
L_p=pocket length
N_{sd}=source or drain doping concentration
X=distance across the channel from source to drain
Ψ_s=surface potential
n=electron density
D_n=diffusion coefficient
W=channel width
T_{ch}=effective channel thickness
Φ_{ms}=work function difference between gate and wafer
$V_{t\text{-}mos}$=ideal threshold voltage
V_{fb}=flatband voltage
μ=mobility of electrons
KT/q=0.26mV at room temperature (300K)
K=1.38X10^-23J/K=Boltzmann's constant
N_i= carriers in intrinsic silicon =1.45X10^10cm^3
Φ_f=0.341V=work function difference between the intrinsic potential and Fermi potential
Cox=gate oxide capacitance per unit area
N_{sub}(substrate doping concentration)La_2O_3=5.2x10^{12} cm^{-3}
N_{pm}(peak pocket doping concentration) La_2O_3=
$1.8 \times 10^{13} cm^{-3}$

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