A Survey on Methods of Parallel Concatenation of LDPC Codes

Aswathy G P, Niyas K Haneefa

Abstract— From the time of discovery of Turbo codes, parallel concatenation of codes has become one of the fieriest topics in code theory. In the recent years, there has been a remarkable advancement in LDPC codes and has seen them outshine turbo codes in terms of performance especially in the error floor and higher code rate. On the other hand, fully parallel LDPC decoder for longer block length suffers from prohibitive implementation complexity, due to the pervasive connectivity in the bipartite graph. Subsequently, in order to achieve better performance for longer codes with reduced decoding complexity, different methods for parallel concatenation of LDPC codes were introduced. Parallel concatenation of LDPC codes provides the advantage of breaking an equivalently long and highly complex LDPC code into multiple small and less complex LDPC codes to distribute the encoding and decoding load. This could offer scalability and scope for improving the performance of LDPC codes in practical delay-sensitive and energy-aware applications. This paper gives an overview of different methods of parallel concatenation of LDPC codes.

Index Terms— LDPC, Parallel concatenation, PCGC, Turbo codes.

I. INTRODUCTION

Low-density parity-check (LDPC) codes are a class of linear block codes, first introduced by Robert Gallager in his PhD. Thesis in 1962 [1], [2], [6]. However, these codes were not deployed much, as they were thought to be impractical due to its implementation complexity. Later, these codes were re-discovered by D. MacKay and R. Neal in 1995, after the discovery of Turbo codes by Berrou in 1993. They proved that LDPC codes have very good coding gain performance. LDPC codes are one of the most attractive error-correction codes due to their capacity approaching performance, high degree of parallelism and relatively low decoding complexity. However, the encoding complexity of LDPC codes increases quadratically with block length and will be relatively high for longer block lengths. On the other hand, fully parallel LDPC decoder for longer block length suffers from prohibitive implementation complexity, due to the pervasive connectivity in the bipartite graph. This could limit the use of LDPC codes in delay-sensitive applications. Therefore, in order to achieve better performance for longer codes with reduced decoding complexity, different methods for parallel concatenation of LDPC codes were introduced. With parallel concatenation, the inherent encoding complexity of long LDPC codes are reduced, while achieving an improved coding performance. This paper describes various methods of parallel concatenation of LDPC codes.

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Aswathy G P, PG Scholar, Department of Electronics and Communication Engineering, Mar Baselios College of Engineering and Technology, Thiruvananthapuram, India.

Niyas K Haneefa, Assistant Professor, Department of Electronics and Communication Engineering, Mar Baselios College of Engineering and Technology, Thiruvananthapuram, India.

The paper is structured as follows: In Section II a short overview of Conventional Parallel Concatenated Gallager Codes (PCGC) will be given, followed by a description of Structured PCGC and PCGC with two sets of source bits in Section III and IV respectively. Section V describes PCGC with single encoder. Section VI presents Modified PCGC. After the presentation of PCGC with interleaver in Section VII, Section VIII concludes the paper.

II. CONVENTIONAL PCGC

Parallel Concatenated Gallager Codes (PCGC), [3], [4] is a class of concatenated codes, in which two LDPC encoders are directly concatenated in parallel without using an interleaver between them. Fig. 1 shows the encoder and concatenated codeword structure for Conventional PCGC. The idea behind the introduction of PCGCs was to include turbo-encoding principle in LDPC codes. The complex encoding and decoding of a long LDPC code is broken down into lower complexity encoding and decoding steps, at the same time maintaining the information flow between the component decoders, and reducing any information loss between the decoding steps. The component codes are selected based on the Mean Column Weight (MCW) of the code's parity-check matrix. MCW is the average column weight over all columns in the parity check matrix. It has been found that by choosing low MCW code as the first component code and high MCW code as the second component code, performance is improved.

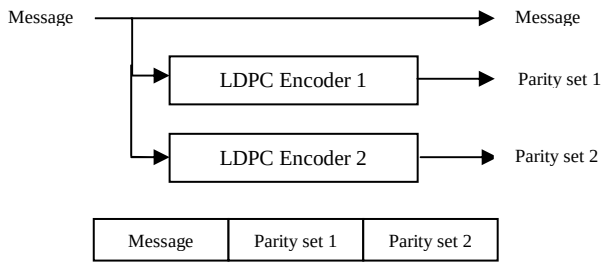

Fig. 1. Conventional PCGC encoder and Concatenated codeword structure [3].

The decoding procedure for PCGCs is similar to that of turbo code decoding, without using an interleaver between the component decoders. Fig. 2 shows the decoder for Conventional PCGC. During decoding, each component LDPC decoder computes the *a posteriori* probability as described in [13] using the sum product algorithm with slight modifications to accommodate the *a priori* (extrinsic) information available from the other component decoder [3].

Decoding of LDPC codes is an iterative process. A super iteration is the process of exchanging information between the two component decoders. A local iteration is referred to one

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complete cycle of the sum-product algorithm performed by the component LDPC decoder. In a super iteration, each component decoder performs a fixed number of local iterations before passing any information to the other component decoder. This process of exchanging information between the component decoders continues until both decoders converge to valid codeword, or a maximum number of super iterations are over. In the latter case, the output from the second component decoder is declared as the best estimate of the transmitted sequence.

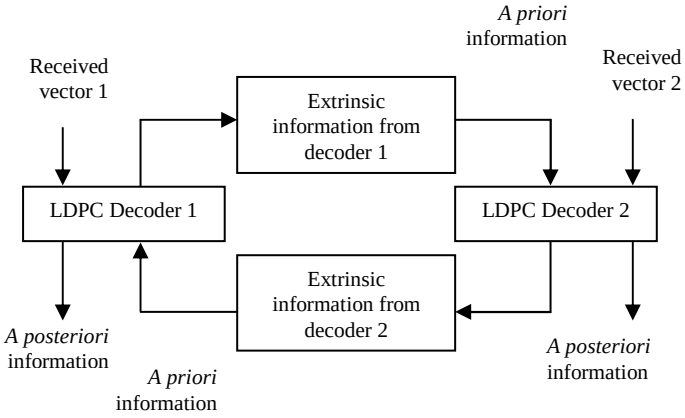

Fig. 2. Conventional PCGC decoder [3].

There are some drawbacks for conventional PCGC. After a fixed number of local iterations in each component decoder, the reliability i.e. log likelihood ratio magnitudes of the systematic message bits (including the error bits) is increased, so it becomes difficult for the next component decoder to correct maximum number of errors. Thus it fails to achieve the coding gain provided by concatenation of codes. Further, when one component decoder performs local iterations, the other component decoder remains idle and exchange of information takes place only after a fixed number of local iterations. Hence decoding delay is more in conventional PCGC. An "extensive computer search" was required to select the component codes with different MCWs. As such, the efficacy of the scheme depends mainly on the complementary behaviours of the individual LDPC codes.

A. Multiple PCGC

Multiple Parallel Concatenated Gallager Codes [7] are a generalization of PCGCs. Fig. 3 shows the encoder for MPCGC. In MPCGC, 'M' distinctive component LDPC encoders are connected in parallel instead of only two component encoders as in conventional PCGC. The parity check matrices of component LDPC codes are constructed randomly based on the selected MCW. While constructing the parity check matrices, the row weights are maintained as uniform as possible. In MPCGC, a very long LDPC code is broken into simple sub codes, so that the overall encoding and decoding complexity is reduced significantly, while at the same time achieves the performance of the equivalent long code. MPCGC also provides an extra benefit in terms of encoding and decoding complexity compared to conventional LDPC. The encoding complexity of conventional LDPC code is quadratic to the block length which is comparatively higher than the sum of the complexities of the individual shorter component codes making up the MPCGC.

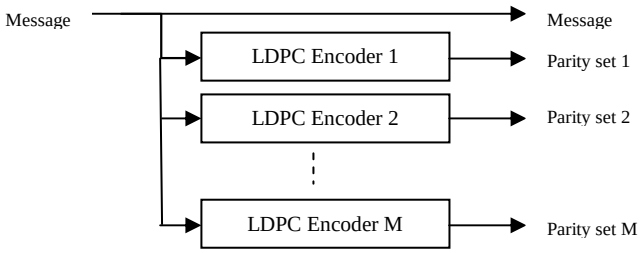

Fig. 3. Multiple PCGC encoder [7].

MPCGC architecture has got greater potential for flexibility in terms of code parameters, as different code rates can be achieved using different subsets of component codes. In order to adapt to different channel conditions, it is also possible to switch to different decoder configurations. This makes the architecture a desirable one for various applications.

In [8], it is observed that LDPC codes with low MCWs outperform LDPC codes with high MCWs (in terms of bit error rate) at low to moderate SNR, while they exhibit low-grade performance at high SNR. MPCGC is designed based on this observation i.e. to combine the strength of low MCW LDPC codes in the low to moderate SNR region, and high MCW LDPC codes in the high SNR region. Design of a good MPCGC relies mainly on choosing the design parameters for its component codes. A combination of component LDPC codes with low, moderate and relatively higher MCWs were to be obtained using "extensive computer search", which is a very difficult task.

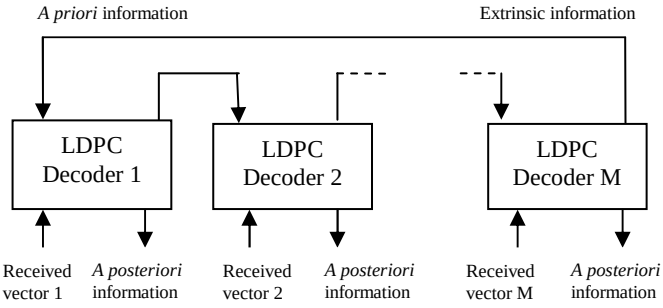

Fig. 4. MPCGC serial decoder [7].

Fig. 4 shows the serial decoder for MPCGC. Decoding is similar to conventional PCGC, except that it is performed using a serial combination of 'M' component decoders. But serial decoding increases the decoding delay. Parallel decoding technique is also evaluated in [7]. Fig. 5 shows the parallel decoder for MPCGC. In parallel decoding, all the 'M' component decoders will be simultaneously performing, so that the decoding delay can be significantly reduced. From the analysis, it was found that at low SNR it is beneficial to increase the number of local iterations and decrease the number of super iterations. While at moderate to high SNR, a few local iterations and more super iterations are recommended [7].

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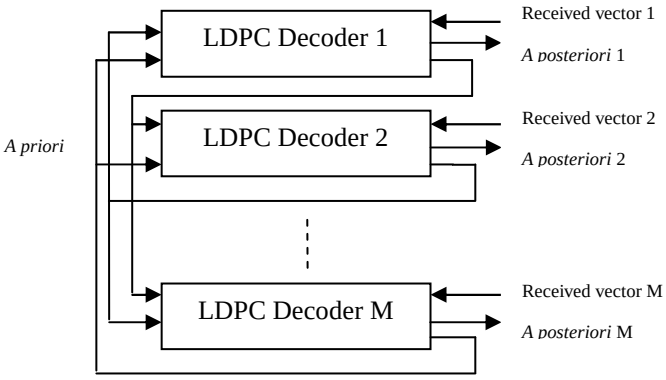

Fig. 5. MPCGC Parallel decoder [7].

The main disadvantage of this technique was that a combination of low, moderate and high MCW LDPC codes were required as component codes. So here also the efficacy of the scheme rested with the complementary behaviours of the individual LDPC codes.

III. STRUCTURED PCGC

For large block lengths, randomly constructed LDPC codes provide excellent bit-error rate (BER) performance. But the memory required to specify the non-zero elements of such a random matrix is a major challenge for hardware implementation. Structured LDPC codes can provide much simpler implementations for decoding and encoding. Girth is an important parameter which characterizes the effectiveness of iterative decoding algorithms for LDPC codes, which determines the number of independent iterations. Girth of LDPC code or parity check matrix, means the length of the shortest cycle in Tanner graph. Cycles especially short cycles (cycles having low girth), in Tanner graph degrades the performance of LDPC decoders, because they affect the independence of the extrinsic information exchanged in the iterative decoding [13]. Therefore, the design of LDPC codes with large girth is of great interest. The main objective of structured LDPC construction methods is to design LDPC codes with a girth as large as possible. In [11], the performance of two structured, half-rate, parallel concatenated LDPC codes, based on Cayley graphs and Graphical models are evaluated. The performance of two concatenated LDPC codes obtained through well-structured procedures with different MCWs are compared with conventional PCGC considering two randomly created component LDPC codes for the same length.

Encoder is similar to conventional PCGC, except that component codes are structured. Decoder follows the same principle as conventional PCGC. Average MCW for structured PCGC is high compared to conventional PCGC. The additional redundancy provided here, only improves the BER performance at high SNR values but actually performs worse than the individual codes at low SNR values. It is observed that the performance of the structured parallel concatenated LDPC codes is similar to that of the random codes. Since the BER performance of the parallel concatenated approach is worse when compared to the performance of the individual codes at low SNR values, it is suggested to assign more iteration to the low MCW decoder if the SNR value of the received signal is low. If the SNR value of the received signal is medium, assign more iteration to the high MCW decoder and assign an even number of iterations to both decoders if the SNR value of the received signal is high. This method is less attractive for long block lengths because, as the length of the individual codes increases the SNR value at which they will be outperformed by the parallel concatenated code is increased. Therefore, it can be concluded that this method is a very good option only for short block lengths and high SNR values. Also it could replace a single LDPC code of the same length.

IV. PCGC WITH TWO SETS OF SOURCE BITS

This scheme has got a much better performance than conventional PCGC, which depend on its architecture of concatenation [9]. In this method, no distinct component code selection is required and the two parity check matrices used are different. Such differences are not characterized in [3], [10] and [11]. Since two different parity check matrices (hence two differently connected bipartite graphs) are used, a natural means of interleaving data between the component decoders is ensured. In this scheme, at the transmitting side, two copies of the source message bits are sent. Because of this, there was no need to remove "channel information" from the a posteriori metrics (unlike conventional turbo schemes), while computing the extrinsic information which is shared between the two component decoders and only the *a priori* information was removed. This is because since two copies of source message bits are sent, the source bit information received by any one component decoder is entirely different and thus independent from the source bit information received by the other component decoder.

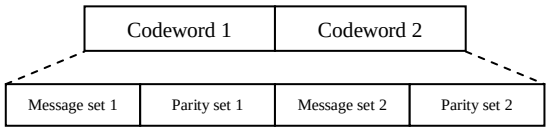

Fig. 6. Concatenated codeword structure for PCGC with two sets of source bits [9].

At the transmitting side, the message bits are duplicated. Each set of message bits are encoded using different generator matrices (corresponding to different parity check matrices), to form two sets of codewords, which are then concatenated. Fig. 6 shows the concatenated codeword structure at transmitting side.This concatenated codeword is modulated using binary phase shift keying (BPSK) and is then sent through the additive white Gaussian noise (AWGN) channel.

Fig. 7 shows the decoder architecture for PCGC with two sets of source bits. At the receiving side of the transmission link, the first set of vectors of the received packet are assigned to first decoder while the second set of vectors are assigned to second decoder. The extrinsic information is shared between the systematic message bits of the two component decoders.

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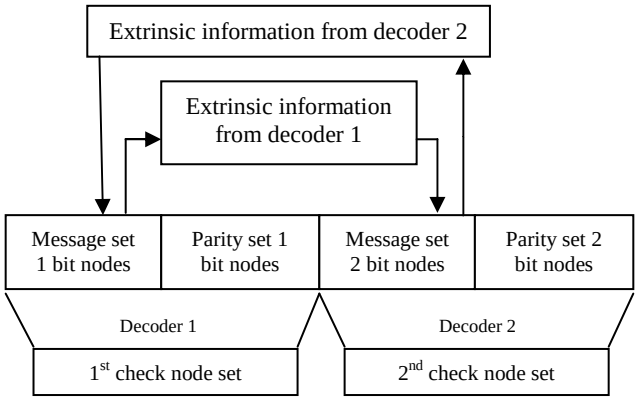

Fig. 7. Decoding architecture for PCGC with two sets of source bits [9].

Decoding procedure is similar to conventional PCGC, except that the source bit information received by any one component decoder is different and independent from that received by the other component decoder.

Here also the decoding delay is more, as when one component decoder performs local iterations, the other component decoder remains idle and exchange of information takes place only after a fixed number of local iterations. Also the need for transmitting the same message bits twice in this scheme is not applicable in low bit rate applications.

V. PCGC WITH SINGLE ENCODER

In PCGC with single encoder [12], only single component LDPC code with MCW >2.5 is used. But the same parity bits corresponding to the message bits are transmitted twice. Fig. 8 shows the encoder and concatenated codeword structure for PCGC with single encoder. Here the encoding complexity is reduced significantly and is much less compared to the other parallel concatenation techniques.

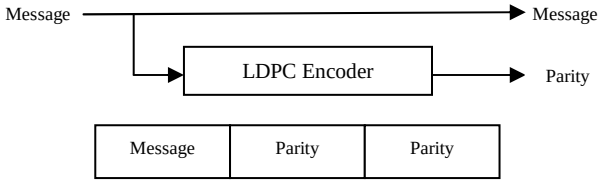

Fig. 8. Encoder and Concatenated codeword structure for PCGC with single encoder [12].

Fig. 9 shows the decoder for PCGC with single encoder. At the decoding side, two component decoders are connected in parallel by using the check nodes, called the interconnecting check nodes. Each interconnecting check node corresponds to one parity-check equation of the corresponding parity-check matrix and an edge joins an interconnecting check node and a bit node of each component decoder if that particular bit is involved in the corresponding parity-check equation. In the first step of super iteration, both component decoders will independently and simultaneously perform one local iteration of the iterative decoding i.e. the intrinsic information from bit nodes are transferred to the check nodes of the corresponding decoder and bit nodes are updated based on the extrinsic message available from the check nodes. In the second step, each bit node of first component decoder is updated (i.e. log likelihood ratio value is modified) by using the updated intrinsic information of the bit nodes of second component decoder and similarly each bit node of second component decoder is updated using the modified intrinsic information of bit nodes of first component decoder through the interconnecting check nodes. This process of super iteration continues until one of the decoder converges to a valid codeword or a maximum number of super iterations are over.

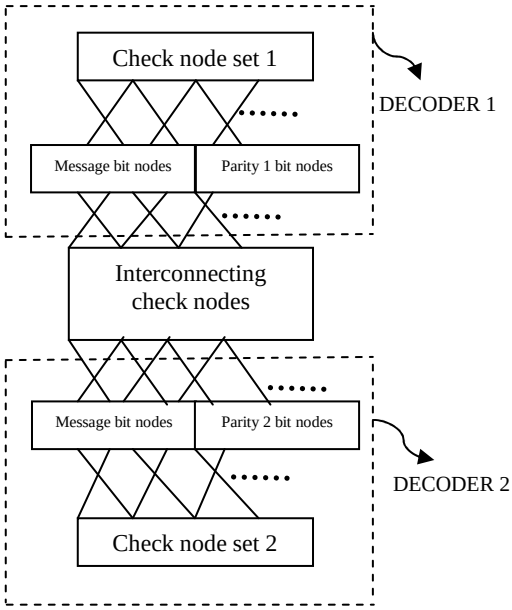

Fig. 9. Decoder for PCGC with single encoder [12].

In PCGC with single encoder, component decoders perform local iteration simultaneously and exchange of information takes place between them after each iteration. Hence, the convergence of codewords for PCGC with single encoder is much quicker than conventional PCGC. To reduce implementation complexity, PCGC with single encoder can make use of the symmetric structure of decoder. The decoder for this PCGC could be replaced with a simple LDPC decoder (defined for the same parity-check matrix), with some additional registers embedded in each variable node. The purpose of these additional registers is to hold the log likelihood ratio values of the corresponding bits in both the codewords, as well as the intermediate values it received from check nodes. Thus the complexity of the PCGC with single encoder (both encoder and decoder) is reduced to half when compared to conventional PCGC.

The disadvantage with this scheme is that even though there is a reduction in the complexity of decoder, it leads to an increased decoding delay. But the decoding delay associated with this PCGC is much less compared to conventional PCGC. On simulation in AWGN channel, it was found that even though there is an improved performance at high SNR region, performance is degraded in low SNR region due to the selected MCW of component code. The performance of this PCGC is not good compared to the performance of the single dedicated LDPC for same block length and rate. Furthermore, repeating the same set of parity bits twice would not provide the required coding gain to achieve the performance of the single dedicated LDPC code.

VI. MODIFIED PCGC

In modified PCGC [14], two different set of parity bits are transmitted for the same information block. One set of parity bits satisfies zero syndrome criteria and another set satisfies

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non-zero syndrome criteria. In order to obtain non-zero syndrome parity set from second encoder, a '1' is added at the start of message block, so that the length of message is one more than that for first encoder. The performance can be slightly increased compared to PCGC with single encoder, due to the increase in minimum distance for the carefully chosen syndrome vector, without any change in complexity of decoder.

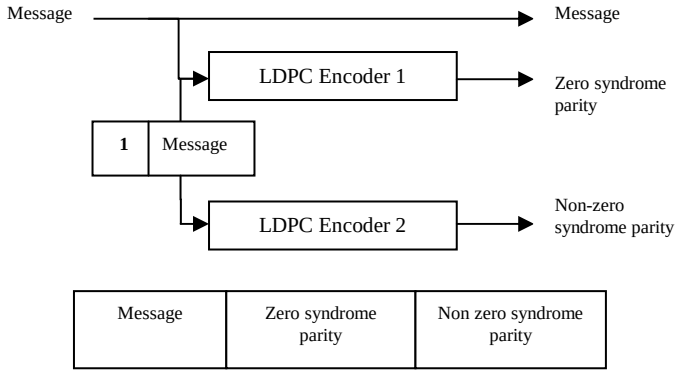

Fig. 10. Modified PCGC encoder and Concatenated codeword structure [14].

Fig. 10 shows the encoder and concatenated codeword structure for modified PCGC. Encoder for modified PCGC consists of a pair of simple LDPC encoders, one for obtaining codeword that satisfies zero syndrome criteria and other for obtaining codeword that satisfies non-zero syndrome criteria.

For decoding, message passing algorithm needed slight modifications to accommodate the non-zero syndrome criteria. Bit flipping algorithm is used for decoding. In the first step of super iteration, decoder will perform a local iteration with codeword satisfying zero syndrome criteria. In the second step, decoder will perform a local iteration with codeword satisfying non-zero syndrome criteria. In the third step, intrinsic information is updated using the extrinsic information that each bit node received from the check nodes. Bit nodes corresponding to parity bits and systematic message bits are updated separately. This process of super iteration continues until one of the decoder converges to a valid codeword or a maximum number of super iterations are over.

The modified PCGC also have some drawbacks. The extrinsic messages received by each bit node during a super iteration are not fully independent and are correlated, which worsens the performance of the iterative decoding. It is because if there is a bit in error, then there is a possibility that the messages received by the bit nodes from the check nodes will be contradictory. So as to have improved performance, all the information received by a bit node has to be independent. Other demerits include its applicability only in Binary Symmetric Channel (BSC) and random selection of non-zero syndrome vector.

VII. PCGC WITH INTERLEAVER

In order to make extrinsic messages received by the bit nodes in PCGC to be independent, an interleaver can be used. In PCGC with interleaver [14], use of an interleaver will make the parity equations entirely different and hence bit nodes will receive totally independent messages, thus improving the performance. Fig. 11 shows the encoder and concatenated codeword structure for PCGC with interleaver. Here, the first encoder gives parity set for message bits while the second encoder provides parity set for interleaved message bits. Both parity bits sets satisfy zero syndrome criteria. A random interleaver is used which randomly permutes the message bits and is of the same length as that of the message block. The main drawback is that complexity will be increased due to the use of interleaver.

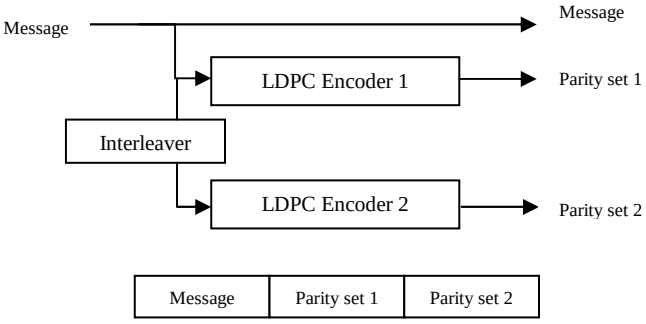

Fig. 11. Encoder and Concatenated codeword structure for PCGC with interleaver [14].

Fig. 12 shows the decoder for PCGC with interleaver. A simple LDPC decoder is used to decode both the codewords. It also consists of a register block, a random interleaver and a de-interleaver.

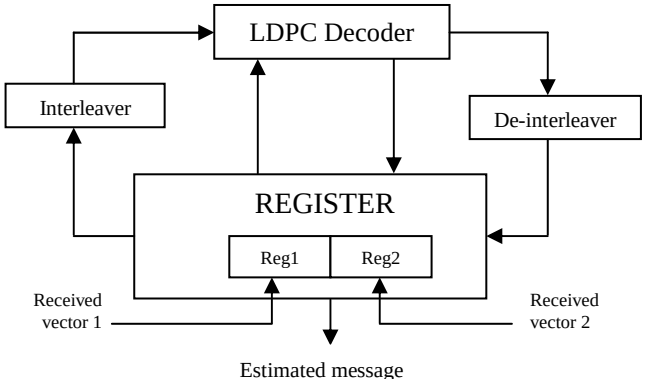

Fig. 12. Decoder for PCGC with interleaver [14].

First, the codewords (de-multiplexed received vectors) are stored in a register block with two sets of registers Reg1 and Reg2. These registers are used to store intrinsic information and total extrinsic information for each bits of corresponding codewords. Decoder outputs the total extrinsic message for each bit after a local iteration. Decoder is connected directly as well as through interleaver and de-interleaver to register block. De-interleaver does the reverse operation of interleaver. Complexity and decoding delay will be more compared with other techniques due to the presence of interleaver and de-interleaver. Decoding delay can be reduced by using parallel set of decoders.

Bit flipping algorithm is used for decoding. In the first step of the super iteration, decoder performs a local iteration with first codeword and the total extrinsic information is sent back to the Reg1 of register block. The intrinsic information of message bits and parity bits are taken directly to decoder and total extrinsic information of the message bits and parity bits are transferred directly to the Reg1. In the second step of the super iteration, decoder performs a local iteration with

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permuted codeword and the total extrinsic information is sent back to the Reg2 of register. Here the intrinsic information of message bits are taken to decoder through interleaver and that of parity bits are taken directly. While the total extrinsic message corresponding to parity bits is sent back through the direct path and the total extrinsic message corresponding to message bits is sent back through the de-interleaver. In the third step of the super iteration, intrinsic information in the register block (Reg1 and Reg2) is updated using the total extrinsic information received from the decoder. But the parity bits and the systematic message bits are updated separately. This process of super iteration continues until one of the decoder converges to a valid codeword or a maximum number of super iterations are over.

PCGC with interleaver showed improved performance compared to modified PCGC in BSC [14]. The factor that improved the performance of PCGC with interleaver in AWGN channel (especially in error-floor or high SNR region), is the indirect increase of column-weight. This is because there is an indirect increase in the number of check nodes connected to each bit node without changing the number of bit nodes connected to each check node. Thus, this concatenation scheme gives the performance as good as dedicated LDPC but with an increased complexity due to deployment of an interleaver. Hence with PCGC with interleaver, the implementation problem associated with longer block length iterative decoder is solved without much compromise in the performance.

VIII. CONCLUSION

LDPC codes are well-known error-correction codes for its capacity approaching performance and other inherent advantages. However, the major shortcoming with the LDPC codes in the current scenario is its implementation complexity especially for longer block length. Even though LDPC codes outperforms Turbo codes, in most of the practical applications, LDPC codes are not still preferred over the Turbo codes because of this limitation. Hence, with these parallel concatenation methods, the problem of implementation complexity associated with longer block length LDPC had been reduced significantly. The parallel concatenation scheme with interleaver is better than the existing schemes in terms of performance. However, the complexity is much high for this scheme due to the presence of interleaver.

REFERENCES

1. R. Gallager, “Low-Density Parity-Check Codes,” IRE Transaction on Information Theory, vol. IT-8, pp. 21–28, Jan. 1962.
2. D. J. C. MacKay and R. M. Neal, “Near Shannon limit performance of low density parity check codes”, Electronics Letters, vol.32, pp.1645-1646, 1996.
3. H. Behairy and S. C. Chang, “Parallel Concatenated Gallager codes”, Electronics Letters, vol. 36, no. 24, pp. 2025 -2026, Nov. 2000.
4. H. Behairy and S. C. Chang, “Parallel Concatenated Gallager Codes for CDMA Applications”, Proceedings of IEEE GLOBECOM’01, San Antonio, TX, pp. 1002-1006, 2001.
5. H. Behairy and S. C. Chang, “Analysis and design of Parallel Concatenated Gallager Codes”, Electronics Letters, vol. 38, no. 18, pp. 1039- 1040, Aug. 2000.
6. D. J. C. MacKay and R. M. Neal, “Near Shannon limit performance of low density parity check codes,” Electronics Letters (reprint with printing errors corrected), vol.33, pp.457-458, Mar.1997.
7. Hatim M. Behairy and Mohammed Benaissa, “Multiple Parallel Concatenated Gallager Codes: Code Design and Decoding Techniques”, IETE Journal of Research, vol: 59, issue: 6, page no: 659-664, Nov-Dec 2013.
8. H. M. Behairy, “Dual Mode PCGCs for Advanced Wireless Communications Networks”, Proceedings of IEEE International Design and Test Workshop, IDT 2007, Cairo, Egypt, Dec. 2007.
9. P. C. Catherine and K. M. S. Soyjaudah, “Parallel Concatenation of LDPC codes with Two Sets of Source Bits”, IEEE Proceedings of International Conference on Emerging Trends in Engineering & Technology, page no: 112-115, 2011.
10. J. C. Serrato and T. O’Farrell, “Parallel Concatenated Gallager Codes using Euclidean and Projective Geometry LDPC Codes”, The Annual London Conference on communications (LCS 2004), University College London, UK, September 2004.
11. J. C. Serrato and O’Farrell, “Structured Parallel Concatenated LDPC codes”, The Annual London Conference on communications (LCS 2006), University College London, UK, September 2006.
12. R. Pravin Kumar and Rakhesh Singh Kshetrimayum, “An Efficient Methodology for Parallel Concatenation of LDPC codes with reduced complexity and decoding delay”, IEEE Proceedings of the National Conference on Communications (NCC), page no: 1-5, February 2013.
13. D. J. C. MacKay, “Good error-correcting codes based on very sparse matrices,” IEEE Transaction on Information Theory, vol. 45, no. 2, pp. 399–431, Mar. 1999.
14. R. Pravin Kumar, “Parallel Concatenation of LDPC codes and its applications”, M. Tech. thesis, Department of Electronics and Electrical Engineering, IIT Guwahati, India, April 2013.

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