International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-5 Issue-4, April 2016

FPGA Implementation for Integrated Circuit Technology Tester

Suhas S, Abhishek Joshi, Ravi Srinivas, Nagarjun C S

***Abstract*—Integrated Circuits have dominated every walk of life in the present world. In this Integrated Circuit era, the need of testing of ICs has become the need of the hour. The implementation and fabrication of new ICs on a daily basis have brought testing to new heights. Albeit these requirements, not many efficient, cheap and readily available testing solutions have been realized. In the following paper, a simple yet highly effective solution to various testing concerns of digital circuits or ICs along with its implementation has been brought out. The real time results got are validated and are readily available for verification of the design under test.**

***Index Terms*—Digital designs, Field Programmable Gate Array [FPGA], Testing**

I. INTRODUCTION

The present days have seen an increase in the usage of Integrated circuits in day to day life. The conversion of sand to supremely useful and utilizable Integrated Circuits or ICs has created a revolution in this world. In almost every field, ICs play an irreplaceable role and our lives today will not be imaginable without these. This exponential increase in demand has resulted in a tremendously large design, speed and power variants among ICs. New designs are created very frequently and fabricated, but while doing so, we must still consider the need to understand their capabilities. While the specifications of the IC are to be kept in mind while fabricating, the testing of ICs are an important aspect.

Testing of ICs can be a costly and lengthy procedure but cannot be overlooked as it is one of the most crucial steps in the making of a marketable and sellable IC. Not only new designs, but, even in the industry or institutions it becomes necessary to check the proper functioning of existing and used ICs. The procedure of testing may not be the same for different ICs and it becomes very tiring to alter an entire setup per IC. Manual verification of ICs is time consuming and becomes cumbersome, which results in the requirement of a single testing setup. The implementation of the test setup using a single FPGA is discussed in the paper below where reduction of complexity and cost is achieved without compromise on reliability.

FPGAs [Field Programmable Gate Arrays] are commonly used devices. Their applications vary over a large degree and are used extensively in a number of fields from defence, military, satellite communication and so on. The easy availability and lower cost when compared to top end testing equipment make FPGA an ideal choice for this purpose of testing. Their versatility can be used for the implementation of a testing circuit as described in this paper. Being readily available in almost all places of importance of testing, FPGAs have been best suited for this purpose. The Xilinx software used to code these FPGAs provides good platform to interface between the user and the FPGA. Even without actual connection of the FPGA hardware, using simulation, the outputs can be verified. The Xilinx software is coded in Verilog Language, as Verilog is a user friendly language [5]. The synthesis of the modules along with the generation of the necessary data is considered for testing the digital IC.

II. BLOCK DIAGRAM AND EXPLANATION

A. Pseudo Random Number Generator

A Pseudo-Random number Generator is a one which is used to generate the number randomly, the technique which is used is the Linear Feedback Shift Register (LFSR), a linear feedback shift register is a sequential circuit, where the bits in the register gets shifted linearly according to the global signal element called clock, whereas the MSB and LSB will be operated using XOR operator and the result of XOR operation will be fed into the MSB and all the elements will be shifted. The fig (1) shows the complete block diagram of IC tester.

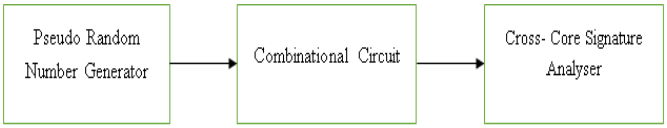


Fig (1) Block Diagram of IC tester

The basic block diagram consists of a Pseudo Random number generator using a Linear Feedback shift register (LFSR) is shown in fig (2).

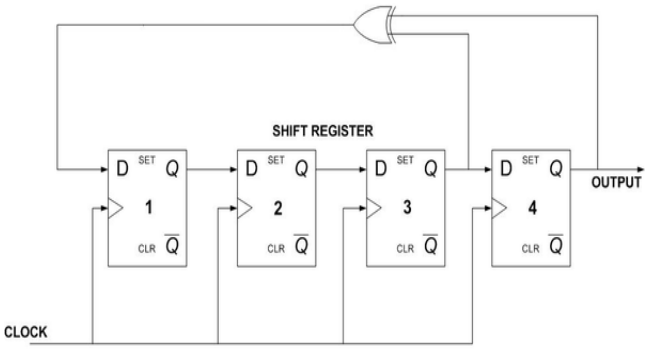


Fig (2)- Linear Feedback Shift Register

Manuscript published on 30 April 2016.
* Correspondence Author (s)
Suhas S, Student, Department of Electronics and Communication, RNSIT, Bangalore, India.
Abhishek Joshi, Student, Department of Electronics and Communication, RNSIT, Bangalore, India.
Ravi Srinivas,Student, Department of Electronics and Communication, RNSIT, Bangalore, India.
Nagarjun.C.S, Student, Department of Electronics and Communication, RNSIT, Bangalore, India.

An LFSR is a circuit consisting of D-flip flops cascaded to form a shift registers circuit whose output is fed back using XOR logic. It is a shift register whose input bit is a linear function of its previous state; here we are using the circuit in which the seed values are the function of XOR gate. Since the output of the XOR gate is fed back as input to the first stage the circuit produces random numbers. The numbers generated in this way show high statistical randomness, hence this LFSR can be called as pseudorandom number generator. LFSR is a shift Register when clocked advances the signal through the next higher set of registers [1]. The main advantage of LFSR especially in the use of FPGA is the test pattern generation randomly [2] .Consider a four bit LFSR as shown in the fig. 2. If the initial seed is considered as 1, during first clock cycle the first D – flipflop sets the output. Remaining three flip flop output will be reset (zero) value because of zero seed value. Hence the random number generated would be '1000'. Here the initial value given should not be '0' for the occurrence of random number generation. If the initial seed value given is zero then the output of all of the flip flops remains '0' and hence does not produce random numbers. Hence, anyone of the 2n values must be given as the initial seed value so that random numbers are generated. The output of the LFSR is fed as input to any digital or analog circuit; here the application used is for any combinational circuits. LFSR can be used to reduce the effect of fault coverage on desired circuits [3]. The added advantage of LFSR is the binary pattern generation for Circuit Under Test (CUT) [4].

B. Combinational Circuit

The combinational circuit refers to a digital logic circuit consisting of a number of logic gates. The combinational circuit can be of any type like 2-bit multiplier, 2-bit ripple carry adder, 4 bit subtractor, 16-bit parallel adder or 32-bit vedic multiplier etc. In the design a 2-bit multiplier and a 2-bit ripple carry adder is considered for analysis. Any binary circuit that is desired to be tested may be placed here.

C. Cross- Core Signature Analyzer

The cross core signal analyzer is essentially a comparator. It compares the input and the actually desired output for proper functioning.

III. Analysis and Testing for 2-bit Multiplier

A 2-bit multiplier is a combinational circuit with 4 inputs and 4 outputs; block diagram of a 2-bit multiplier is shown in fig (3).

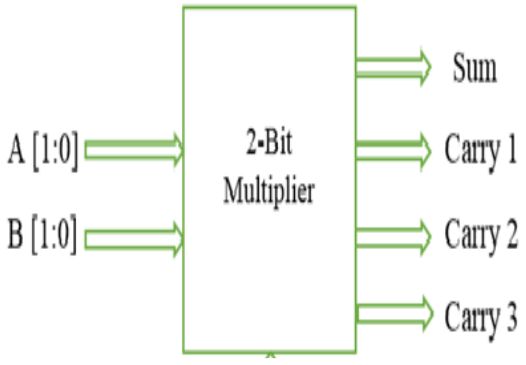


Fig (3) – BD of 2-bit multiplier

The truth table of the same is as presented in Table (1).

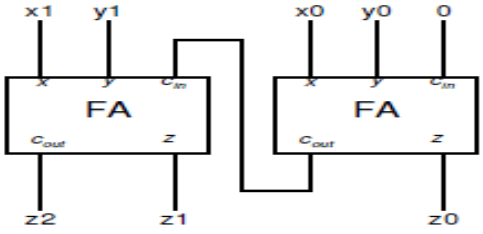
TABLE (1): LOOK-UP TABLE OF 2-BIT MULTIPLIER

a0	a1	b0	b1	carry3	Carry2	carry1	sum
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Here the inputs are represented as A [1:0] i.e.a0 and a1, B [1:0] i.e. b0 and b1 respectively. The outputs are sum, carry1, carry2 and carry 3 respectively. Here the 2 inputs A and B gets the input from the pseudo random number generator, those inputs will be fed to the multiplier and the output will be generated accordingly. The generated output will be compared with the actual output stored in the look up table. The comparison operation will be done by cross core signature analyzer. In its comparison if the actual output matches exactly with the generated output then the gate is said to be non-faulty and even if there is a one bit mismatch then the gate is said to have a fault.

IV. Analysis and Design for 2-bit Ripple Carry Adder

A ripple carry adder is a combinational circuit where in which the carry out of the full adder will be fed as an carry-input to the next higher full adder. The block diagram of a 2-bit ripple carry adder is shown in fig (4).



Fig(4)- Ripple Carry Adder Block Diagram

In the block diagram we can see that there are 2 inputs to each of the full adder indicated as 'FA' which is (x0, y0) and (x1, y1) respectively. The outputs are indicated as z0, z1 and z2 respectively. Here 'z0' is the sum value of the first full adder and from the figure 4 the Cout of first full adder is fed as an carry-input to the second full adder. Then 'z1' will be the sum value of second full adder and the final carry out of second full adder is indicated as 'z2'.

Here the inputs X and Y will obtain the values from the pseudo-random number generator and these values will be fed to ripple carry adder circuit.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

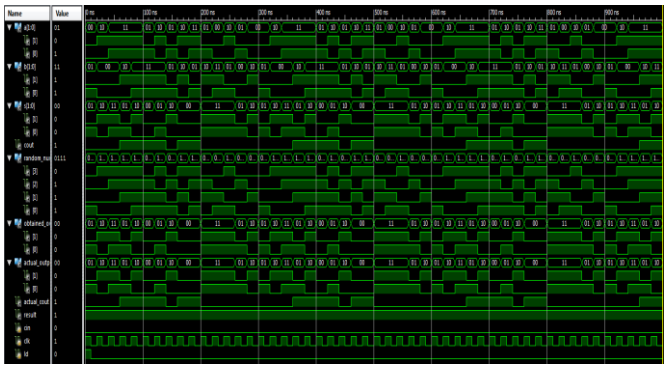
The circuit will generate the appropriate result according the input values and designing functionality of the circuit. The output generated from the circuit will be compared with the look up-table of the ripple carry adder in the cross-core signature analyzer. The look up table of the ripple carry adder is shown in the table (2) below.

Table 2:Look-Up Table of 2-Bit Ripple Carry Adder

Input			Output	
A	B	Carry in	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

V. RESULTS

The simulation of the In the schematic diagram of a ripple carry adder, a and b are the inputs with a vector size of [1:0], the sum is represented as 'S' with the same vector size. Initially carry-in 'Cin' is set 0 and in the second stage 'Cout' from first stage as indicated in the figure (5) will provide the input to second stage of 'Cin'. The random number is indicated 'random number' which provides the random value to the circuit. The 'obtained output' is the output generated from the circuit and the 'actual_output' is the look-up table of the 2-bit ripple carry adder. The 'actual_output' is compared with 'obtained_output', if both of them are equal then 'result' is 1 otherwise the 'result' is 0. When 'result' is 1 then the gate is non-faulty and when 'result' is 0 then the gate is faulty.



Fig(5): Simulation Waveform for Ripple Carry Adder

The Representation and the overall operation of 2-bit multiplier is similar to that of 2-bit ripple carry adder. The simulation is as shown in fig (6).

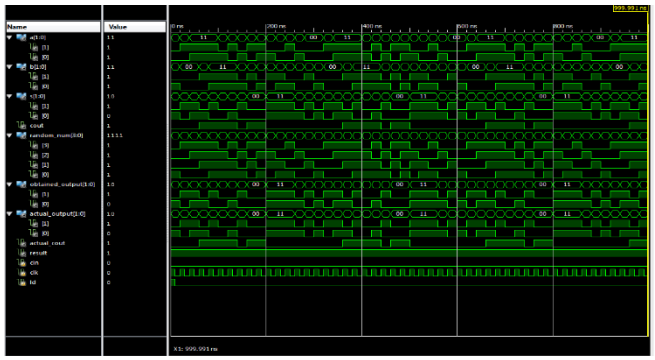


Fig (6) – Simulation Waveform for 2- bit multiplier

VI. CONCLUSION AND FUTURE SCOPE

IC industry is dominating the present day digital world, the booming world of microprocessor is largely due to integrated circuit technology. As we are using the IC in every walks of our daily life it becomes important to test and verify the IC which is acting as a solution to many problems in the real time environment. Here an effective solution for testing of the IC has been described, where the concept of Linear Feedback Shift Register (LFSR) is employed which generates a random number of any given length of the bits. The random number of bits which are generated are fed as an input to the designed combinational circuit, the combinational circuit provides an output according to its design for the generated input. The output of the combinational circuit is compared with the actual output by the cross-core signature analyzer, based on the comparison we can determine whether the gate of an IC is fault or fault free. As digital IC technology plays a very important role right from low-level academic application to high-end space level application. Therefore the testing cannot always be restricted to combinational circuit design hence there is a high level importance for sequential level design. For the testing and validation purpose we are employing pseudo-random number technique using LFSR that can also be tried and achieved through other methods such as T-flip flop technique. As testing for IC cannot be solved for one or two problems there exists a multitudinal problems which needs to be solved through various other methods such as data acquisition technique for structural IC testing can also be employed.

ACKNOWLEDGMENT

The Authors like to thank Mrs. Sangeetha B G, Assistant Professor, RNSIT, Bangalore for her valuable guidance and support.

REFERENCES

1. Md. Fokhrul Islam, M. A. Mohd. Ali, Burhanuddin Yeop Majlis, " FPGA Implementation Of An LFSR Based Pseudorandom Pattern Generator For MEMS Testing", International Journal of Computer Applications (0975 – 8887) Volume 75– No.11, August 2013
2. R. V. PrasadaRao, N. A. Varaprasad, G. S. Babu and C. M. Mohan, "Power Optimization of Linear Feedback Shift Register for Low Power BIST Implemented in HDL", International Journal of Modern Engineering Research (IJMER), Vol. 3, Issue. 3, pp. 1523-1528 (2013).
3. C. R. Reddy, S. Zilani and V. Sumalatha, "Low Power, Low-Transition Random Pattern Generator", International Journal of Engineering Research & Technology (IJERT), Vol. 1, Issue 5 (2012).
4. A. Jutman, A. Tsertov and R. Ubar, "A tool for Advanced Learning of LFSR-Based Testing Principles", Baltic Electronics Conference, 2006 International.
5. Nazeih.M.Botros "HDL Programming Using VHDL and VERILOG", John Weily India, 2008.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)