

FPGA Based 12-Tuple Fast Packet Classification IP Core for SoC Design

Adnan Hussein Ali, Begared Salih Hassen, Aassia Mohammed Ali Jassim

Abstract— Due to increased demand for the speed of communication over Internet. Packet header analysis and classification needs to be performed at same speed in network devices to provide Quality of Service (QoS). As network speed is increasing quickly, high speed packet classification is required at wire speed. In this paper, we propose a novel FPGA based pipelined architecture intended for 12-tuple packet classification on gigabit networks such as 1G/10G/40G/100G. Our solution also enables wire speed packet classification which can be used in Ethernet based SoC designs. It takes one clock cycle to classify the packet after arrival of required information. The proposed method has been designed and synthesized on FPGA using VHDL and can be reused in powerful high speed Ethernet based communication devices. The architecture is optimized for high speed processing and consumes only small amount of FPGA resources. More than 85% throughput can be achieved.

Index Terms—IP, FPGA, Packet Classification, Router, SoC.

I. INTRODUCTION

Computer Networking is any set of computers or devices connected to each other so as to communicate or exchange data. For a network to function, the devices are interconnected through routers at various places. Routers are generally known as intermediate systems, which operates at the network layer of the OSI reference model, routers are devices used to connect two or more IP networks or a LAN to the Internet. The router is responsible for the delivery of packets across different networks. Routers filter out network traffic by specific protocol rather than by packet address. Routers also divide networks logically instead of physically. An IP router can divide a network into various subnets so that only traffic destined for particular IP addresses can pass between segments. Network speed often decreases due to this type of intelligent forwarding. Such filtering takes more time than that exercised in a switch or bridge, which only looks at the Ethernet address. However, in more complex networks, overall efficiency is improved by using routers. Routers are categorized into four types: Workgroup routers, Enterprise routers, Edge routers and Core routers. Workgroup routers connect closely located machines. Enterprise routers connect machines as well Workgroup routers. Edge routers connect the local area network (LAN) to the wide area network (WAN). The last type of routers is the Core routers and they sit inside the WAN. It is the responsibility of the router to

deliver those packets in a timely manner. The effectiveness of internetwork communications depends, to a large degree, on the ability of routers to forward packets in the most efficient way possible. Packet classifiers are essential components of many network router utilities, including security services like firewalls and packet filters. A packet classifier inputs a list of rules and each rule is specified based on multiple fields in the packets. IP router is a basic building block of IP data communication networks as shown in figure 1. Its primary role is to forward packets based on their content, specifically header data at the beginning of the packets. As part of this forwarding operation, packets are classified, queued, modified, transmitted, or dropped. Each router performs a forwarding decision on incoming packets to determine the packet next-hop router based on specific rules. Additionally, an IP router may also choose to perform special processing on incoming packets as described earlier by network administrator.

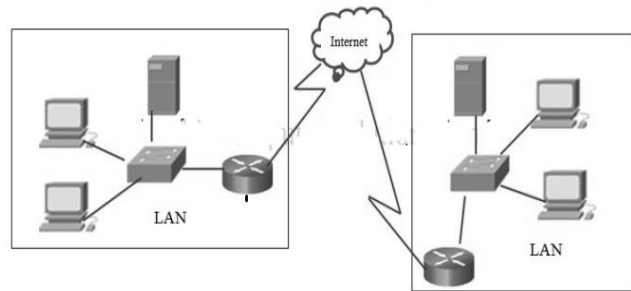


Figure1. Router in network

II. LITERATURE SURVEY

Packet classification has received much attention and continued to be an important topic in design of next generation IP network. Packet classification is an enabling function for network applications, such as (QoS), security, monitoring, and multimedia communications and found bottleneck in high performance routers. In order to classify a packet into a particular flow, each incoming packet needs to be determined the output port it should be sent to and the action it should be taken. Unlike the IP lookup problem, packet classifiers in routers need to compare multiple header fields of each incoming packet with a set of rules to determine which action should be applied, for example, acceptance or denial. In a typical IP based network, the traffic is heterogeneous and consists of multiple applications and utilities. Many of these applications are unique and have their own requirements and are to be met. These requirements are easy to meet Local Area Network (LAN) due to availability of huge bandwidth and usually are a challenging to meet same requirements on the WANs due to bandwidth constraints.

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Thus, there is need of traffic management on the WANs by properly prioritizing different applications across the limited WAN bandwidth and ensure that these requirements are met. In general, packet classification on multiple fields is a difficult problem. Hence, researchers have proposed a variety of algorithms. Classification of different type's traffic is only solution to identify different applications and protocols that exist in a network to improve the network performance. The packet classification is the vital part mechanism that leads to create many networking services in the internet as firewall packet filtering and traffic accounting [7]. So the packet classification is in need to enables many networking services in the network. Typically, once the packets are classified as per application or protocol will help the router to determine appropriate service policies to be applied for those traffic process at wire speed[7][22][23].

Packet classification is very important task handled in design of next generation IP routers. There is continues research in this field across the globe. Various Algorithms were proposed. In this section we have discussed some important algorithms. The design of domain specific processors that require high performance, low power and high degree of programmability is the bottleneck in many general processor based applications. General purpose processors cannot provide wire speed performance for Packet processing and analysis [1] [2].

A continuously growing number of network appliances are deploying packet classifiers to implement QoS, security, traffic engineering functionalities. As a consequence, in the last years several authors have proposed novel algorithms to achieve better results in terms of classification time and memory consumption ,Researchers have proposed many classification methods such as Tuple Space Search (TSS), Set Pruning Multi-Bit Tree (SPMT), Ternary Content Addressable Memories (TCAMs), RFC (Recursive Flow Classification), Fat Inverted Segment tree (FIS) ,Cross Producing and Bitmap-intersection[3][4][8].

Due exponential demand growth of Internet traffic, network bandwidth and Internet based applications rise problems of performance, flexibility in network traffic analysis. The survey shows that Flexibility can be achieved through the programmable devices like General purpose processors and performance can achieve through hardwired solutions like Field Programmable Gate Arrays. While General purpose processors can't achieve wire speed performance however with FPGA technology designed to address the performance and flexibility problems [6]. The FPGA has become an attractive option for implementing real time network processing engines. Although, multi-dimensional packet classification is a saturated area of research, little work has been done using FPGAs. Developing FPGA packet Analysis which can receive the packets processes the packets and forwards the packet with wire speed while utilizing the maximum network bandwidth.

Packet processing is the evolving technology of Internet and is usually performed with fixed function custom made ASIC chips. As IP communication protocols evolve rapidly, there is increasing interest in adapting features of the processing over time and, since FPGA is the preferred way of expressing complex computation in pipeline, we are interested implementing FPGA based platform to execute

packet processing software with the best possible throughput. Because FPGAs are widely used in network equipment and they can implement processors, we are motivated to investigate executing packet processing on directly on the FPGAs [1][8]. Our goal is to allow multiple pipeline execution in an FPGA to reach a higher aggregate throughput than commercially available shared memory soft multiprocessors We study a number of processor pipeline organizations to identify which ones can scale to a larger number of execution threads and found FPGA based packet processing provide compact IP cores with high throughput. FPGA based packet processing technology reduces development costs and offers the possibility of reconfiguration. Especially changing hardware behavior during product life cycle enables a long lifetime of network devices [9] [20][21][22].

It is relatively simple to perform packet classification at high speeds using excessively large amounts of storage, or at low speeds with small amounts of storage. When matching multiple fields simultaneously, theoretical bounds show that it is difficult to achieve both high classification rate and modest storage in the worst case. In this paper we surveyed different algorithm proposed by various authors. Overall study shows that real packet classification algorithms onto Hardware based pipeline architectures appears to be a promising alternative in future for packet classification

In this research we have proposed simple, effective and high speed packet classification architecture which will take maximum one clock cycle of rate of communication speed to classify the packet based on tuple rule set.

III. IMPLEMENTATION METHODOLOGY

A main motivation for this research came from telecommunication equipment providers interested in the use of FPGA technology to provide high-performance. The FPGA has become an attractive option for implementing real time network processing engines. Although, multi-dimensional packet classification is a saturated area of research, little work has been done using FPGAs. Developing FPGA packet Analysis which can receive the packets processes the packets and forwards the packet with wire speed while utilizing the maximum network bandwidth[7][18].

The proposed 12-tuple packet classifier architecture is capable of finding source MAC ID, Destination MAC ID, classify various type field such as IP type, VLAN, MPLS, ARP and IPv6 datagram. In IP field it classifies IP protocol such as TCP, UDP, ICMP and GGP etc. We have implemented our proposed architecture in VHDL and synthesized. Figure 2 view the top level of packet classifier SoC architecture and the RTL view is shown in figure 3 and 4. The proposed Packet Classifier SoC architecture consists of three main blocks as follows:

- 1) Packet Processor.
- 2) Tuple Look table.
- 3) Tuple Comparator logic

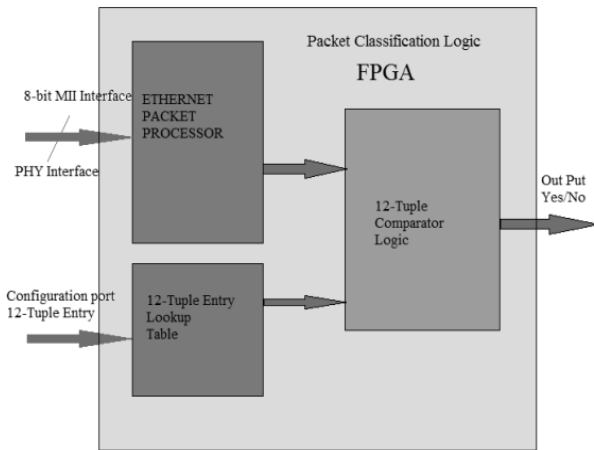


Figure 2. Packet Classifier SoC architecture

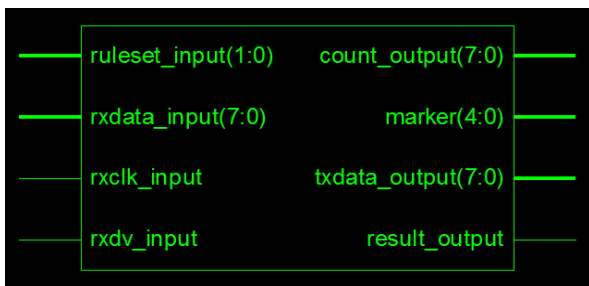


Figure3. RTL View of Packet Classifier

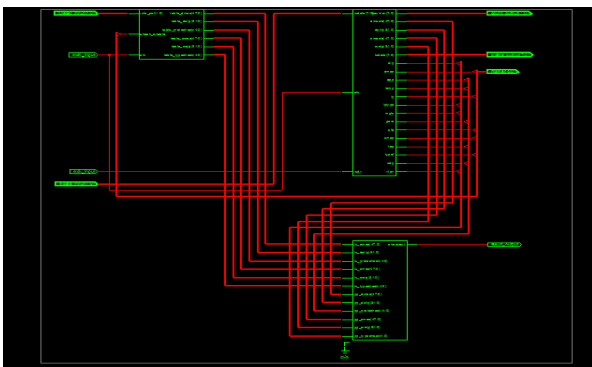


Figure 4. RTL View of Packet Classifier with three blocks interconnected.

1) Packet Processor.

Packet processor is the main functional block for packet classifier. It accepts 8-bit MII data through PHY Chip. The RxDv signal indicates that frame has arrived. The Ethernet frame arrives 8-bit at each rising edge of RxClk. The incoming data is stored and processed. The packet processor handles the break down and analysis of incoming packets, the generation of markers and extraction of sourceMAC ID, destination MAC ID and source ip and destination ip. It handles the Preamble+sfd, Link (Ethernet, ARP, VLAN, ipv6 datagram, MPLS), Internet (IPv4,ICMP), and Transport (UDP layers (TCP/IP also available)). The Ethernet processor uses a proprietary micro coded digital logic to process the incoming packets at the rate the clock speed. The markers are connected for handling of automated response packets. Each packet processor contains a large 50 byte entry for storage and high-speed search of the possible packet tuples as shown in figure. The a table contains the two MAC address, VLAN, MPLS, ARP,IP and two IP

address and TCP,UDP and ICMP port. Simulation result of packet processor is shown in figure 5.

2) Tuple Look Table

In this paper we have proposed in-built tuple look up table in the architecture consist of rule set specifying type field, protocol field and MAC ID and IP address are stored. Packet classifier will classify the incoming packet based on this information.

3) Tuple comparator

Tuple comparator uses comparator for verifying rules set by user with the extracted information from incoming packet.

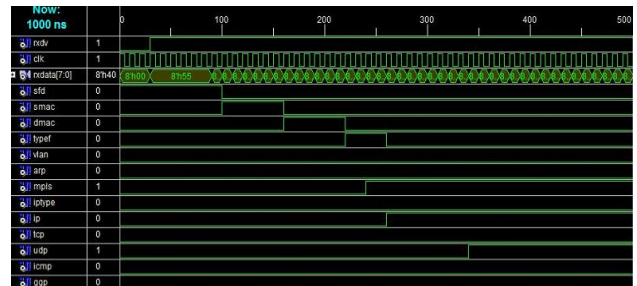


Figure5. Simulation Result

IV. SYNTHESIS REPORT

We used Xilinx 3s1600 FPGA to design Packet classifier IP core for SoC. Xilinx ISE 14.2 tool is used for compilation and synthesis. Table 1 shows the synthesis report.

Table 1: The synthesis report

Macro Statistics	Resources
# ROMs	1
4x170-bit ROM	1
# Adders/Subtractors	3
11-bit adder	1
32-bit adder	2
# Registers	188
11-bit register	1
32-bit register	2
5-bit register	2
8-bit register	2
# Comparators	6
32-bit comparator equal	2
48-bit comparator equal	2
5-bit comparator equal	2
Flip-Flops	280

V. CONCLUSION

This paper has introduced a novel FPGA based pipelined architecture for a packet classification for high performance gigabit packet processing systems. To ensure flexibility and guaranteed full link utilization over the network speed. The proposed a novel FPGA based pipelined architecture intended for 12-tuple packet classification on gigabit networks such as 1G/10G/40G/100G. Our solution also enables wire speed packet classification which can be used in Ethernet based SoC designs. It takes one clock cycle to classify the packet after arrival of required information.



The proposed architecture consists of a combination of pipelined hardware logic blocks. Furthermore, this architecture integrates well into the any FPGA based hardware SoC design involved in process of packet classification systems by reusing its IP core.

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