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A Survey on the Performance Analysis of FinFET SRAM Cells for Different Technologies

Girish H, Shashi Kumar D. R

Abstract — This paper presents a survey on the performance analysis of FinFET SRAM Cells for different technologies. Industry requires high performance low power devices and memories. CMOS devices scaled down to reduce the size. As CMOS devices are scaled down the variation in the design metrics like SNM, Leakage power and delay increases. FinFET is an emerging technology in the VLSI design to overcome the drawbacks of CMOS. FinFET has become the most promising alternatives to conventional CMOS. In this paper, comparison of conventional CMOS, Independent-Gate (IG) and Tied Gate (TG) FinFET SRAM standard cells performance analysis is done with respect to leakage power, Static Noise Margin (SNM) and delay.

Index Terms— FinFET, SRAM, SNM, Leakage Power, Delay.

I. INTRODUCTION

FinFET is one of the leading technology and an alternative device structure to replace a conventional CMOS for deep submicron device. The continuous scaling of planar CMOS technology has led to an enormous increase in the leakage current and power. Scaling beyond 14nm technology is difficult owing to degrade short channel effects. FinFET devices offers distinct advantages in suppressing short channel effects and reduction in leakage currents [1] and power compared to that of conventional bulk CMOS. FinFET has emerged as one of the most promising candidates to extend CMOS scaling beyond the sub-22nm node because of superior electrostatic control (short channel effects, SCE) and better immunity to random dopant fluctuations (RDF) [31,32]. FinFETs have emerged as one of the most suitable candidates for DGFET structure [30]. To have a better control on the channel, the structure of FinFET allows for fabrication of separate front and back gates. FinFET transistor can be used to operate in two modes they are Tied-gate mode and Independent-gate (IG) mode.

• Tied-gate (TG) mode, in which both the front and the back gates are tied to the same control signal. Tied-gate FinFET avoids the short channel effects due to superior gate-to-channel coupling [2].Tied-gate FinFET is the simplest FinFET gate with shorted front gate and back gate.

• Independent-gate (IG) mode, in which the front and back gates are tied to different control signals. Independent-gate FINFET merges the parallel P-type Fin-FET, and ties the back gates of the N-type FinFET to ground to achieve matching rising and falling delays [3].

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FinFET based SRAMs have been investigated extremely in literature. The paper highlights the performance analysis of FinFET SRAM cells with respect to Static Noise Margin (SNM), Delay and leakage power. The organization of the paper is as follows: Section 2 describes about FinFET device. Section 3 describes about FinFET SRAM CELLS. Section 4 describes about Design Metrics and Section 5 concludes the paper.

II. FINFET DEVICE

This FINFET based transistors offers good tradeoff for power as well offering interesting delay. The Figure 1. (a), shows 3D structure of a one-fin tied-gate FinFET and 1. (b), shows the 3D structure of a one-fin independent-gate FinFET [19]. The FINFET model structure consists of following regions.

- Low doping silicon fin
- Highly doped poly-silicon region,
- Highly doped contact region between source and drain
- Gate region- oxide (SiO2)

The FinFETs device structure used in this paper have asymmetrical structure [4], as shown in Fig. 1. This structure allows FinFET devices to enhance the energy efficiency, ON/OFF current ratio, and soft-error immunity compared with bulk CMOS counter parts [29].

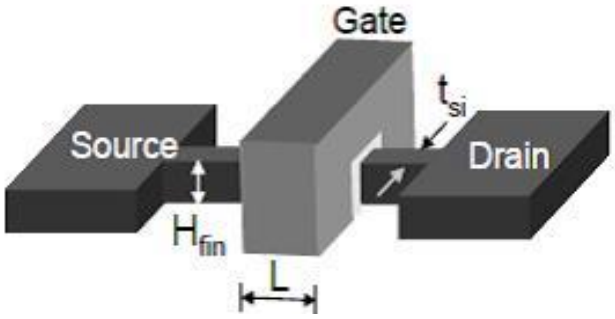

Fig. 1(a): 3D structure of one-fin tied-gate FinFET [4].

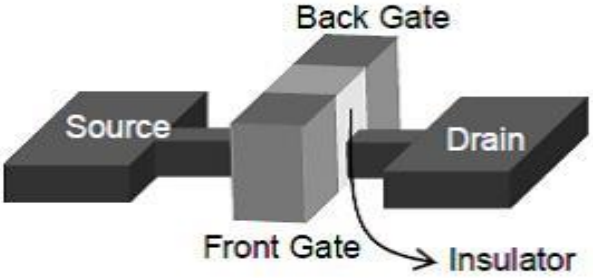

Fig. 1(b): 3D structure of one-fin independent-gate FinFET [4].

The FinFETs width is reduced due to the vertical gate structure. The minimum transistor width is determined by the fin height (W_{min}). The two gates of a single-fin FET tied together, $W_{min} = 2 \times H_{fin} + t_{si}$, Where H_{fin} is the height of the fin and tsi is the thickness of the silicon body as shown in Fig. 1. Since H_{fin} is fixed in a FinFET technology, multiple parallel fins are utilized to increase the width of a FinFET. The total physical transistor width (W_{total}) of a tied-gate FinFET with n parallel fins is given by $Wtotal = n \times W_{min} = n\times (2 \times H_{fin} + t_{si})$. Independent-gate FinFET is obtained by depositing silicon-dioxide on top of the fin there by separating the two vertical gates of a FinFET as shown in Fig. 1b.

III. FINFET SRAM CELLS

The design 6T FinFET SRAM circuits are provided in this section. The CONVENTIONAL 6T SRAM CELL is described in section 3.1. The tied-gate FinFET SRAM cells are presented in Section 3.2. The independent-gate FinFET (IG-FinFET) SRAM circuits are described in Section 3.3.

A. Operation of conventional 6T SRAM Cell

The conventional 6T SRAM cell consists of 6 transistors in which 4 transistors M1, M2, M3 and M4 forms a flipflop and two M5, M6 are the nmos pass transistors. The two bit lines are used for read and write operations [14]. Data is stored in gate capacitance of inverters. The structure is shown in Fig.1. The read and write operation depends on the WL and two bit lines BL and BLB. When WL =1, the transistors M5 and M6 turns 'ON' and allow access to store data in 'Q' and 'QB'. For the write operation, both the bit lines are at opposite voltages i.e. if bit line BL='1', then bit line BLB will be logic '0'. In 6T SRAM cell, both bit lines are kept at opposite voltages (BL=1, BLB=0 or BL=0,BLB=1) and when WL enables transistorsM5 and M6, the data writes on the nodes Q and QB of back to back connected inverters. Similarly, read operation of SRAM cell is inverted of the write operation. For read operation, both bit lines are at logic high, and WL is raised to high. Since one of the nodes is low, one of the pre-charged bit lines start discharging and at that instant data can be read at the time of discharging. A sense amplifier is connected to the output node to read the changing value. Therefore read and write cycle is performed [11]. The waveform is shown in Fig.2.

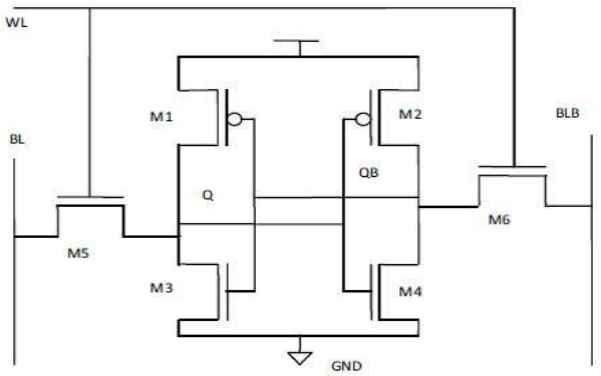

Fig. 2: Schematic of conventional 6T SRAM cell [4]

B. Standard TG-FinFET SRAM Cells

The data stability of a memory circuit is prone to noise during a read operation [5]. In order to maintain the read stability, the current conducting capability of the pull-down transistors must be higher as compared to the access transistors [4]. Alternatively, for write ability, the current conducting capability of the access transistors must be stronger as compared to the pull-up transistors [5] [6]. Two tied-gate FinFET SRAM cells (SRAM-TG1) is presented in this paper, as shown in Fig. 3. All of the six transistors in SRAM-TG1 are sized minimum (one fin), as shown in Fig.3.

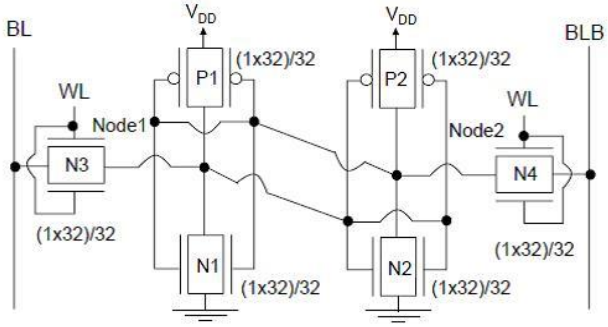

Fig. 3: Two tied-gate FinFET SRAM cells [4].

C. IG-FinFET SRAM Cells

Two IG-FinFET 6T SRAM cells [6], [7], [8] are presented in this section. The idle mode leakage power consumption is reduced with the IG-FinFET SRAM cells while enhancing the data stability and the integration density as compared to the tied-gate FinFET SRAM circuits [4]. All of the transistors in the two independent-gate SRAM cells have single fin (minimum width) as shown in Fig. 4.

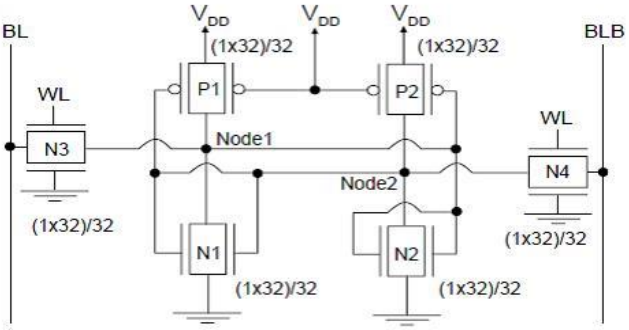

Fig. 4. The IG-FinFET SRAM cells. SRAM-IG1 [4].

IV. DESIGN METRICS

Design considerations for FinFET SRAM Cells presented in this paper are Static Noise Margin (SNM), Delay and leakage current.

A. Static Noise Margin (SNM)

Static noise margin (SNM) is the design metric used in this paper to characterize the read and write stability of the SRAM cells [4]. The SNM is defined as the minimum DC noise voltage necessary to flip the state of an SRAM cell [9] [19]. The read and write SNM of the four SRAM cells during a read and write operation are shown in Fig. 6.

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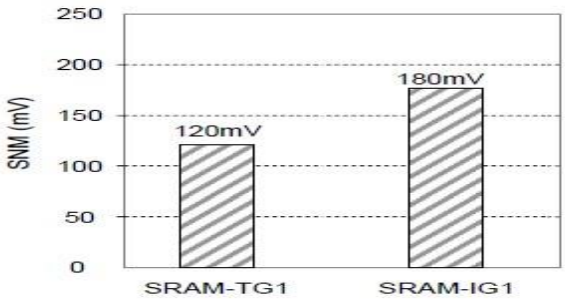

Fig. 6.The read SNM of the tied-gate and the independent-gate FinFET SRAM cells.

TABLE I. Read & Write SNMS Voltages

Technology	SRAM Cell	Read SNM (mV)	Write SNM (mV)
32nm	Conventional 6T SRAM CELL[22]	250	268.70
32nm	SRAM-TG1[23]	179	172
32nm	SRAM-IG[22]	260	186
22nm	Conventional 6T SRAM CELL[23]	218	250
22nm	SRAM-TG1[19]	120	160
22nm	SRAM-IG[19]	180	172

Table I shows the comparison of Read and Write SNM for 32nm and 22nm technologies. From the table it is seen that Read and Write SNM of SRAM-TG1 is less when compared to that of SRAM-IG and conventional 6T SRAM Cell for 32nm and 22nm.

B. Leakage Power Consumption

The leakage power consumption of the FinFET SRAM cells at 70°C and 27°C are shown in Fig. 7. The leakage power of an SRAM cell is determined by the total effective transistor width that produces the leakage current. In SRAM-TG1 and SRAM-IG1 all the transistors are sized minimum. SRAM-TG1, SRAM-IG1 therefore consume the lowest leakage power [4] as illustrated in Fig. 6. The leakage power consumed by SRAM-IG1 & SRAM-TG1 are same. The leakage power consumed by conventional 6T SRAM cell is less when compared to that of SRAM-TG1 and SRAM-IG1 [12][13].The leakage power consumed by 6T SRAM cell is less when compared to that of conventional 6T SRAM, SRAM-TG1 and SRAM-IG1.

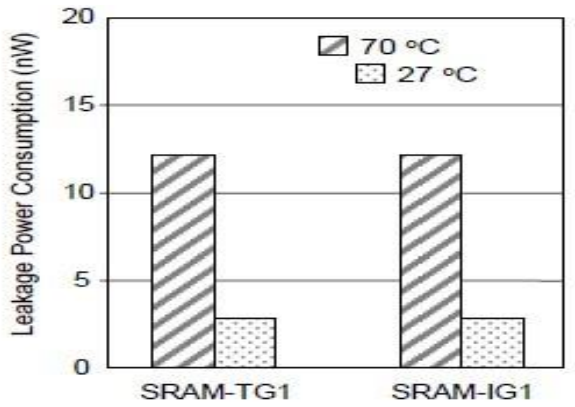

Fig. 7. The leakage power consumptions of the FinFET SRAM cells.

TABLE II. Leakage power consumptions

Techno-logy	Parameter	Conventi-onal 6T SRAM CELL	SRAM-TG1	SRAM-IG
32nm	Leakage power consumption [22] (µW)	28.22	1.0293	0.667
22nm	leakage power consumption (µW) for VDD= 0.8V [19]	3.19	1.32	1.01

Table II shows the comparison of leakage power consumption for 32nm and 22nm technologies. From the table it is seen that leakage power consumption of SRAM-IG is less when compared to that of SRAM-TG1 and conventional 6T SRAM Cell for 32nm and 22nm.

C. Propagation Delay

The junction and oxide capacitances of the access transistors attached to the bit-lines are extracted for each FinFET SRAM cell. The length of the bit-lines is estimated based on the cell layout height. The read delay is defined as the time required for developing a voltage difference of 200mV between BL and BLB [10]. The delay of the four FinFET SRAM circuits are shown in Fig. 8.

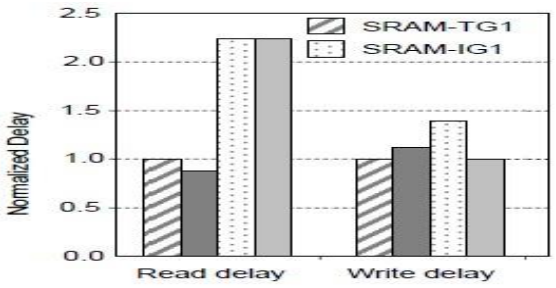

Fig. 8. The propagation delays of the FinFET SRAM circuits.

TABLE III. Propagation Delay

Techno - logy	parameter	Conventional 6T SRAM CELL	SRAM -TG1	SRAM -IG
32nm	Read Delay[27] [10] (ps)	62.32	63.12	108.77
32nm	Write Delay[27] [10] (ps)	2.185	30.1	27.7
22nm	Read Delay[19] (ps)	18.46	63.12	108.77
22nm	Write Delay [19](ps)	18.73	30.1	27.7

Table III shows the comparison of read delay and write for 32nm and 22nm technologies. From the table it is seen that read delay of conventional 6T SRAM Cell is less when compared to that of SRAM-TG1 and SRAM-IG for 32nm and 22nm.

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V. CONCLUSION

Conventional CMOS, Independent-gate FinFET and Tied Gate 6T SRAM cells are presented in this paper for enhancing the SNM, to reduce, leakage current and to reduce the propagation delay. This paper discusses various design aspects of Conventional and FinFET based SRAM design. All of the six transistors of the SRAM-IG cells are sized minimum. Furthermore, the leakage power consumption of the SRAM-IG cells is same as compared to that of a 6T tied-gate FinFET SRAM cell that is sized for comparable read static noise margin.

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