Fault Tolerant Voltage Source Converter for HVDC Transmission System

Patil Mounica, Elizabeth P Cheriyan

Abstract*—this paper presents Fault *Tolerant Voltage Source Converter for HVDC transmission system based on a hybrid multilevel voltage source converter with ac-side cascaded H-bridge cells. The proposed converter offers a unique feature of dc fault blocking capability (ability to block power exchange between the ac and dc sides during the dc side faults, hence no current flows in converter switches), operational flexibility in terms of active and reactive power control, black start capability, in addition to improve ac fault ride through capability. In this paper, four quadrant operation and voltage support, the ac and dc fault ride-through capabilities of the proposed converter will be demonstrated.

Index Terms*—AC and DC fault ride through capabilities, DC fault reverse blocking capability, hybrid multilevel converter with ac side cascaded H bridge cells.

I. INTRODUCTION

In the past decade, VSC-HVDC transmission systems have evolved from simple two level converters to neutral point clamped converters and then to true multilevel converters such as modular converters. This results to lower semiconductor losses and increase power handling capability of VSC-HVDC transmission systems in comparison to conventional HVDC systems based on current source converters topology. However, the inability to withstand the effects of the HVDC network to dc side fault and the capability to operate at high voltage to isolate the dc fault current in absence of dc circuit breakers makes an issue towards the evolution of the dc grid. The main issues of the HVDC network during dc side faults are:

- Over-current on converter switches during dc side faults, and after the fault cleared, inrush current as the dc link voltage builds up.
- Dc side fault exposes the dc circuit breakers to high let-through current to tolerate the discharge of high fault current flowing at the dc side. It must be capable of operating at high voltage and isolates temporary or permanent dc faults.

A new generation of converter using H-bridge cells has been implemented to eliminate the drawbacks for VSCs know as the Hybrid multilevel converter with H-bridge cells in the ac side. These converters inherently provide dc fault reverse blocking capability, which can be used to improve VSC-HVDC resiliency to dc side faults. The following of this paper is organized as follows.

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Section II describes the operating principle of Hybrid multilevel converter with H-bridge cells in the ac side. Section III describes the control strategy for an HVDC transmission system based on a hybrid multilevel VSC with ac-side cascaded H-bridge cells. Section IV presents test network and simulations of a hybrid multilevel converter HVDC transmission system. Section V gives conclusion.

II. HYBRID MULTILEVEL CONVERTER WITH H-BRIDGE CELLS IN THE AC SIDE

Fig .1 shows single phase of a hybrid multilevel converter with N, H-bridge cells per phase. It can generate 4N+1 voltage levels at converter terminal “a” with respect to supply midpoint “0”. Therefore, with large number of cells per phase, the converter will produce pure sinusoidal voltage at the converter transformer. The H-bridge cells between “M” and “a” are operated as a series active filter to attenuate the harmonics in voltage produced by two level converter bridge. In order to minimize the conversion losses in the H-bridge cells, the requirement of number of cells has been reduced to produce a voltage of $V_{dc}/2$ across the H-bridge floating capacitor. As a result of using less number of H-bridge cells, a small converter station is required than modular multilevel converter. Here a seven cell topology is used which provides 29 level voltage at converter terminal. The effective switching frequency is less than 150 Hz per device. However the operation of hybrid multilevel VSC requires a voltage balancing scheme which ensures that the voltage across the H-bridge cells are maintained at Vdc/N under all operating conditions, where the Vdc is the total dc link voltage. By using this feature the following benefits are achieved:

- The risk of failure of converter switches during dc side fault is reduced due to DC fault reverse blocking capability.
- Reduces the current rating of dc circuit breaker that will be required to isolate dc side faults.
- It allows recovery without interruption from temporary dc side faults. It also simplifies the recovery strategy from dc side faults as the current in the dc side will decay to zero.

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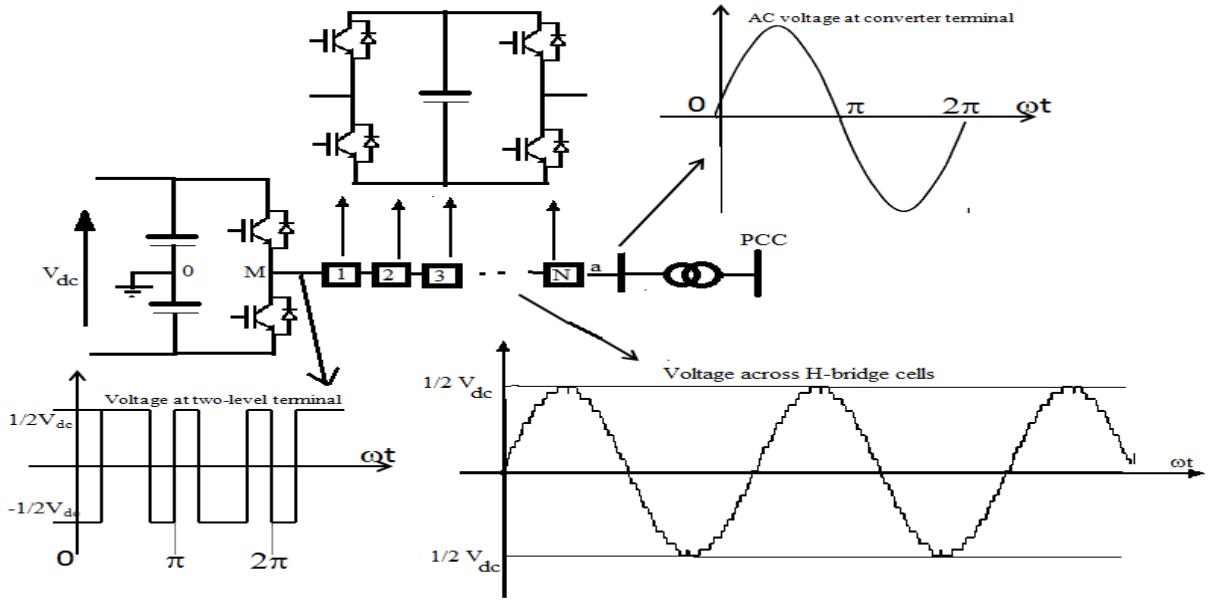

Fig.1. Hybrid multilevel converter with H-bridge cells in the ac side

III. CONTROL STRATEGY FOR AN HVDC TRANSMISSION SYSTEM BASED ON A HYBRID MULTILEVEL VSC

A HVDC transmission system based on a hybrid multilevel VSC with ac-side cascaded H-bridge cells requires three control system layers. The inner control layer represents the modulator and capacitor voltage-balancing mechanism that generates the gating signals for the converter switches and maintains voltage balance of the H-bridge cell capacitors. The intermediate control layer represents the current controller that regulates the active and reactive current components over the full operating range. The outer control layer is the dc voltage (or active power) and ac voltage (or reactive power) controller that provide set points to the current controllers. The current, power, and dc link voltage controller gains are selected using root locus analysis, based on the applicable transfer functions. Fig. 2 summarizes the control layers of the hybrid multilevel VSC.

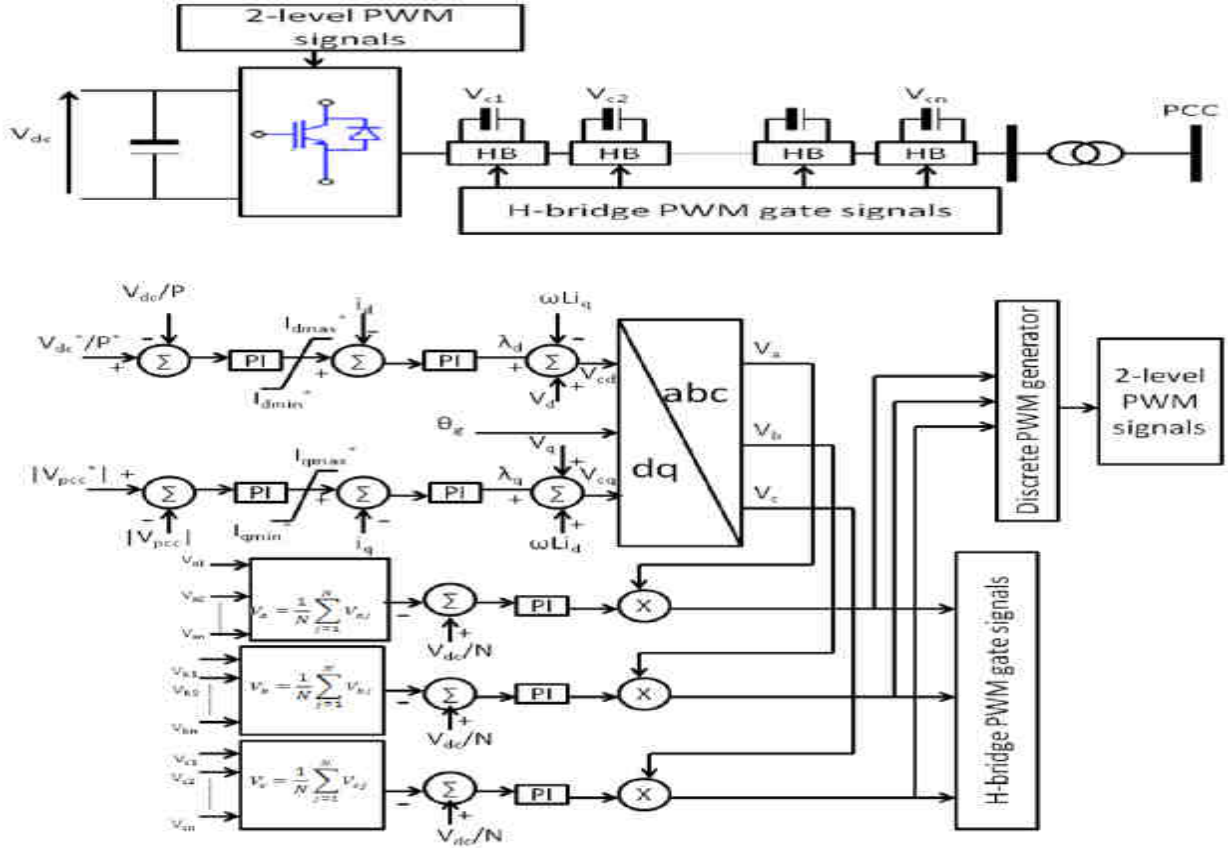

Fig.2. Schematic diagram represents the control layer of the hybrid multilevel converter with ac side cascaded H-bridge cells

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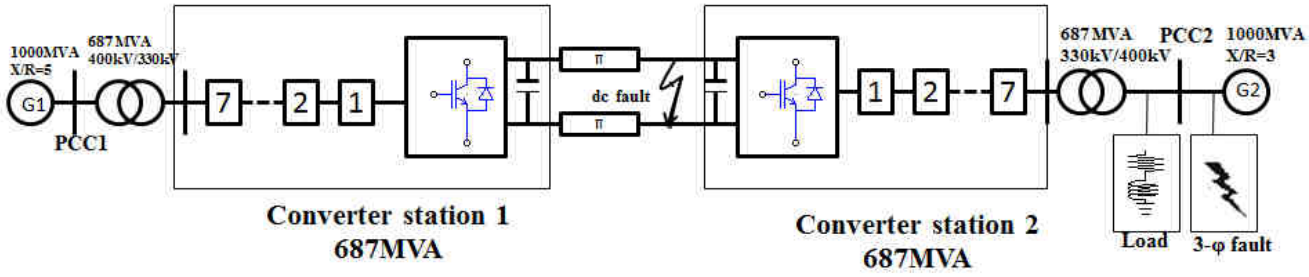


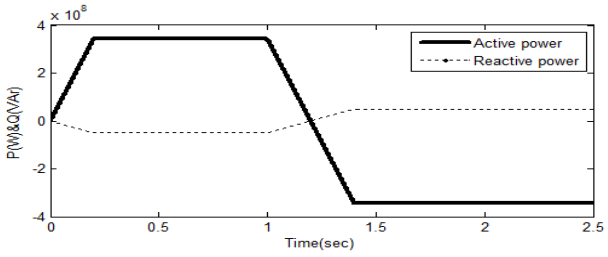
Fig.3 Test System

IV. TEST SYSTEM AND SIMULATIONS

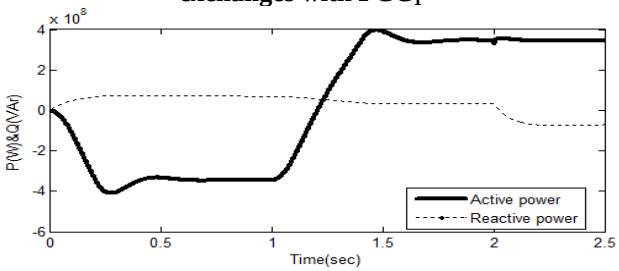
Fig.3 shows the test system where the 687MVA VSC based on the topology shown in Fig.1, are operated as two converter stations of the VSC-HVDC transmission system. The VSC control system is designed for active power control and voltage magnitude at the PCC_2. In order to minimize the dc link voltage rise, when the VSC active power transfer collapses as the voltage at PCC_2 collapses during ac faults, the active power loop is modified so as to maintain power balance between the ac and dc sides and to eliminate the trapped energy in the dc link. G_2 represents a strong grid of 400kV, 1000MVA and X/R=3. In order to demonstrate the ac fault ride through capability of the converter, the system in Fig.3 is subjected to three phase fault with fault duration of 140msec. For dc fault capability, the system in Fig.3 is subjected to pole to pole with fault duration of 140msec.

A. Four Quadrant Operation and Voltage Support

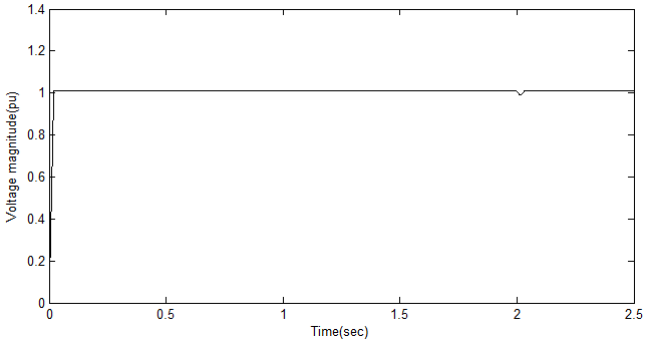
For four quadrant operation and voltage support to the system in Fig.3, converter station 1 is commanded to increase its output power from G_1 to G_2 from 0 to 0.5pu at 2.5pu/sec. At time t=1sec it is recommended to reverse the active power flow in order to import the power from grid G_2, at -2.5pu/sec. At t=2sec a load of 120+j90MVA is introduced at PCC_2. Fig.4 shows the system is able to meet steady state requirements, such as provision of voltage support and four quadrant operation without compromising the voltage and current stress on the converter switches.



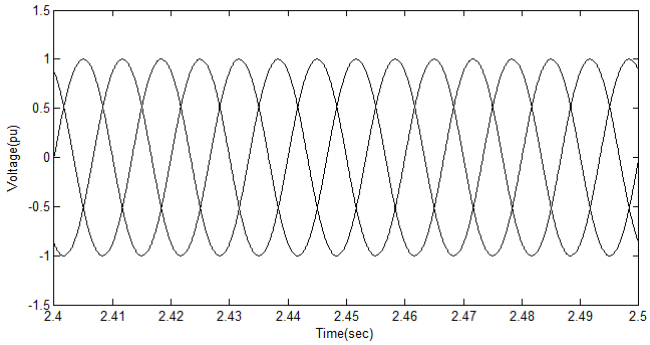
(a) Active and reactive power converter station1 exchanges with PCC_1



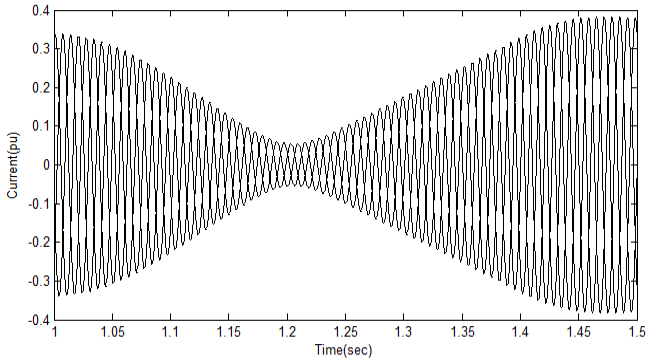
(b) Active and reactive power converter station2 exchanges with PCC_2



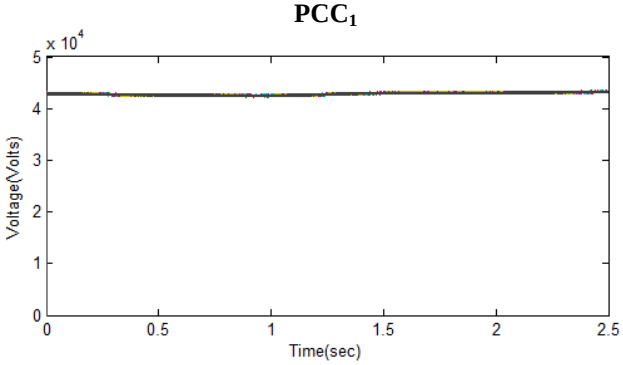
(c) Voltage magnitude at PCC_2



(d) Voltage waveform at PCC_2



(e) Current waveforms converter station1 exchanges with PCC_1



(f) Voltage across the cell capacitors of the three phases of converter 1

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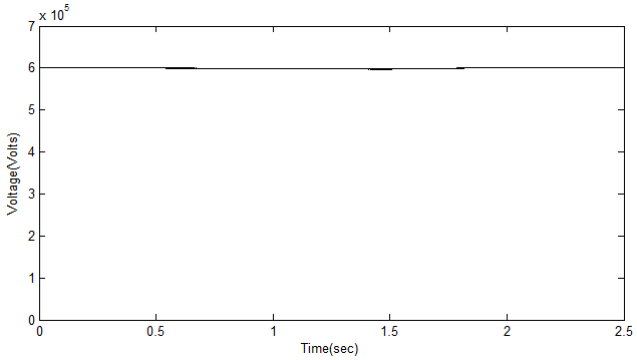
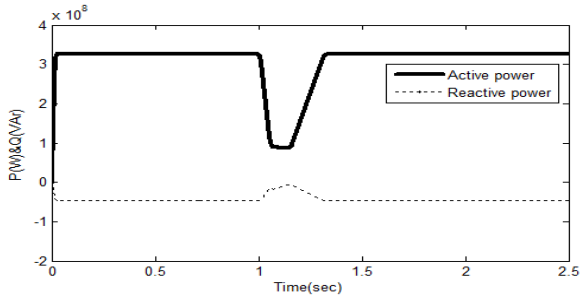


(g) Voltage across the dc link of converter station2

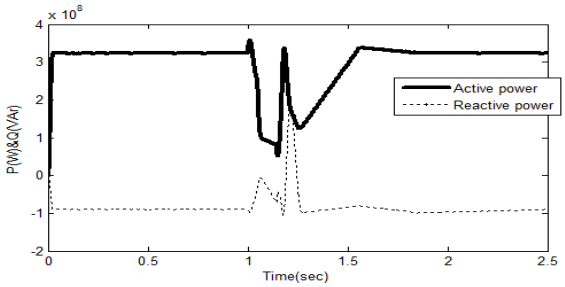
Fig.4 Waveforms demonstrating the steady state operation of HVDC system.

B. AC fault ride-through capability

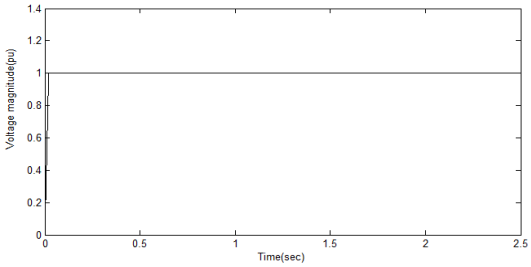
Fig.5 shows the result obtained when the test system is subjected to a 140msec three phase fault to ground at the location shown in Fig.3. During the fault period, converter active power output is reduced to zero to minimize the trapped energy in the dc side thus minimizing the dc link voltage rise. The converter station recovers from the three-phase fault with the current controller limiting the current contribution to the fault during the entire fault period even the voltage magnitude at PCC_2 collapsing to zero. Also the voltage stress across converter switches is controlled as the voltage across the cell capacitors remains at the desired set point.



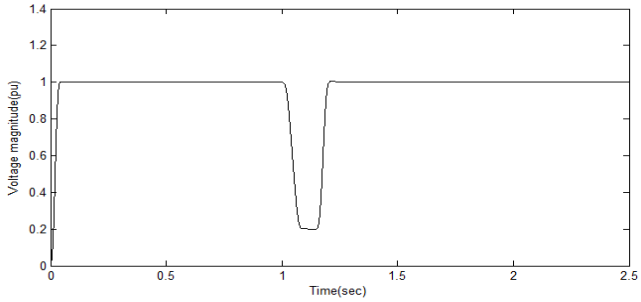
(a) Active and Reactive power converter 1 exchanges with PCC_1



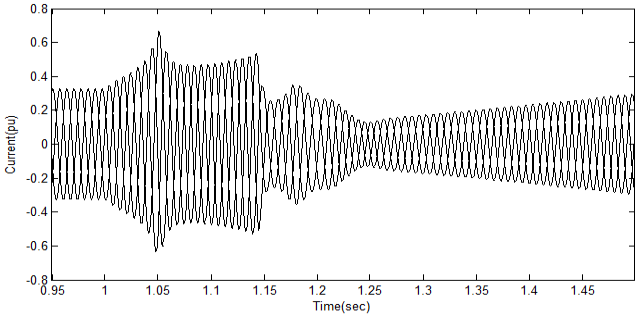
(b) Active and Reactive power converter 2 injects into PCC_2



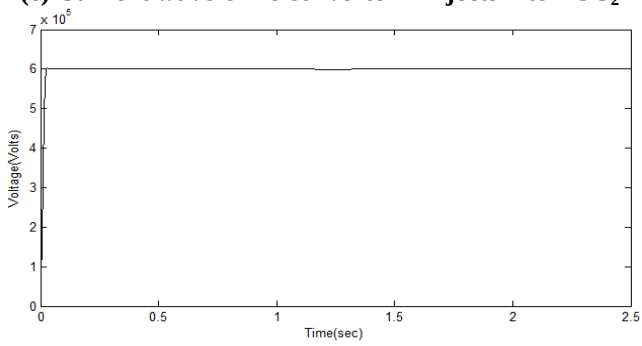
(c) Voltage magnitude at PCC_1



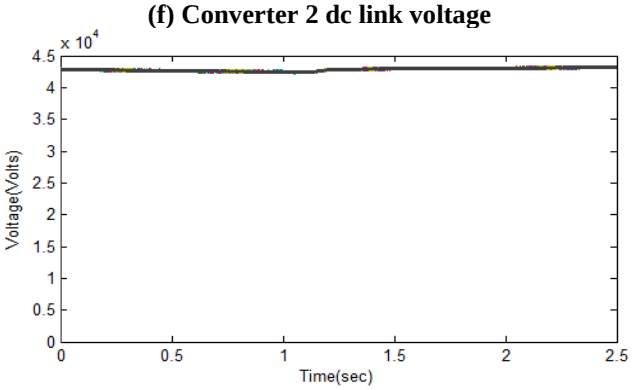
(d) Voltage magnitude at PCC_2



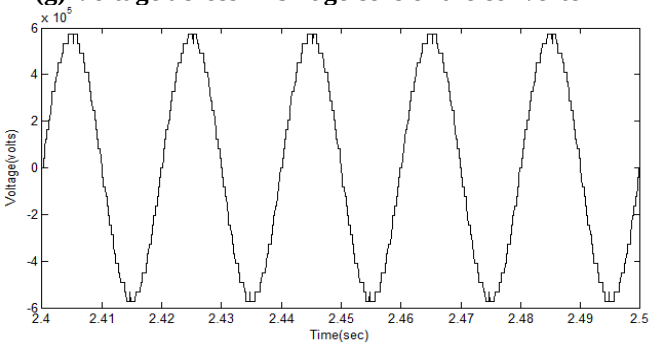
(e) Current waveforms converter 2 injects into PCC_2



(f) Converter 2 dc link voltage



(g) Voltage across H-bridge cells of the converter 2



(h) Line to line voltage waveform at the terminal of converter1

Fig.5 Waveforms when the system in Fig.3 is subjected to a three phase to ground fault ,at time t=1sec with a fault duration of 140msec

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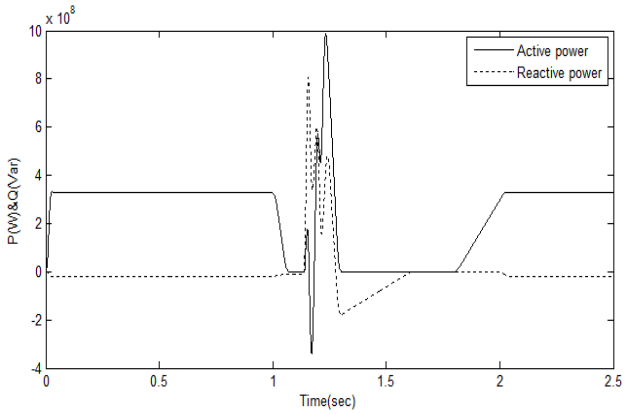
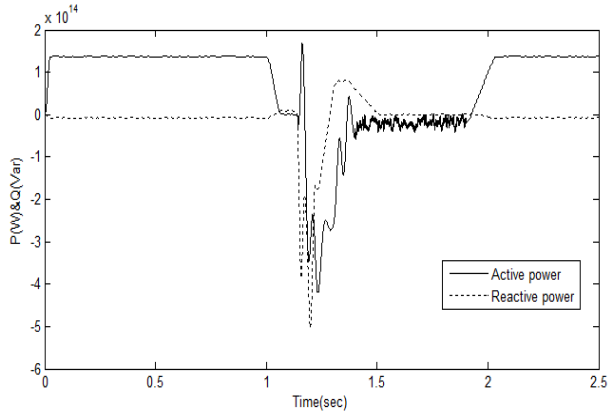
C. Dc fault ride-through capability

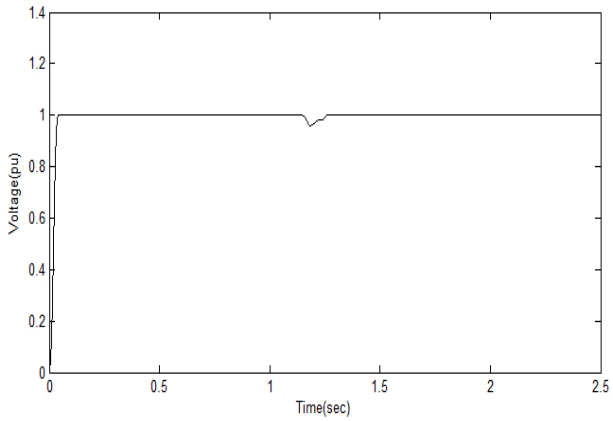
Fig.6 show the results obtained during pole to pole dc faults as shown in Fig.3 at time t=1sec with a duration of 140msec. During the fault period the converter station output active power is reduced to zero and converter reverse blocking capability is achieved by inhibiting the gating signals to the converter switches. The gate signals to converter switches are restored when the fault is cleared at t=1.4sec and is followed by a gradual increase in converter output active power as shown in Fig.6. During the entire fault period, the active and reactive power exchange with the grid are blocked,resulting in zero current in the converter switches. This confirms the ability of the H-bridge multilevel converter to eliminate the grid contribution to the dc fault current,hence reduces the risk of over current in the converter switches.



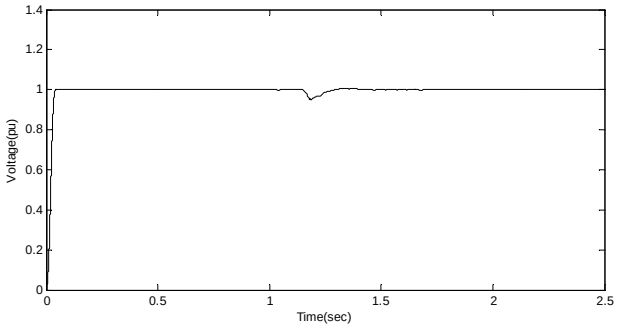
(a) Active and Reactive power converter 1 exchanges with PCC_1



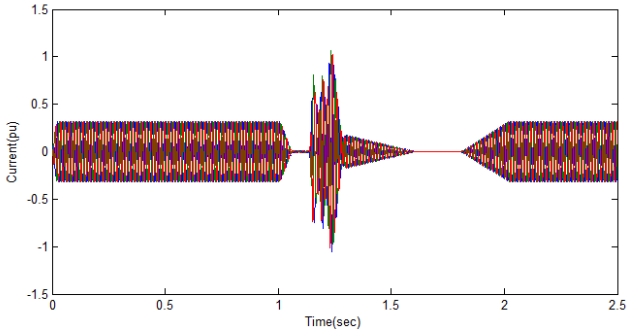
(b) Active and Reactive power converter 2 exchanges with PCC_2



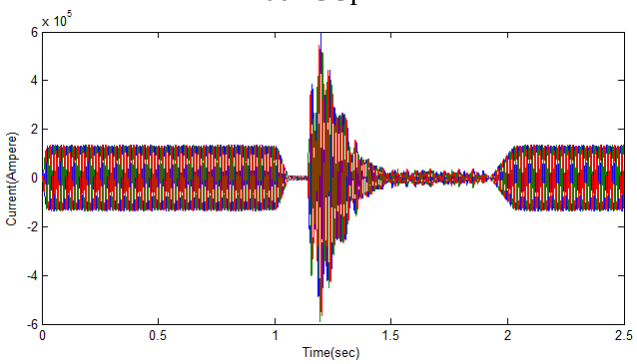
(c) Voltage magnitude at PCC_1



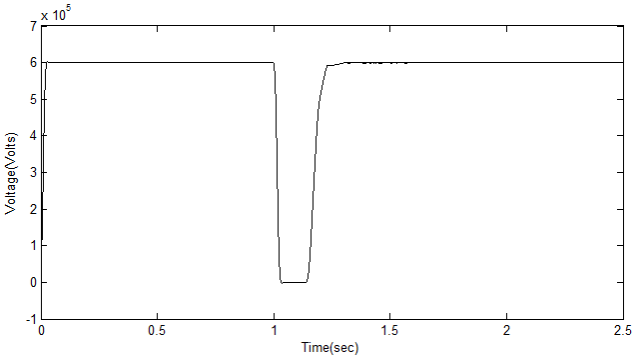
(d) Voltage magnitude at PCC_2



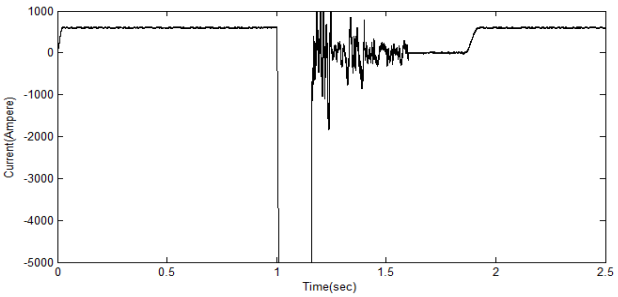
(e) Current waveforms converter1 exchange with grid G_1 at PCC_1



(f) Current waveforms converter2 exchange with grid G_2 at PCC_2



(g) Converter2 dc link voltage



(h) dc link current with dc fault reverse blocking capability

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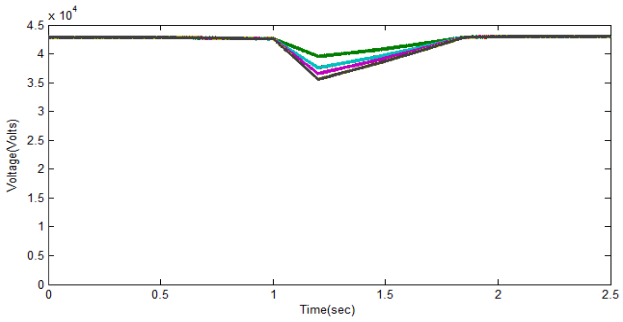
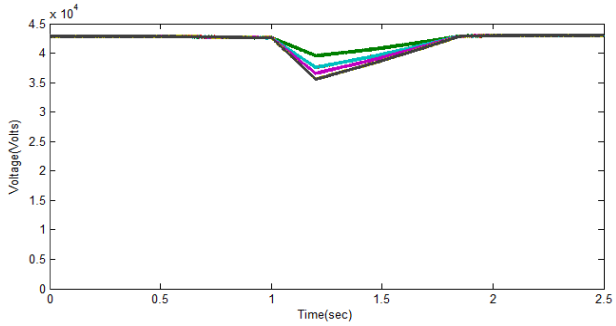


(i)Voltage across the H-bridge cell capacitors of converter1



(j)Voltage across the H bridge cell capacitors of converter2

Fig.6 Waveforms during pole-to-pole dc fault at t=1sec with a duration of 140msec

V. CONCLUSION

Based on the developed control strategy for the VSC-based HVDC power transmission i.e. the design of the current controller, the DC voltage controller, the active and reactive power controllers and the AC voltage controllers, the VSC-HVDC transmission system based on a hybrid multilevel converter with ac-side cascaded H-bridge cells is implemented. The behavior of the four-quadrant operation, voltage support capability and the ac fault ride-through capability of the HVDC system are simulated in the MATLAB Simulink and results are obtained.

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