International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-4 Issue-4, April 2015

Architecture and Design of 4x4x4 NOC for Multicore SOC

Shalaka V. Parmar, Roshani B. Kharche, Payal V. Mamankar, Hasan M. Raza

ABSTRACT: ***Network on Chip (NoC) architecture provides a good way of realizing efficient Interconnections in multiprocessors. 3D NoC uses a mesh topology with wormhole switching and stall-go flow control scheme. It improves scalability, diminished concurrent communication, and low power consumption. NoC communication is realized by data packets and forwarded among the network which routes according to Look-Ahead-XYZ routing algorithm (LA-XYZ). The proposed paper focuses on design and verification of 4x4x4 3D NoC. The proposed 3D Network on Chip is designed in VHDL language at RTL level and verified on Xilinx using ISE 14.1 tools. The targeted device is FPGA Virtex-6 XC5VLX30.The minimum input arrival time before clock and maximum output time required time after clock is estimated as 13.094 ns and 10.107 ns respectively.***

Keywords-3D-NoC; Concurrent; LA-XYZ;

I. INTRODUCTION

Network-on-Chip model is promising as the solution for the problems of interconnecting number of cores into a single system on chip. NoC interconnects CPU, DRAM, SRAM and DMA memories on hop-by-hop basis [2]. NoC consists of computational processing elements (PEs) and routers. Each PE is connected to the PE of a local router. When a packet is sent from a source PE to a destination PE, the packet is forwarded hop by hop on the network via the decision made by each router. For each router, the packet is first received and stored in an input buffer. The control logic in the router is responsible to make routing decision and channel arbitration. The router navigates the granted packet through a crossbar to the next node, and the process repeats until the packet reaches at its destination node [3]. Eventually as technology scales and switching speed increases, network on chips becomes sensitive and prone to errors and faults. The Network on Chip is a new paradigm to replace the classic interconnections such as point to point, crossbar, bus, etc. The 2D mesh NoC architecture is the most used topology due to its regularity, simplicity for routing and easy integration in FPGA circuit. All the links have the same length, thus exhibiting the same latency. The limitation of sufficient bandwidth for any transaction between memories and cores as well as communication between different cores comes from high diameter that suffers from NoC.

Manuscript published on 30 April 2015.
***** Correspondence Author (s)
Shalaka V. Parmar, Department of Electronics and Telecommunication, Government College of Engineering, Chandrapur
Roshani B. Kharche, Department of Electronics and Telecommunication, Government College of Engineering, Chandrapur
Payal V. Mamankar, Department of Electronics and Telecommunication, Government College of Engineering, Chandrapur
Hasan M. Raza, Department of Electronics and Telecommunication, Government College of Engineering, Chandrapur

For all these reasons, need for optimizing NoC based architecture becomes necessary for designing fast routers and new network topologies.

II. NETWORK ON CHIP- A BACKGROUND

Nanometer technologies allow fabrication of millions of transistors onto a single chip which kept increasing along the past few decades [3]. Systems used in SoCs are Conventional bus based systems and point to point links. These systems are no longer reliable architecture for highly complex systems. It should be capable of providing rapid data transfer among processors and memories. Network on Chip (NoC) provides a scalable architecture with a large potential to handle the increasing complexity [4]. Network on chip architectures are becoming the network fabric for both general purpose multiprocessors and application-specific SoCs design.

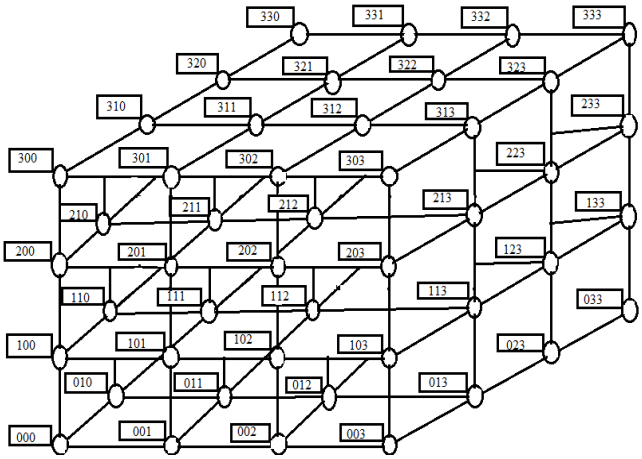

Figure 1: 3D-NoC based on 4x4x4 Mesh Topology

In a 4x4x4 mesh network topology each of the network nodes are interconnected with one another as shown in figure 1. Some nodes are connected through single hops and some may be connected with more than one hop. Wormhole flow control is a system of simple flow control mechanism in computer networking based on known fixed links. Router store one packet and send the stored packet before arriving next flit to neighboring routers [5]. Stall-Go module manages the case of the buffer overflow. When the buffer exceeds its limitation on hosting packet (if the number of packets waiting for process are greater than the depth of the buffer), a flow control has to consider preventing from buffer overflow. Thus, they allocate available resources to packets as they progress along their route [6]. Stall-Go flow control used as it gives a low-overhead efficient design and also gives remarkable performance as compare to the other flow control schemes.

In stall-Go mechanism, capacity of buffer is fulfilled up to the level as it passes one packet at a time and buffer generates stop_out signal. It works as stop_in signal for the Stall-Go mechanism. If stop_in signal is zero, buffer is nearly full else it is one. If step-in is one , blocked signal is one i.e. data transfer is not suspended and if stop_in is zero and data sent is one then blocked signal goes to zero according to the stall-go mechanism so the data packet transfer is suspended.

III. 3D-NoC OVERVIEW

A. Input port Module

The input-port module consists of input buffer and router module as illustrated in figure 2. Incoming 81 bits packet data from different neighboring switches are first stored in the input buffer. Each input port has a FIFO buffer with depth four and width of 81 bits. It can host up to four packets of 81 bits each. When the sw_grant signal goes high stored packet is fetched from the FIFO buffer and passes to the next pipeline stage (RC). The switch grant (sw_grant) is used as a read enable signal to the FIFO buffer. The data packet is sent to the Router circuit where LA-XYZ routing algorithm is used to determine the New-Next-Port address for the next downstream node. LA-XYZ computation is accomplished in two steps: (I) Assign next address and (II) Define new Next-port i.e. New-Next-Port. The first step fetches the Next-Port identifier from the incoming packet. Depending on the direction of this identifier the address of the next downstream node can be predicted [7]. This address is then used in the second step by comparing it with the destination address of the packet. Finally, information about the Next-Port is obtained in the packet.

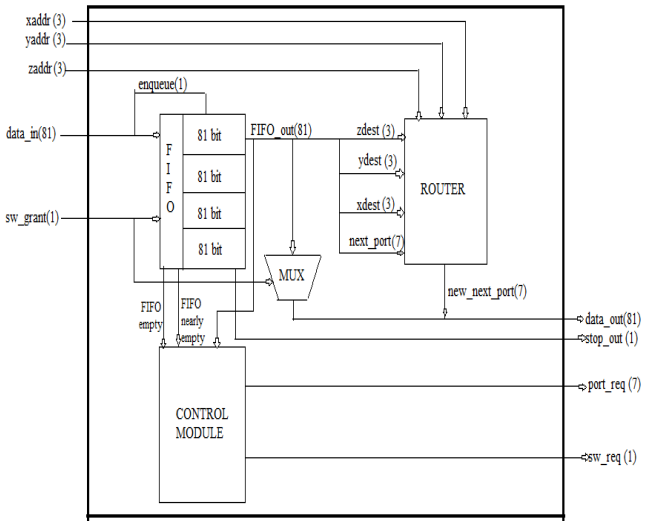

Figure 2: Input-port module architecture

At the same time, Next-Port identifier is also used to generate the port request (port_req) for the particular output port and also generate switch request (sw_req).These request are generated using the two signals fifo_empty and fifo_nearly empty which are issued from the buffer to give information about buffer status. The stop-out signal of the input port module is the fifo_nearly full signal generated when FIFO buffer has space to host only one packet. To simplify the process of routing on the network, address of node is expressed in X, Y and Z co-ordinates, where X represents horizontal position, Y represents longitudinal position and Z represents vertical position. The proposed router architecture uses Look Ahead XYZ routing algorithm (LA-XYZ) so as to minimize number of hops while routing of the data packets from source to destination. Routing algorithm compares the address of the processing node with the address of destination node address to determine the New-Next-Port address. The routing mechanism works in two steps. Steps one deals with determining next_xaddr, next_yaddr and next_zaddr [8].

B. Switch-allocator Module

The switch allocator module is used to perform arbitration between the different requests. Figure 3 shows the switch allocator module composed of stall-Go flow control and priority based arbiter. When several packets compete for the same output port, 3D-NoC arbiter in the switch allocator grants the request based on priority.

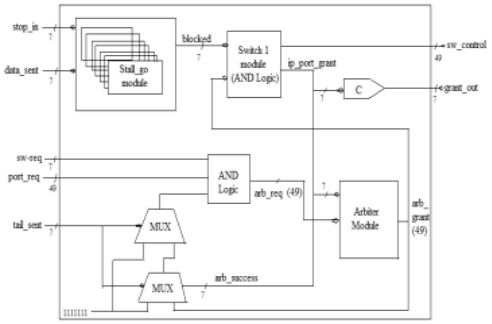

Figure 3: Switch allocator module circuit

The input port_req and sw_req issued from input-port module gives information about Next Port and are transmitted to the switch allocator module to perform the arbitration between the different requests [9].When more than two flits from different input-ports are requesting the same output-port at the same time, the switch allocator manages to decide the output port to be allocated.

C. Crossbar Module

In crossbar module, each mux is provided with seven bit select signal which is the control signal provided by switch allocator. The switch allocator sends the control signal to the crossbar circuit to complete crossbar traversal pipeline stage (CT), where information about the selected input port and next-port are embedded and stored in sw_cntrl register as shown in figure 4.

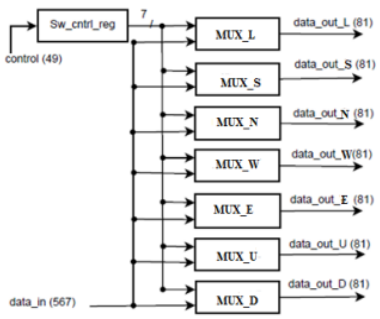

Figure 4: Crossbar module

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When all the flits are transmitted, the tail bit informs the switch allocator via a tail-sent signal that the packet transmission is completed [7].

IV. SIMULATION RESULTS

Simulation refers to the verification of design, its function and performance. The proposed 3D Network on Chip is designed in VHDL language at RTL level and verified on Xilinx using ISE 10.1 tool. The target device is FPGA Virtex-6 XC5VLX30.In this section we present and discuss the synthesis results. Table 1 shows the parameters used for synthesis for both 2D and 3D Node designs. Node performances are evaluated in terms of area and clock frequency. Area of the node increases with addition of number of ports. The 7-port router needs more area than a 2D router due to the addition of the two vertical ports and a large crossbar. We compared our 2D Node and 3D Node implementation with previously designed [9] nodes as shown in Table 2. The area of our Node which uses a buffer for each input port is lower than the area presented in [9].The minimum input arrival time before clock and maximum output time required time after clock is estimated as 13.094 ns and 10.107 ns respectively.

Table 1: Simulation parameters

Node parameters	2D Node	3D Node
Buffer depth	4	4
Packet size	76	81
Switching policy	Wormhole	Wormhole
Flow control	Stall-Go mechanism	Stall-Go mechanism
Scheduling	Fixed priority	Fixed priority
Routing	LA-XY	LA-XYZ
Target device	Virtex-5 XC5VLX30	Virtex-5 XC5VLX30

Table 2: Performance comparison with Other node

Resources	5 Ports (2D)		7 ports (3D)	
	[9]	Our	[9]	Our
Slices (Area)	3850	2391	8895	6335
Frequency (MHz)	252	522	250	205
Flip-Flops	3654	2290	6869	3398

V. CONCLUSION

Proposed 3D Network on Chip architecture is used to forward data packet from source node to destination node. The synthesis and simulation of the proposed NoC is verified through VHDL codes at RTL level using Xilinx ISE 14.1 tool. Despite increasing the frequency, proposed 4x4x4 node 3D NoC shows an improvement in terms of area by reducing delay overall compared to 2D NoC. The performance of our design is enhanced by optimizing the routing algorithm. The reliability and the robustness of the proposed router can be improved. Matrix arbiter of switch allocator on the basis of rotating priority can be implemented. To obtain an enhanced design of 3D-NoC, performance can be increased while keeping the hardware cost balanced and reasonable.

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