International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-4 Issue-2, December 2014

Sub Threshold Level Shifters and Level Shifter with LEC for LSI's

J. Chaitanya Varma, R. Ramana Reddy, D. Rama Devi

Abstract*— Wide-range level shifters play critical roles in ultralow-voltage circuits and systems. In this paper level shifter circuits that are capable of converting subthreshold to above threshold signal levels are presented. Level shifters are designed using current mirrors. The circuit has a distinctive current generation scheme using a logic error correction circuit that works by detecting the input and output logic levels. The proposed level shifter circuit can convert low-voltage digital input signals to high-voltage digital output signals. The circuit achieves low-power operation because it dissipates operating current only when the input signal changes. Simulations are carried out using Mentor Graphics 130-nm technology. Performances of the proposed level shifters are compared in terms of delay, power consumption and duty cycle.

Index Terms: Level Shifters, Current mirrors, Logic Error Correction Circuit, Mentor Graphics.

I. INTRODUCTION

Subthreshold operation is an emerging method to achieve ultralow power consumption in digital systems. This advantage comes at the cost of reduced performance and robustness. Some parts of a digital system might be implemented in conventional above-threshold logic to satisfy strict performance constraints, while other parts can be operated in subthreshold mode to reduce power dissipation. Such an approach leads to multivoltage subthreshold systems on- a-chip (SoCs). Even if the whole core of a chip operates at subthreshold voltage levels, a secondary above-threshold supply voltage is still needed for the digital I/O pad cells. Using analog pad cells directly connected to subthreshold logic is not practical because very large buffers would be needed to achieve acceptable transition times considering the high parasitic capacitance of the bond pad, bond wire, device package, PCB tracks, and further off-chip load. Level Shifters are needed externally to connect subthreshold chips to logic analyzers, or other equipment. Resource-efficient onchip level shifters with high robustness are needed to interface subthreshold circuit parts with above-threshold modules. To address these issues an efficient Level Shifter (LS) is required to convert the signal from the sub-threshold voltage level to a higher voltage.

Manuscript published on 30 December 2014.
***** Correspondence Author (s)
J. Chaitanya Varma*, Department of ECE, M.V.G.R College of Engineering, Vizianagaram, India.
Dr. R. Ramana Reddy, Department of ECE, M.V.G.R College of Engineering, Vizianagaram, India.
Mrs. D. Rama Devi, Department of ECE, M.V.G.R College of Engineering, Vizianagaram, India.

II. CONVENTIONAL LEVEL SHIFTER

Fig. 1 shows the schematic of a Conventional LS circuit. The circuit consists of cross-coupled p MOSFETs (MP1 and MP2) and two n MOSFETs (MN1 and MN2) driven by complementary input signals IN and INB. The circuit has critical problems when the voltage difference between low supply voltage V_{DDL} and high supply voltage V_{DDH} becomes large. When the voltages of IN and INB are Low and High, MN1 and MN2 are OFF and ON, respectively. MN2 then pulls down node OUT, causing MP1 to turn ON. OUTB increases to V_{DDH} resulting MP2 turns OFF, and OUT drops to the GND level. Voltage at OUT is determined by the drive currents of pull-up transistor MP2 and pull-down transistor MN2. If the drive current of MP2 is larger than that of MN2, OUT cannot be discharged. In the case of extremely low-voltage subthreshold digital LSIs, ON-current of MN2 becomes quite low, the drive currents of the n MOSFETs are significantly smaller than those of the p MOSFETs, which operate in the strong inversion region. Thus, OUT cannot be discharged.

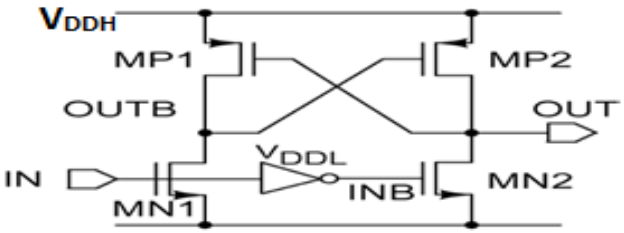

Figure 1: Conventional level shifter

On the other hand, when IN is high and INB is low, the transistor MN1 turns ON and MN2 turns OFF. The node OUT is still low and starts increasing only after node OUTB has dropped one threshold voltage (Vth) below V_{DDH}. Consequently MN1 has to sink the load discharge current as well as an extra short circuit current that is flowing from MP1. As a result, a conventional LS circuit cannot operate effectively.

III. HALF LATCH BASED LS

A half-latch-based level shifter circuit is shown in Fig. 2. The low voltage signals A and AN are connected to the gates of NMOS transistors M3 and M4, respectively. PMOS transistors M5 and M6 form a half-latch. On each input transition, either M3 or M4 must overcome the drive strength of the corresponding PMOS to make the half-latch switch.

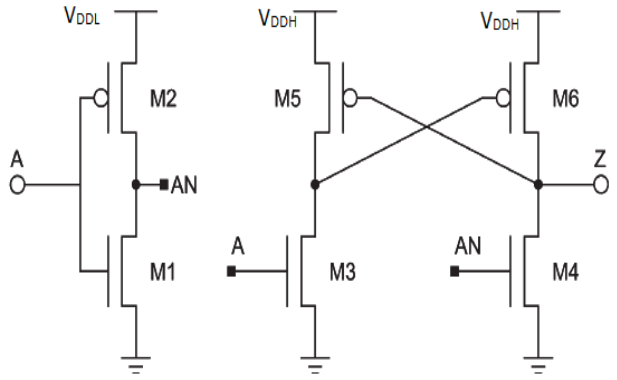

Figure 2: Half Latch based LS

Modified half latch based level shifter that uses the Wilson current mirror is presented in Fig. 3 which is a subthreshold to above-threshold level shifter. The principal part consists of transistors M3–M7. The Wilson current mirror M5–M7, operated in its overdrive region, ensures that no static current can flow through M3 or M4, if one of these transistors is switched OFF. If A is low and AN is high, M4 conducts and pulls Z low. As M3 is turned OFF, V1 is charged through M6 until M6 and M7 are also turned OFF. If A is high and AN is low, M3 conducts, leading to a current flow through M3, M5, and M6. As M6 and M7 forms a current mirror, this current also flows through M7, charging node Z. As Z rises, M5 is turned OFF so that, again, no static current can flow through M3, M5, and M6.

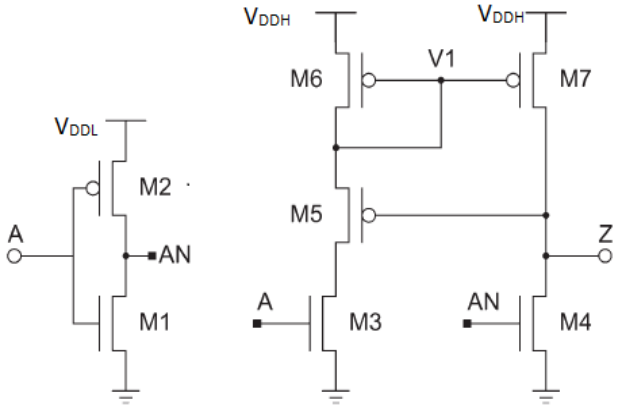

Figure 3: Modified Half Latch LS

IV. NEW PROPOSED LEVEL SHIFTERS

Conventional Level Shifters can be modified by incorporating Current mirror, Wilson current mirror and Logic Error Correction Circuit.

Following Level Shifters are proposed by incorporating suitable modifications.

1.Current Mirror based LS
2.Wilson current mirror based LS
3.LECC based LS.

A. CURRENT MIRROR BASED LS

A current mirror reads a current entering in a read-node and mirror this current (with a suitable gain factor) to an output node (nodes). PMOS current mirror is shown in Fig.4 is used to design a current mirror level shifter circuit shown in Fig.5. The current mirror level shifter can convert a deep subthreshold level to above threshold because a high drain-to-source voltage of PMOS transistors facilitates the construction of a stable current mirror, which offers an effective ON-OFF current comparison at the output node. A high amount of quiescent current occurs when the input voltage is subthreshold. This high power consumption limits the use of the current mirror level shifter. Input is applied to M3 and an inverted input is applied to the M4. MosFETS M1 and M2 form a current mirror. The drain node power of M3 is mirrored at gate of M2.

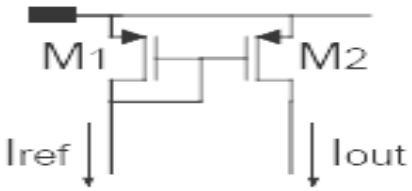

Figure 4: PMOS Current Mirror

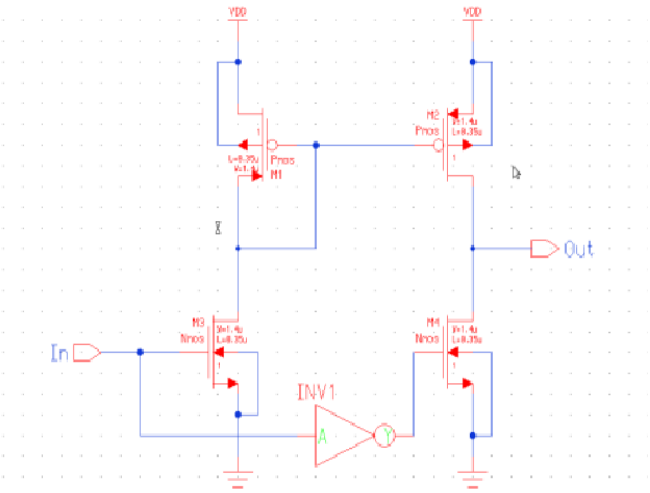

Figure 5: Current Mirror based LS

Should be legible, approximately 8 to 12 point type.

B. WILSON CURRENT MIRROR BASED LS

A Wilson current mirror is a three terminal circuit that accepts an input current at the input terminal and provides a mirrored current at the output terminal and shown in Fig.6. Fig.7 shows a level shifter that uses a Wilson current mirror (WCM), which clamps the quiescent power consumption under a subthreshold input.

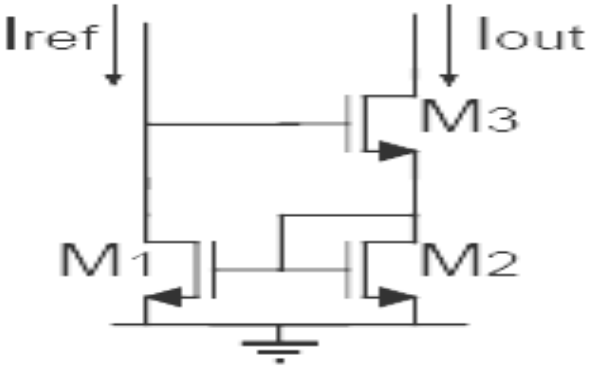

Figure 6: Wilson current Mirror

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

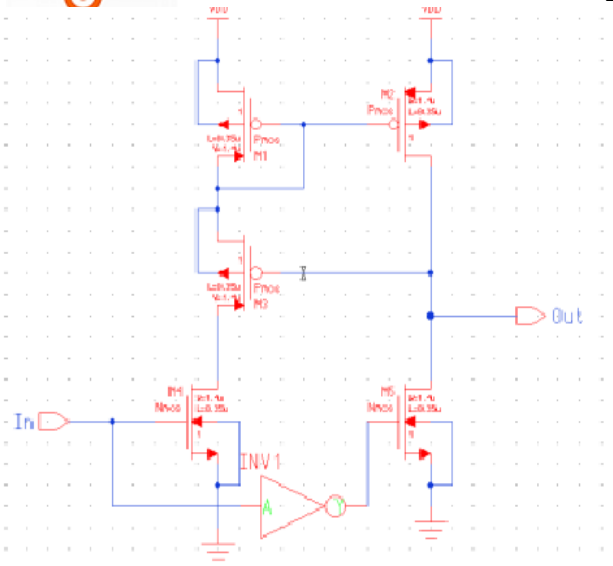

Figure 7: Wilson Current Mirror based LS

In Wilson current mirror level shifter the MOSFETs M1, M2 and M3 forms Wilson current mirror.

C. LOGIC ERROR CORRECTION BASED LS

Fig. 8 shows the schematic of the LS with Logic Error Correction Circuit (LECC). It consists of level shifter circuit and logic error correction circuit. The complementary input signals (IN an INB) and the output signal (OUT) are applied to the LECC. The LECC supplies the operating current for the level conversion circuit only when the LECC detects a logic error.

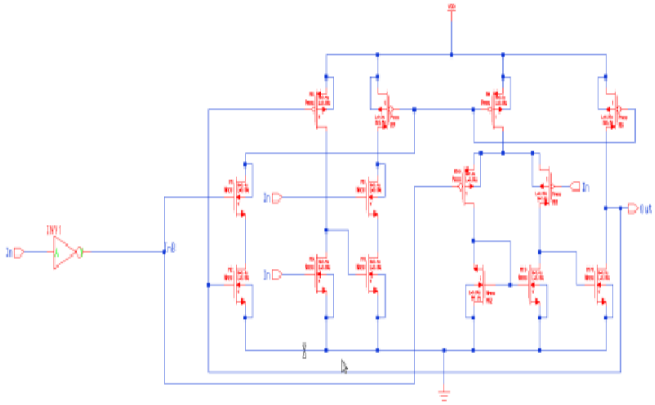

Figure 8: LECC based LS

Level Conversion Circuit: The level conversion circuit is based on a conventional two-stage comparator circuit. The comparator generates output voltage signal, OUT, according to the difference in the voltage of IN and INB. The voltage at OUT is determined by the drive currents of pull-up transistor MP6 and pull-down transistor MN8, and the currents flowing in MP6 and MN8 depend on current flowing through MP2. As both drive currents are determined by the same current, the circuit is free from the limitations discussed in the conventional ones. In the conventional comparator design, a current reference circuit needs to operate steadily. As the current reference circuit dissipates static current and increases power dissipation, it cannot be used. Logic Error Correction Circuit (LECC): The LECC consists of two circuit blocks: 1) a Low Logic Error Correction Circuit (LLECC) and 2) a High Logic Error Correction Circuit (HLECC). They are driven by IN, INB, and OUT. The LECC generates an operating current such that IN and OUT correspond to each other. When the output logic level of the LS circuit corresponds to the input logic level, the LECC does not supply current. When they do not correspond, the LECC detects the logic error, and the LLECC or HLECC supplies an operating current. As the LECC supplies an operating current only when the input and output logic levels do not correspond to each other, the power dissipation of the circuit is minimized.

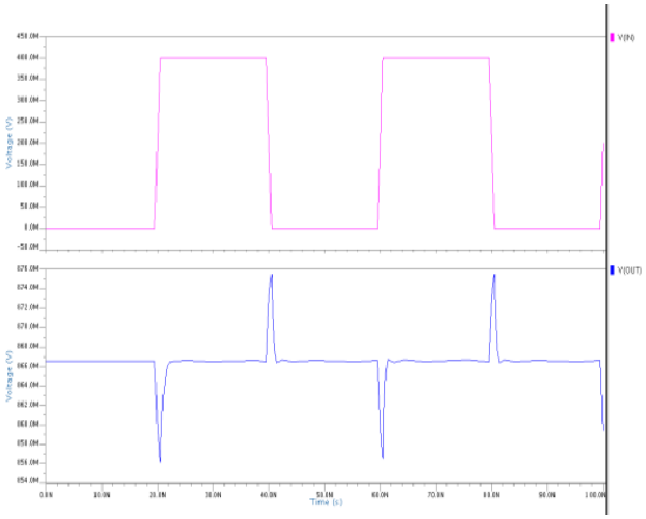

Figure 9: LECC based LS waveforms

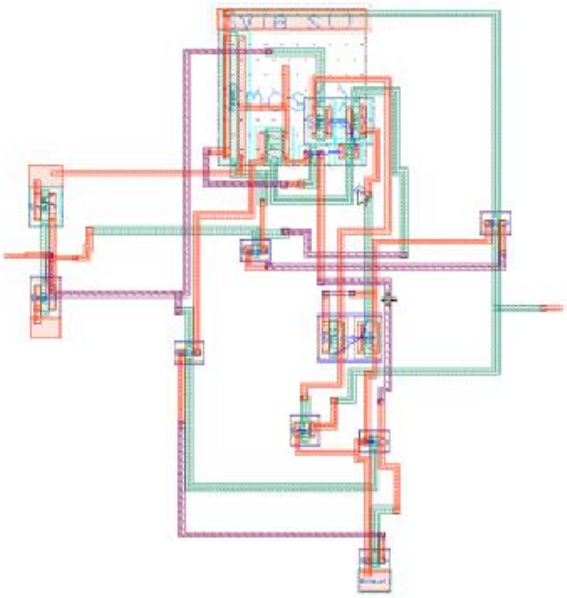

Figure 10: LECC based LS Layout

The output waveform of LEC based LS circuit is shown in Fig.9 and the layout is shown in Fig.10. LLECC: The low logic error correction circuit, LLECC, consists of two nMOSFETs (MN1 and MN2) connected in series. The LLECC operates only when OUT does not correspond to the "Low" logic of IN. When IN changes from High to Low, or when INB changes from Low to High, there is a period during which OUT does not correspond to IN. HLECC: The high logic error correction circuit, HLECC, consists of three nMOSFETs (MN3, MN4 and MN5) and a pMOSFET (MP1). In contrast to the LLECC, the circuit operates only when OUT does not correspond to the "High" logic of IN.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

When IN changes from Low to High, there is a period during which OUT does not correspond to IN. When IN and OUT correspond, the LECC does not supply any current to the level conversion circuit, except leakage current. As the voltage gain in the level conversion circuit is sufficient to keep the output node, OUT is kept at a voltage, i.e. V_{DDH} or GND.

V. RESULTS

Simulations are carried out using Mentor Graphics 130 nm technology. Performance parameters like Power dissipation, Delay and Duty cycle are computed and tabulated in Table 1.

Table 1: Comparison of Performance factors of various Level Shifters.

Model	Power dissipation	Delay	Duty cycle
Basic Level Shifter	329.01pW	–	–
Half Latch LS	329.10pW	42.604nS	513.00m
Modified Half Latch LS	304.44pW	38.187nS	470.96m
Basic Current Mirror LS	268.54pW	23.593nS	455.78m
Wilson Current Mirror LS	233.48pW	18.445nS	438.63m
LS with LECC	159.60uW	1.302nS	414.02m

VI. CONCLUSION

A level shifter circuit for extremely low-voltage digital LSIs is presented. The proposed circuits consist of a logic error correction circuit and current mirror circuits. It can convert low-voltage digital input signals into high-voltage digital output signals and achieve low power operation because it dissipates current only when the input signal changes when LECC based LS is used. The simulation results of the level shifter in a 130-nm process technology show that the circuit topology offers good performance, low power dissipation and delay.

VII. ACKNOWLEDGMENT

J. Chaitanya Varrna would like to thank Dr. R. Ramana Reddy, Professor and Mrs. D. Rama Devi, Associate Professor, ECE Department who had been guiding throughout the project and supporting me in giving technical ideas about the paper and motivating me to complete the work efficiently and successfully.

REFERENCES

[1] "A Subthreshold to Above-Threshold Level Shifter Comprising a Wilson Current Mirror" Sven Lütkemeier and Ulrich Rückert, *Member, IEEE* IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 57, NO. 9, SEPTEMBER 2010.

[2] "A Low-Power Level Shifter with Logic Error Correction for Extremely Low Voltage Digital CMOS LSIs"IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 47, NO. 7, JULY 2012.

[3] "Low-Power Level Shifter for Multi-Supply Voltage Designs", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 59, NO. 12, DECEMBER 2012.

[4] "Low energy multi-stage level converter for sub-threshold logic", www.ietdl.org, IET Comput. Digit. Tech., 2011, Vol. 5, Iss. 5.

[5] "Level-Shifter Free Design of Low Power Dual Supply Voltage CMOS Circuits Using Dual Threshold Voltages" Abdulkadir Utku Diril, Yuvraj Singh Dhillon, Abhijit Chatterjee, and Adit D. Singh, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 13, NO. 9, SEPTEMBER 2005.

[6] "The Advantages of Latch-Based Design Under Process Variation" Aaron P. Hurst, Robert K. Brayton University of California, Berkeley Berkeley.

[7] "A Robust, Input Voltage Adaptive and Low Energy Consumption Level Converter for Sub-threshold Logic", Hui Shao and Chi-Ying Tsui.

[8] "Level shifter design for low power Applications", International journal of computer science & information technology (ijcsit) vol.2, no.5, october 2010.

[9] "A Low-Power Subthreshold to Above-Threshold Voltage Level Shifter", S.Rasool Hosseini, Mehdi Saberi, *Member, IEEE,* and Reza Lotfi, *Senior Member, IEEE,* 1549-7747 (c) 2013 IEEE.

[10] "CMOS current mirrors with reduced input and output voltage requirements", V.I. Prodanov and M.M. Green.

J. Chaitanya Varma, completed his B.Tech in Electronics and Communication Engineering from St.Theressa Institute of Engineering and Technology, Chipurupalli, Andhra Pradesh, India in 2012 He is now pursuing his Master of Technology (M.Tech) in VLSI at M.V.G.R College of Engineering, Vizinagaram, Andhra Pradesh, India. His interest includes ASIC Design, and VLSI Testing.

Dr. R. Ramana Reddy, did AMIE in ECE from The Institution of Engineers (India) in 2000, M.Tech (I&CS) from JNTU College of Engineering, Kakinada in 2002, MBA (HRM & Marketing) from Andhra University in 2007 and Ph.D in Antennas in 2008 from Andhra University. He is presently working as Professor & Head, Dept. of ECE in MVGR College of Engineering, Vizianagaram. Coordinator, Center of Excellence – Embedded Systems, Head, National Instruments LabVIEW academy established in Department of ECE, MVGR College of Engineering. Convenor of several national level conferences and workshops. Published about 44 technical papers in National/International Journals / Conferences. He is a member of IETE, IEEE, ISTE, SEMCE(I), IE,ISOI. His research interests include Phased Array Antennas, Slotted Waveguide Junctions, EMI/EMC, VLSI and Embedded Systems.

Mrs. D. Rama Devi, did her B.E from Andhra University and M.Tech from JNTU University, Kakinada. She is at present, Associate Professor in Electronics and Communication Engineering, MVGR College of Engineering, Vizianagaram, Andhra Pradesh and is pursuing her research under the guidance of Prof. G.S.N Raju. Her research interests are Antenna arrays and EMI/EMC.