International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-4 Issue-2, December 2014

A Reduced Clock Power Flip-Flop for Sequential Circuits

G. Bhala Bharath, R. Ramana Reddy

Abstract— In most Very Large Scale Integration digital circuits, clock system is one of the major power consuming component. It consumes around 40% of the total system power. There is need to reduce the power consumption because power budget is severely limited on portable digital circuits. In this paper, a new Low Power Clocked Pass Transistor Flip-Flop is proposed, which will considerably reduce the number of transistors in the discharging path and also reduces the capacity of the clock load by minimizing number of clocked transistors leading to reduction in clocking power which will improve the overall power consumption. Proposed reduced clock power flip flop is compared with conventional flip flops and Parallel In Parallel Out shift register is designed using this proposed flip-flop. Simulations are done using Microwind & Tanner software tools.

Index Terms—Flip-flop, Low Power Clocking System, Microwind, Pass transistors, Shift register, Tanner.

I. INTRODUCTION

Moore's law drives the VLSI technology to continuously increase the transistor densities. There are hundreds millions of transistors or even billions of transistors on a chip today, which result in increased power consumption of VLSI chip [1]. Although the capacitances and the power supply are scaled down, the power consumption of the VLSI chip is still increasing continuously. Flip-Flops are extremely important circuit elements in all VLSI circuits. They are not only responsible for the correct timing, functionality and performance of the chip, but are also responsible for other clock distribution networks which consume a significant portion of the total power of the circuit. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power. Moreover, flip-flops have a large impact on circuit speed. The performance of the Flip-Flop is an important element that determines the performance of the entire circuit. Flip-Flops are the basic elements for storing information and they are the fundamental building blocks for all sequential circuits. Flip-flops have their content change only either at the rising or falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input changes. Conditional Discharging Flip Flop (CDFF) uses 14 clocked transistors and Conditional Capture Flip Flop (CCFF) [2] uses 14 clocked transistors.

Manuscript published on 30 December 2014.
***** Correspondence Author (s)
G. Bala Bharat, presently pursuing M. Tech Degree, VLSI Design, MVGR College, JNTU University Kakinada, Vizainagaram, India.
Dr. R Ramana Reddy, Professor & Head, Department of ECE, MVGR College of Engineering, Vizianagaram, India.

In conventional D Flip Flops like the clock signal always flows in irrespective of whether the input changes or not. Part of theclock energy is unnecessarily consumed by the internal clock buffer to control the transmission gates. Hence, if the input of the flip-flop is identical to its output, the switching of the clock can be suppressed to conserve power. A large part of the on-chip power is consumed by the clock drivers. It is desirable to have less clocked load in the system.

II. CONDITIONAL DATA MAPPING D FLIP-FLOP

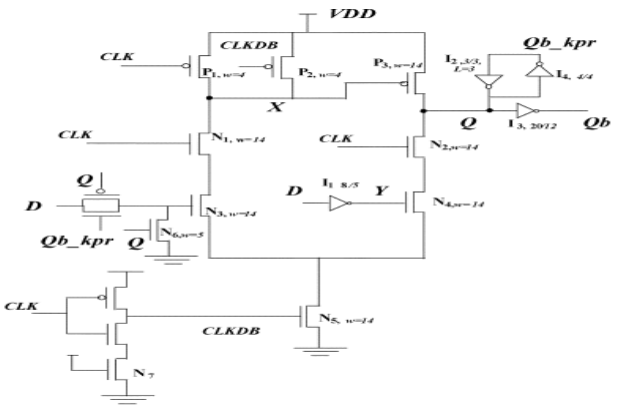

Fig. 1. Conditional Data Mapping Flip flop Design

Conditional Data Mapping Flip Flop (CDMFF) [3]used only 7 clocked transistors, resulting in about 50% reduction in the number of clocked transistors.The Fig.1 shows the Conditional Data Mapping Flip Flop Design. There is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the precharging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on criticalpath because its first stage is dynamic. When clock signal CLK transits from 0 to 1, CLKDB will remain 1 for a short period of time, which produces an implicit pulse window for evaluation. During that window, both P1, P2 are off. In addition, if D transits from 0 to 1, the pull down network will be disconnected by N3 using data mapping scheme (N6 turns off N3); If D is 0, the pull down network is disconnected from GND. Hence internal node X is not connected with Vdd or GND. During pulse windows, it is essentially floating periodically. With feature size shrinking, dynamic node is more prone to noise interruption because of the undriven dynamic node.

If a nearby noise discharges the node X, PMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nano scale circuit, a glitch not only consumes power but could propagate to the next stage which makes the system more vulnerable to noise. Hence, CDMFF could not be used in noise intensive environment.

III. CLOCK PAIR SHARED FLIP-FLOP DESIGN

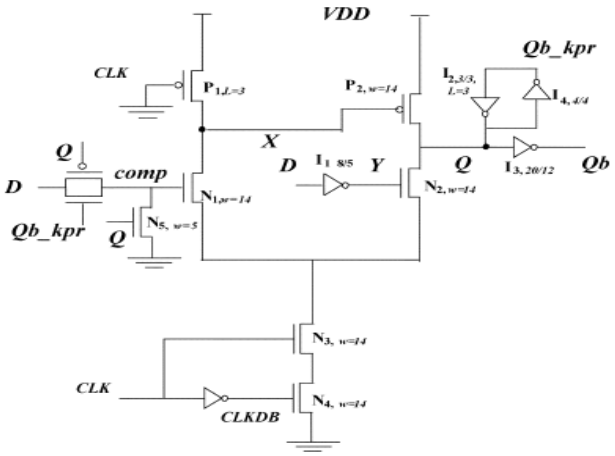

Fig. 2. Clock Pair Shared Flip-Flop Design

Clocked Pair Shared Flip Flop (CPSFF) [4] used only 4 clocked transistors. Clocked Pair Shared flip-flop (CPSFF) showing in Fig.2 uses less clocked transistors than CDMFF and overcomes the floating problem in CDMFF. In the clocked-pair-shared flip-flop, clocked pair is shared by first and second stage. The p-MOS transistor P1is always ON and is used to charge the internal node rather than using the two clocked pre charging transistors (P1,P2) in CDMFF. Comparing with CDMFF, a total of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. CPSFF uses four clocked transistors rather than seven clocked transistors in CDMFF, resulting in approximately 40% reduction in number of clocked transistors [6].

IV. PROPOSED LOW POWER CLOCKED PASS TRANSISTOR FLIP-FLOP DESIGN

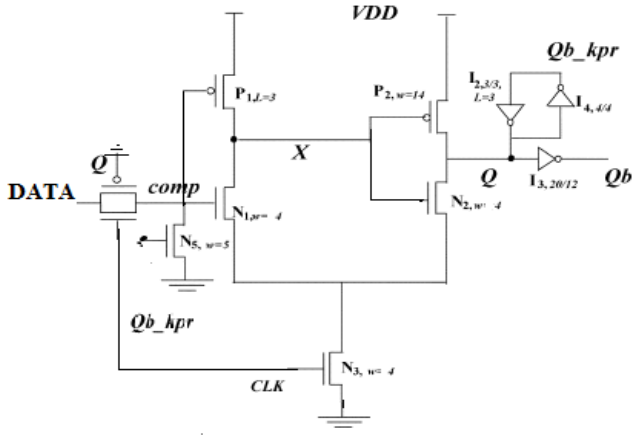

Fig. 3. Proposed Low Power Clocked Pass Transistor flip-flop

Proposed Low power Clocked Pass Transistor Flip-Flop is Designed [5-8] by using Pass Transistor Logic family, In this designonly one clocking transistor is used so that it will consume less power in the clock network of the Flip flop.

When clock signal CLK transits from 1 to 0,P1 is conducting then node X is precharged and Q is'0', QB is '1', at that time Data 0 or 1. When clock signal CLK transits from 0 to 1,P1 is not conducting then node X is discharged and Q is'1', QB is '0', at that time Data '1'.By using the proposed flip flop, power consumption and area required are reduced compared to other conventional flip flops, and also delay factor is reduced due to the reduced number of transistors. Therefore, the proposed low power flip flop can be used in design of sequential circuits to meet low power and area requirements. The operating condition used in simulations is 500 MHz/1.0V.

V. SIMULATION OF VARIOUS FLIP-FLOP DESIGNS

Since pulse width design is crucial to the correctness of data capturing as well as the power consumption, the pulse generator logic in all designs is first sized to function properly across process variation. All designs are further optimized subject to the tradeoffs between power and D-to-Q delay, i.e., minimizing the product of the two terms. The target technology is the UMC 90-nm and CMOS process is used. The layouts are designed using Microwind tool and are presented in Fig.4 to 6 for CDMFF, CPSFF, LPCPFF respectively. The Simulation results with inputs, outputs and power consumed are presented in Fig.7 to 9 for CDMFF, CPSFF, LPCPFF respectively.

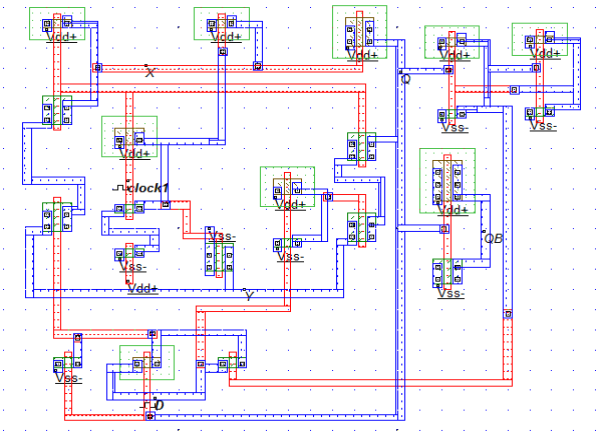

Fig. 4. Conditional Data Mapping Flip-Flop layout

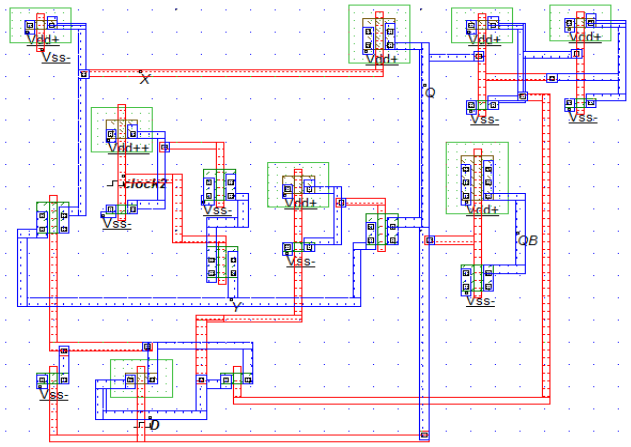

Fig. 5. Clock Pair Shared Flip-Flop layout

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

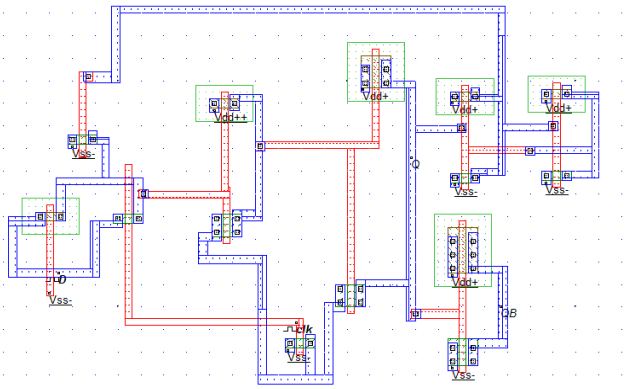

Fig. 6. Low Power Clocked Pass transistor Flip Flop layout

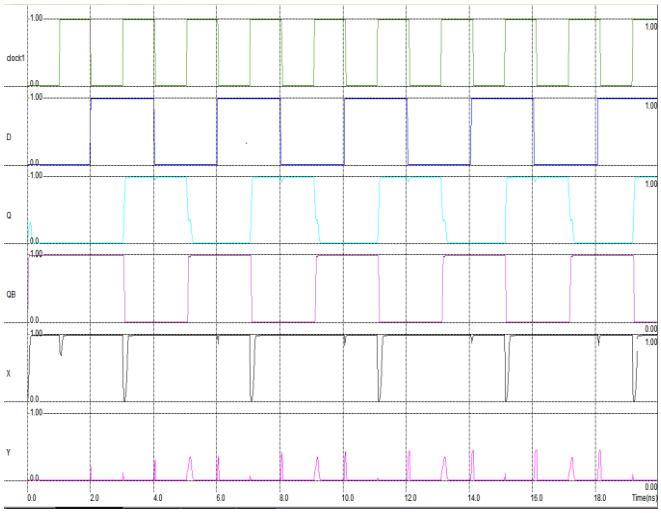

Fig. 7. Power consumed by CDMFF

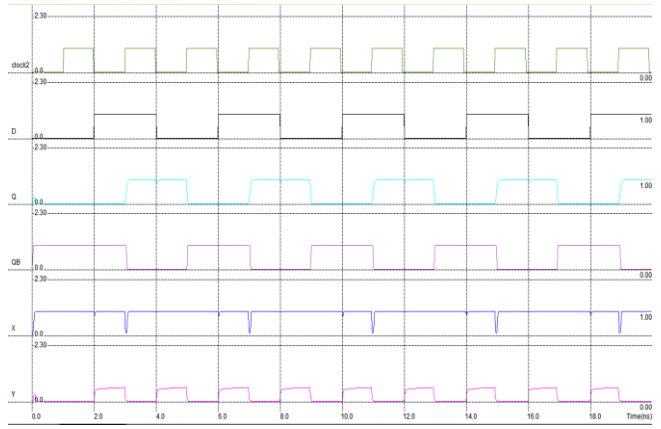

Fig. 8. Power consumed by CPSFF

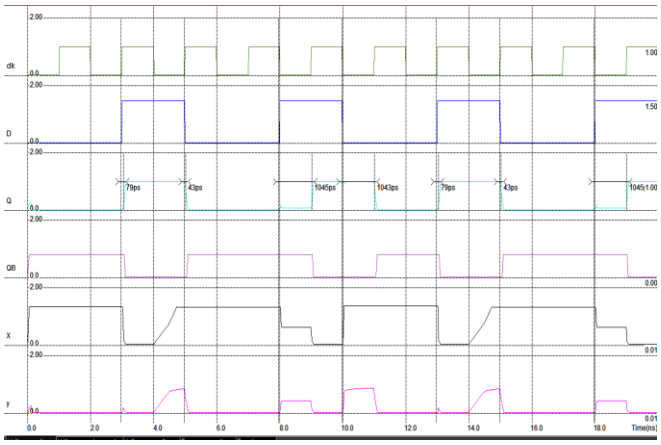

Fig. 9. Power consumed by LPCPFF

TABLE I. Comparison of Various P-Ff Designs

P-FF	CDMFF	CPSFF	LPCPFF
No. of Transistors	22	19	14
Area(um^2)	130.8	123.6	107.7
Average Power (uw)	5.54	4.83	2.87

VI. SHIFT REGISTERS

Shift register is a sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states [10]. All flip-flops are driven by a common clock. The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity. For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits.

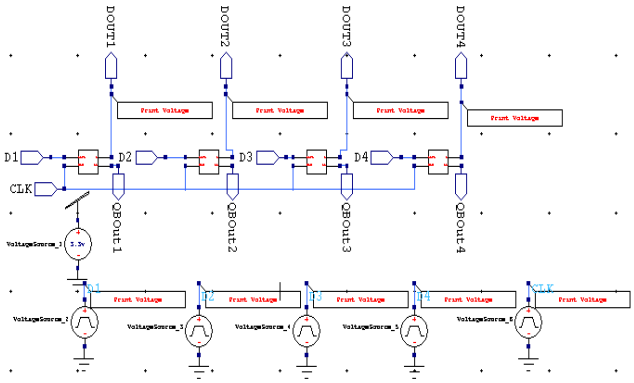

Fig. 10. Schematic of Parallel in Parallel out Shift Register

VII. SIMULATION OF SHIFT REGISTERS

Simulations are carried out using Microwind tool. Parallel in Parallel out shift registers are designed using CDMFF, CPSFF and LPCPFFs and layout designs are shown in Fig.11,12 &13 respectively. The simulation results are shown in Fig.14, 15 and 16 respectively. The power consumption is also shown on the right bottom portion of the window.

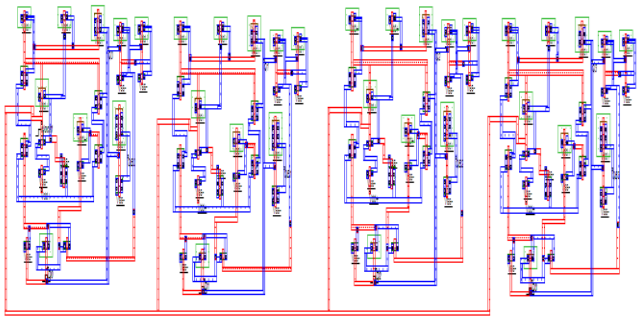

Fig. 11. Parallel in Parallel out Shift Register using CDMFF in Micro wind tool

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

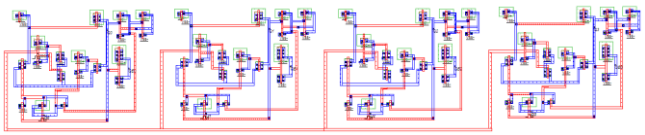

Fig. 12. Parallel in Parallel out Shift Register using CPSFF in Soft Ware Microwind tool

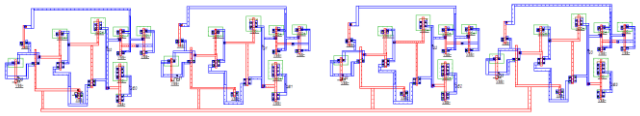

Fig. 13. Parallel in Parallel out Shift Register using LPCPFF in Soft Ware Microwind tool

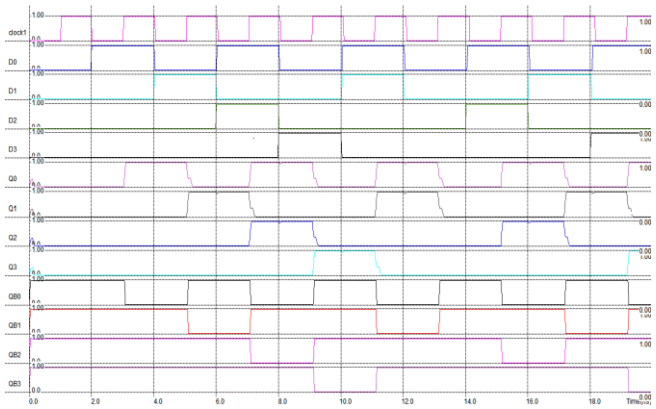

Fig. 12. Power consumed by Parallel in Parallel out Shift Register using CDMFF

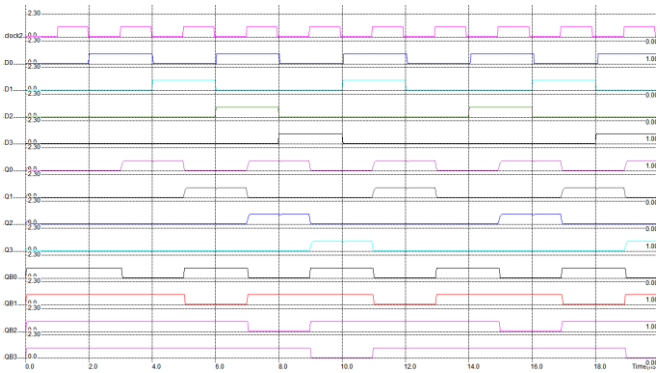

Fig. 13. Power consumed by Parallel in Parallel out Shift Register using CPSFF

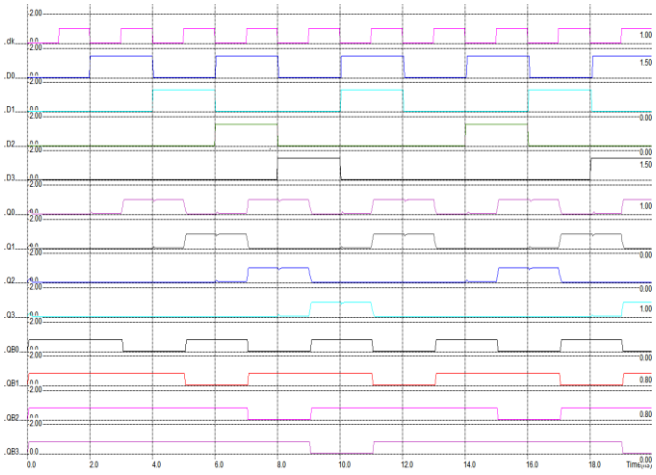

Fig. 14. Power consumed by Parallel in Parallel out Shift Register using LPCPFF

TABLE II. Comparison of Various Parallel in Parallel out Shift Register Designs

Parameters	PIPO Shift Register Using CDMFF	PIPO Shift Register Using CPSFF	PIPO Shift Register Using LPCPFF
No. of Transistors	88	76	36
Area(um^2)	677.3	623.7	98.2
Average Power (uw)	15.243	12.227	9.686

VIII. CONCLUSION

The Low Power Clocked Pass Transistor Flip Flop (LPCPTFF) in the clocked load resulting in reduction in number of Transistors and Power consumption and Delay. LPCPFF uses less number of transistors compared to CDMFF and CPSFF resulting in reduced area and delay. Power consumption in LPCPFF is reduced by 51.8% compared to CDMFF and 59.4% compared to CPSFF. Parallel In Parallel Out shift registers are designed using proposed technique and it is observed that LPCFF occupies less area and consumes less power compared to other techniques. From the results obtained, it is evident that LPCPFF is more power efficient, fast and occupies less area. Hence this flip flop is very much useful in computer systems and in SOC applications.

REFERENCES

[1] Peiyi Zhao, Jason McNeely, WeidongKuang, Nan Wang, and Zhongfeng Wang "Design of Sequential Elements for Low Power Clocking System" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 5, May 2011

[2] Seyed E. Esmaeili, Asim J. Al-Kahlili, and Glenn E. R. Cowan "Low Swing Differential Conditional Capturing Flip-Flop for LC Resonant Clock Distribution Networks" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 8, aug 2012.

[3] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki, "Conditional data mapping flip-flops for low-power and high-performance systems," IEEE Trans. Very Large Scale Integr. (VLSI), vol.14, no.12, Dec. 2006.

[4] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp.1263–1271, Aug. 2001.

[5] H. Kawaguchi and T. Sakurai, "A Reduced Clock-Wing Flip-Flop (RCSFF) for 63% power reduction," IEEE Solid-State Circuits, vol.33, no. 5, pp. 807–811, May 1998.

[6] A. Chandrakasan, W. Bowhill, and F. Fox, "Design of High-Performance Microprocessor Circuits," 1st ed. Piscataway, NJ: IEEE Press, 2001.

[7] J.Tschanz, S.Narendra, Z.P.Chen, S.Borkar, M.Sachdev, and V. De, "Comparative delay and energy of single edge-triggered & dual edge triggered pulsed flip-flops for high-performance microprocessors," in Proc. ISPLED, Huntington Beach, CA, Aug. 2001, pp.207–212.

[8] P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, W. D. Kuang, and B. Barcenas, "Low power clock branch sharing double-edge triggered flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 3, pp. 338–345, Mar. 2007.

[9] Nayeem, N.M. ; Dept. of Comput. Sci. & Eng., Univ. of Dhaka, Dhaka, Bangladesh ; Hossain, M.A. ; Jamal, L. ; Babu, H.M.H., " Efficient Design of Shift Registers Using Reversible Logic,"IEEE International Conference on Signal Processing Systems, Pg nos474 – 478,15-17 May 2009

[10] A. J. Nichols "Minimal shift-register realizations of sequential machines", *IEEE Trans. Electronic Computers*, vol. EC-14, pp.688 - 700 1965

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)

G. Bala Bharat, received his B.Tech degree from PVP Siddhartha College, JNTU University in Vijayawada in the year 2010 and presently pursuing M.Tech degree in VLSI Design in MVGR College, JNTU University kakinada, Vizainagaram. His interests include Digital IC Design&Verification, Mixed Signal design

Dr. R. Ramana Reddy, did AMIE in ECE from The Institution of Engineers (India) in 2000, M.Tech (I&CS) from JNTU College of Engineering, Kakinada in 2002, MBA (HRM & Marketing) from Andhra University in 2007 and Ph.D in Antennas in 2008 from Andhra University. He is presently working as Professor & Head, Dept. of ECE in MVGR College of Engineering, Vizianagaram. Coordinator, Center of Excellence – Embedded Systems, Head, National Instruments LabVIEW academy established in Department of ECE, MVGR College of Engineering. Convener of several national level conferences and workshops. Published about 32 technical papers in National/International Journals / Conferences. He is a member of IETE, IEEE, ISTE, SEMCE(I), IE,ISOI. His research interests include Phased Array Antennas, Slotted Waveguide Junctions, EMI/EMC, VLSI and Embedded Systems.

Published By:
Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP)