

# Area Efficient Higher Order FIR Filter Design using Improved Distributed Arithmetic with Look up Tables

R. Santosh, K. V. Lalitha Bhavani

**Abstract-** This paper describes the design and implementation of highly efficient LUT based circuit for the implementation of FIR filter using Distributed arithmetic algorithm. It is a multiplier less fir filter designed and designed based on distributed arithmetic algorithm. The DA based technique consists of Look Up Table (LUT), shift registers and scaling accumulator. Analysis on the performance of filter order with partition on different address length of partial tables are done using Xilinx 12.1 synthesis tool. The proposed architecture provides an efficient area-time-power implementation which improves latency and less area-delay complexity through pipelining technique when compared with existing structures for FIR Filter.

**Index Terms--**Distributed Arithmetic (DA), FIR filter, Look up table (LUT), FPGA.

## I. INTRODUCTION

FIR filters are used intensively in video and communication systems, high performance in speed, area and power consumption is demanded. Basically, digital filters are used to modify the characteristic of signals in time and frequency domain and have been recognized as primary digital signal processing [1]. In signal processing, the design methods were mainly focused in multiplier-based architectures to implement the multiply-and- Accumulate (MAC) blocks that constitute the main component in FIR filters and several functions [2]. The FIR filter is represented as

$$y[n] = \sum_{k=0}^{N-1} c[k]x[n-k] \quad (1)$$

Where  $y[n]$  is the FIR filter output,  $x[n-k]$  is input data and  $c[k]$  represents the filter coefficients Eq. (1) shows that multiplier-based filter implementations may become highly expensive in terms of area and speed. This issue has been partially solved with the new generation of low-cost FPGAs that have embedded DSP blocks [3]. The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches. Distributed Arithmetic (DA) algorithm appeared as a very efficient solution especially suited for LUT-based FPGA architectures. Croisier et al [7] had proposed the multiplier less architecture of DA algorithm and it is based on an efficient partition of the function in partial terms using 2's complement binary representation of data.

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Many DSP applications use the function such as convolution, correlation and filtering. Inner product computations are important for this function. This inner product computation is done using the Distributed Arithmetic principles. The partial terms can be pre-computed and stored in LUTs. Yoo et al. [8] observed that the requirement of memory/LUT capacity increases exponentially with the order of the filter, given that DA implementations need  $2K$  – words,  $K$  being the number of taps of the filter. The work in this paper presents the design and implementation of parallel distributed algorithm for FIR filter target as Spartan 3E FPGA. The results of the implementation experiment are analyzed in terms of parameters such as area and speed. The brief description of the distributed algorithm is presented in Section 2. The implementation of the proposed technique for FIR filters is discussed in Section 3. The Section 4 presents the implementation results. The last section concludes the work and presents the future work.

## II. IMPROVED DISTRIBUTED ARITHMETIC (IDA)

Distributed arithmetic (IDA) is an important FPGA technology.

$$y[n] = \langle c, x \rangle = \sum_{k=0}^{N-1} c[k]x[n-k] \quad (2)$$

DA system, assumes that the variable  $x[n]$  is represented by-

$$x[n] = \sum_{b=0}^{B-1} x_b[n]2^b, x_b[n] \in [0,1] \quad (3)$$

If  $c[n]$  are the known coefficients of the FIR filter, then output of FIR filter in bit level form is:

$$y[n] = \sum_{k=0}^{N-1} c[n] \sum_{b=0}^{B-1} x_b[n]2^b \quad (4)$$

In distributed arithmetic form-

$$y = \sum_{b=0}^{B-1} 2^b \times \sum_{n=0}^{N-1} f(c[n], x_b[n]) \quad (5)$$

In Eq. (5) second summation term realizing as one LUT. The use of this LUT or ROM eliminates the multipliers [9]. For signed 2's complement number output of FIR filter can be computed as- In Eq. (5) second summation term realizing as one LUT. The

$$y = -2^B x f(c[n], x_B[n]) + \sum_{b=0}^{B-1} 2^b \times \sum_{n=0}^{N-1} f(c[n], x_b[n]) \quad (6)$$

Where  $B$  represents the total number of bits used. Fig 1 shows the Distributed architecture for FIR filter and different with the MAC architecture. use of this LUT or ROM eliminates the multipliers [9]. For signed 2's complement number output of FIR filter can be computed as-  
When  $x[n] < 0$ , Binary representation of the input is [10], The output in distributed arithmetic form-

$$x[n] = -x_b[0] + \sum_{b=1}^{B-1} x_b[n]2^{-b} \quad (7)$$

If the number of coefficients  $N$  is too large to implement the full word with a single LUT (Input LUT bit width = number of coefficients), then partial tables can be and add the results as shown in Fig2. If pipeline registers are also added, then this modification will not reduce the speed, but can dramatically reduce the size of the design [8].

$$y = -(\sum_{n=0}^{N-1} c[n]x_b[0] + \sum_{b=1}^{B-1} (\sum_{n=0}^{N-1} c[n]x_b[n])2^{-b}) \quad (8)$$

If the number of coefficients  $N$  is too large to implement the full word with a single LUT (Input LUT bit width = number of coefficients), then partial tables can be and add the results as shown in Fig2. If pipeline registers are also added, then this modification will not reduce the speed, but can dramatically reduce the size of the design [8].

### 2.1 Serial Distributed Arithmetic

In conventional MAC method with a limited number of MAC engines, as the filter length is increased, the system sample rate is decreased. This is not the case with serial DA architectures since the filter sample rate is decoupled from the filter length. As the filter length is increased, the throughput is maintained but more logic resources are consumed. Though the serial DA architecture is efficient by construction, its performance is limited by the fact that the next input sample can be processed only after every bit of the current input samples is processed. Each bit of the current input samples takes one clock cycle to process.

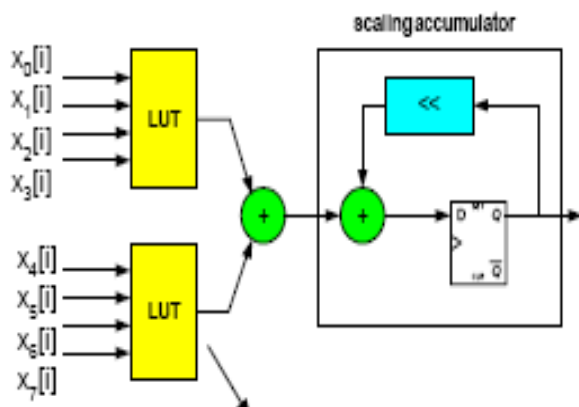


Fig. 1: Serial DA FIR Filter Block Diagram

### 2.2 Parallel Distributed Arithmetic

The performance of the circuit can be improved by modifying the architecture to a parallel architecture which processes the data bits in groups. Figure 2.3.3.1 shows the block diagram of a 2 bit parallel DA FIR filter. The tradeoff here is performance for area since increasing the number of bits sampled has a significant effect on resource utilization on FPGA. For instance, doubling the number of bits sampled, doubles the throughput and results in the half the number of clock cycles. This change doubles the number of LUTs as well as the size of the scaling accumulator. The number of bits being processed can be increased to its

maximum size which is the input length  $n$ . This gives the maximum throughput to the filter. For a fully parallel implementation of the DA filter (PDA), the number of LUTs required would be enormous. In this work we show an alternative to the PDA method for implementing high speed FIR filters that consumes significantly lesser area and power.

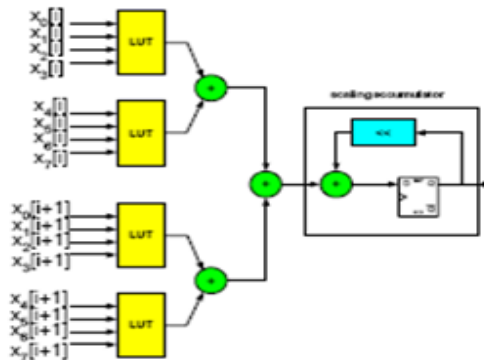
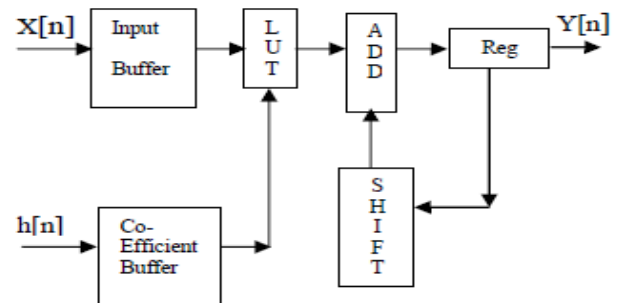


Fig. 2: Parallel DA FIR Filter Block Diagram

### 2.3 Dynamic Distributed Arithmetic:

A popular technique for implementing the transposed form of FIR filters is the use of a multiplier block, instead of using multipliers for each constant as shown in Figure 2.3.4.1. The multiplications with the set of constants  $\{h_k\}$  are replaced by an optimized set of additions and shift operations, involving computation sharing. Further optimization can be done by factorizing the expression and finding common sub expressions. The performance of this filter architecture is limited by the latency of the biggest adder and is the same as that of the PDA.



## III. FIR FILTER DESIGN

To evaluate the performance of the Distributed Arithmetic in parallel scheme for symmetric FIR filters are designed and synthesized using Xilinx ISE 12.1 Target as a Spartan 3E (Xc3s500E-FT256) FPGA device and the results are compared to conventional FIR filter. ISE design software offers a complete design suit based programmable logic devices on Xilinx ISE. The design can be simulated and synthesized in the form of schematic or HDL entry on Xilinx ISE platform. Spartan 3E FPGA can be programmed directly from Xilinx ISE in configuration logic blocks interconnected with switching matrix. Spartan 3E has specialized mechanism for DSP design that can be designed for less resources, high speed and low power.



The designed FIR filter is programmed in verilog HDL language [12]. The proposed design is designed for small memory location LUT and also for large memory location LUT to analyze the performance of the proposed design for speed and area parameters. In the present work, the proposed design is analyzed through 4 –tap DA.

### 3.1 FILTER DESIGN PROCEDURE:

#### DESIGN METHODOLOGY AND SPECIFICATIONS

FIR filters specifications:

- 16th-order FIR filter (Band pass Filter)
- Sampling frequency is : 2.25 MHz
- The pass band cutoff frequency is :100 kHz
- Width of the input data : 16 bits
- Length of the input data : 07
- Width of the output data : 16 bits
- Length of the output data : 22
- The filter coefficient is : 20 bits

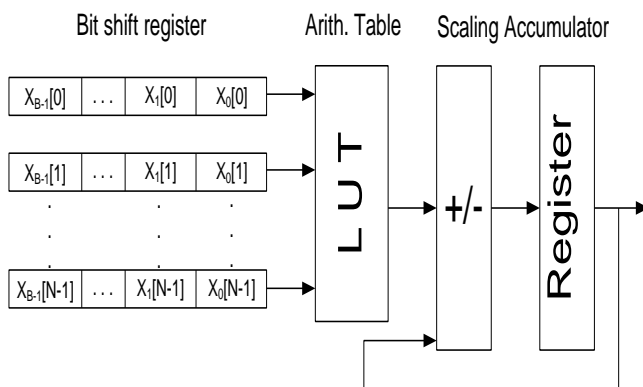


Fig. 1 DA Block Diagram

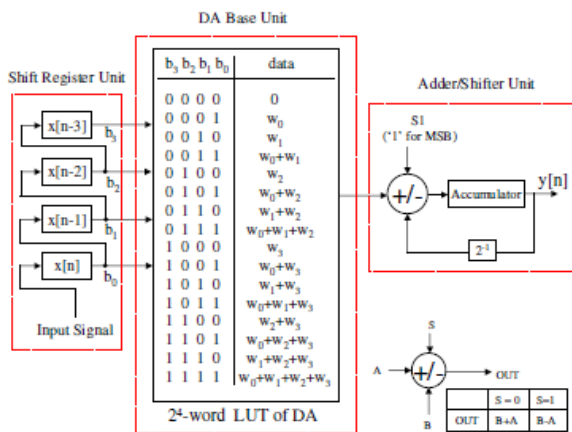


Fig. 2 LUT based DA Implementation of a 4-tap (K = 4) FIR Filter

### 3.2 ACCUMULATOR:

The accumulator module is to add reactive power of all harmonics but we need not consider all the 64 samples in the FFT output. It is enough to consider only first 32 samples in the FFT output. The 32 samples which we require will not be in the normal order. Since we are following the radix\_4 algorithm. Therefore the samples which we require are the first two samples in each iteration. There will be 16 iterations and hence required 32 samples are available.

## IV. DISCUSSION

The implementation results of 4-tap FIR filter after applying the distributed arithmetic algorithm as shown in Table 1. The 4-tap parallel DA FIR filter take high speed and lowest power dissipation in comparison to conventional FIR filter as shown in Table 1. For small tap filters, the parallel DA algorithm saves 50 % of the area and cost in comparison to the conventional design techniques. The speed is approximately and 3 times in parallel DA is achieved and very less power is consumed in comparison to simple FIR filter.

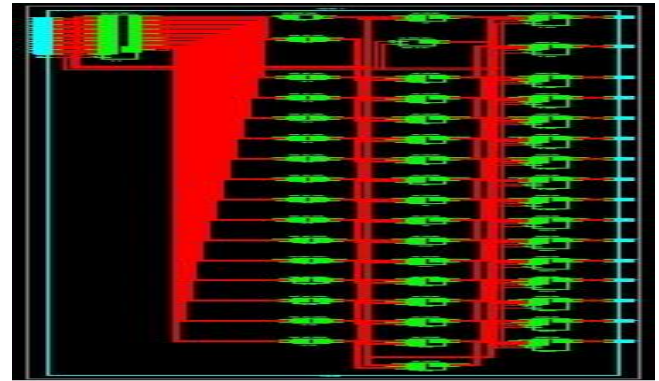


Fig. 5: RTL view of 4 tap FIR Filter

The FIR filter design using improved DA algorithm has been designed onto a Xilinx Spartan XC3S500E FT256 chip. The chip is having 9312 LUT's and a maximum of 2868 are used. A maximum of 1506 are used out of 4656 slices which results to 32%. Spartan XC3S500E FT256 is one of the primitive chips and after it several chips of greater densities have been released. The current design of FIR filter occupies around a maximum of 30%. of the total chip space there by leaving a lot of space for fitting the other components present in a bigger and complete SOC IC.

/tb_fir_top/x0	00001010	00001010
/tb_fir_top/x1	00001010	00001010
/tb_fir_top/x2	00001010	00001010
/tb_fir_top/x3	00001010	00001010
/tb_fir_top/x4	00001010	00001010
/tb_fir_top/x5	00001010	00001010
/tb_fir_top/x6	00001010	00001010
/tb_fir_top/x7	00001010	00001010
/tb_fir_top/x8	00001010	00001010
/tb_fir_top/x9	00001010	00001010
/tb_fir_top/x10	00001010	00001010
/tb_fir_top/x11	00001010	00001010
/tb_fir_top/x12	00001010	00001010
/tb_fir_top/x13	00001010	00001010
/tb_fir_top/x14	00001010	00001010
/tb_fir_top/x15	00001010	00001010
/tb_fir_top/y0	0000000100101011	0000000100101011
/tb_fir_top/y1	0000010010100111	0000010010100111
/tb_fir_top/y2	0001001010001011	0001001010001011
/tb_fir_top/y3	0010100111100101	0010100111100101
/tb_fir_top/y4	0111110110100011	0111110110100011
/tb_fir_top/y5	0001010110000011	0001010110000011
/tb_fir_top/y6	0110001011011110	0110001011011110
/tb_fir_top/y7	0011101000101111	0011101000101111
/tb_fir_top/y8	0100101101101111	0100101101101111

Fig. 5: Simulation of 4 Tap FIR Filter

Table 1. Synthesis and Simulation Result for 4 tap FIR Filter

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	1501	4656	32%
Number of Slice Flip Flops	379	9312	4%



Number of 4 input LUTs	2868	9312	30%
Number of GCLKs	2	24	8%

## V. CONCLUSION AND FUTURE WORK

The complicated multiplication-accumulation operation is converted to the shifting and adding operation when the DA algorithm is directly applied to realize FIR filter. Aiming at the problems of the best configuration in the coefficient of FIR filter, the storage resource and the calculating speed, the DA algorithm is optimized and improved in the algorithm structure, the memory size and the look-up table speed. The arithmetic expression has clear layers of derivation process and the circuit structure is reasonable, which make the memory size smaller and the operation speed faster. The design improves greatly compared to the conventional FPGA realization and it can be flexibility applied to implement high-pass, low-pass and band-stop filters by changing the order and the LUT coefficient.

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