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Small-Signal Amplifiers with BJT, FET and MOSFET in Triple Darlington Topology

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Abstract*— Circuit models of two discretely developed small-signal amplifiers are proposed and qualitatively analyzed perhaps for the first time. Design of first amplifier uses Triple Darlington topology based hybrid unit of BJT-JFET-MOSFET in RC coupled voltage divided biasing network with two additional biasing resistances. However the second amplifier uses JFET-BJT-MOSFET hybrid unit in the similar circuit design. Both the amplifiers successfully amplify small-signals swinging in 1-10mV range at 1KHz frequency. These circuits simultaneously produce high voltage gain (≈ 291 and 345 respectively) and current gain (≈ 719 and 27K respectively) in narrow bandwidth region (≈ 8KHz and 13KHz respectively). Variations of maximum voltage gain with different biasing resistances and DC supply voltage, temperature sensitivity of performance parameters, THDs, small-signal AC equivalent circuit analysis and noise performance of the circuits are elaborately studied and discussed. The proposed amplifiers may be useful for those applications where high voltage and current gain would be the prime requirement of amplification in narrow band frequency region. Moreover, the proposed circuits may also useful for radio and TV receiver stages and low-frequency power sources.

Index Terms*— Small-signal amplifiers, Darlington amplifiers, Compound Darlington configurations, Triple Darlington topology.

I. INTRODUCTION

Most of the electronic systems require amplifiers for scaling signals to a useful level [1]-[3]. The output signals from these systems are often too small in magnitude to be processed reliably for any useful function [2]-[4]. Usually, practical amplifiers employ non-linear devices in their circuits and thus exhibit non-linear characteristics. However, there is a region in the mid-band frequency range where the voltage or current gain remains constant. If the amplifiers are configured to operate in this region, a small variation in the input signal causes more-or-less linear variation in the corresponding output. This is achieved by biasing amplifiers to operate at a specific quiescent point. A Darlington pair (conventionally a compound unit of two identical BJTs) acts as good amplifier if operated in the linear region. Principally, this paired unit enjoys high input resistance, low output resistance and voltage gain approximately equal to unity. It has superior characteristics regarding current gain due to which it is generally employed for the design of output stages in operational amplifiers [3], [4].

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However, a major drawback is encountered with the performances of conventional Darlington pair or Triple Darlington based amplifiers. At higher frequencies their responses become poorer than that of a single transistor amplifier [3]-[7]. To overcome this problem, a number of modifications are attempted in Darlington pair amplifiers. These modifications include addition of extra biasing resistances in respective amplifier, use of identical active devices in Triple Darlington topology and replacement of BJTs of the (Darlington) pair with other active devices like JFETs or MOSFETs [5],[7]-[10]. However use of dissimilar active devices or hybrid combination of unlike active devices in Darlington's topology is still a challenging area for electronic circuit designers to work with [8],[11],[12]. In the present manuscript, authors proposed two circuit models of small-signal amplifiers using hybrid combination of BJT, JFET and MOSFET in Triple Darlington topology. The proposed amplifiers are well suited for the stages requiring simultaneously high voltage and current gain in narrow band frequency region.

II. CIRCUIT DESCRIPTION

Present work includes a qualitative comparison between two differently configured small-signal amplifier circuits which are mentioned in the manuscript as 'Proposed amplifier-1' (Fig.1) and 'Proposed amplifier-2' (Fig.2).

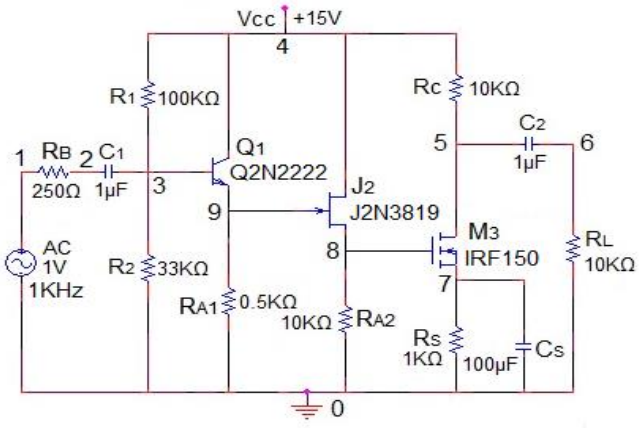

Fig. 1: Proposed Amplifier-1

Circuit designs of these amplifiers use potential divider biasing methodology and consist BJT (NPN with β=255.9), JFET (N-Channel with V_{TH}= -1.422) and MOSFET (N-MOS with V_{TH}= 2.831) in Triple Darlington topology based compound units [8],[12]. The compound unit of proposed amplifier-1 (Fig.1) uses BJT at driver position whereas proposed amplifier-2 (Fig.2) uses JFET as driver.

Two additional biasing resistances R_{A1} and R_{A2} are employed in the circuits of proposed amplifiers which provide them proper biasing against Triple Darlington compound units of unlike active devices.

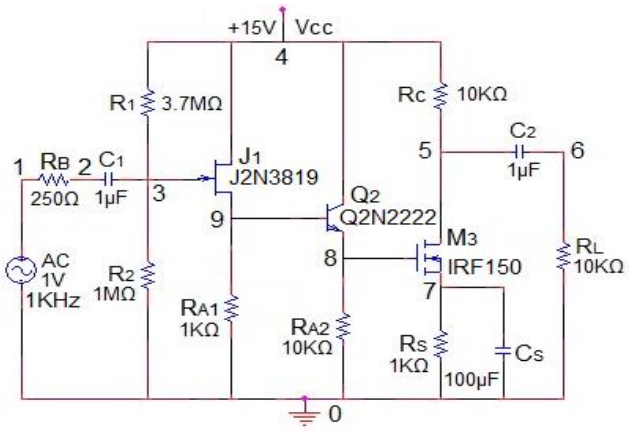

Fig. 2: Proposed Amplifier-2

The amplifiers under discussion are biased with +15V DC power supply. Respective observations are made by feeding the amplifier circuits with 1V AC input signal source from which, a small and distortion less AC signal of 1mV for both the amplifiers at 1KHz frequency is drawn as input for the amplification purpose. All the observations mentioned in the present manuscript are furnished through PSpice simulation software [3]-[5], [7], [9]-[13]. Biasing components and their values are listed in TABLE I.

III. Results and Discussions

The amplifiers of Fig.1 and Fig.2 provide fair and distortion-less results for 1-10mV AC input signals.

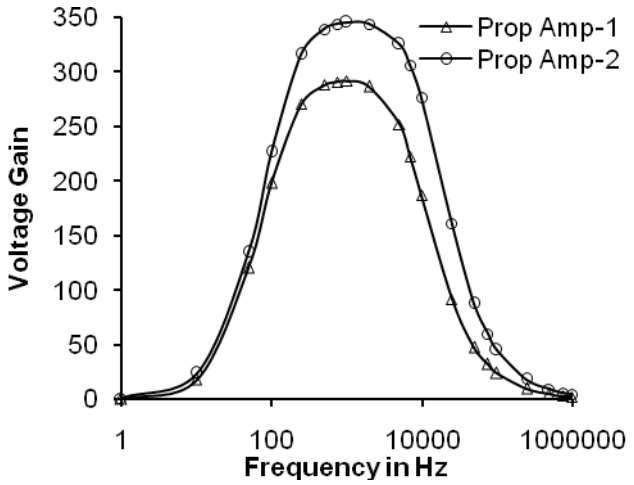

Fig. 3: Variation of Voltage Gain with Frequency

Fig.3 shows the variation of voltage gain as a function of frequency. At depicted biasing parameter values, Proposed amplifier-1 (Fig.1) produces 291.494 maximum voltage gain A_{VG} (with peak output voltage V_{OP} =297.263mV), 7.2088 maximum current gain A_{IG} (with peak output current I_{OP}= 29.726μA) and 8.286 KHz bandwidth B_W (with lower cut-off frequency f_L=108.369Hz and upper cut-off frequency f_H=8.286 KHz). However, the Proposed amplifier-2 (Fig.2) produces 345.562 A_{VG} (with V_{OP} =350.343mV), 27.212K A_{IG} (with I_{OP}=35.034μA) and 13.089 KHz B_W (with f_L=155.77Hz and f_H=13.245 KHz). Respective values of voltage and current gains logically set power gain of the proposed amplifiers considerably larger than unity. Simultaneously, both the amplifiers (Fig.1 and Fig.2) effectively remove the problem of poor response of conventional Darlington pair or Triple Darlington amplifiers at higher frequencies [3],[5],[7],[10]. It is to be noted that both the amplifiers under discussion show phase reversal in respective output waveforms [5],[7],[8],[12]. The phase reversal property of independent active devices is responsible to produce 180° phase difference in the output waveform of proposed amplifiers which are using composite unit of BJT-JFET-MOSFET and JFET-BJT-MOSFET in their respective circuit configurations[2],[3],[5],[7],[10]. Total Harmonic Distortion (THD) percentage for both the proposed amplifiers is calculated using established rules [10]-[12], [17]. Proposed amplifier-1 (Fig.1) holds 1.17% THD for 10 significant harmonic terms whereas Proposed amplifier-2 (Fig.2) shows only 1.13% THD for 10 significant harmonic terms [15].

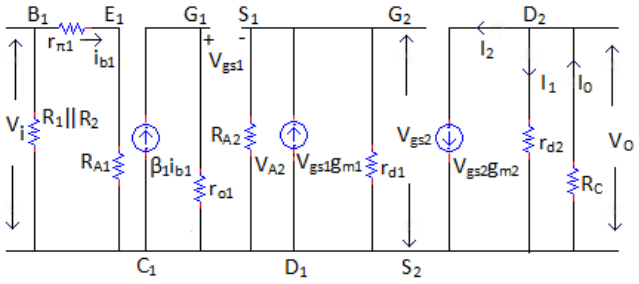

Fig. 4: Small-Signal AC Equivalent of Proposed Amplifier-1

Small-signal AC equivalent circuit of the Proposed amplifier-1 is depicted in Fig.4. AC voltage gain of this circuit (Fig.1) is approximated as following -

$$A_V = \frac{-g_{m1}\, g_{m2}\, \beta_1 r_{o1}}{\left(\frac{1}{R_c}+\frac{1}{r_{d2}}\right)\left(g_{m1}+\frac{1}{R_{A2}}+\frac{1}{r_{d1}}\right)(r_{\pi 1}+R_{A1})}$$

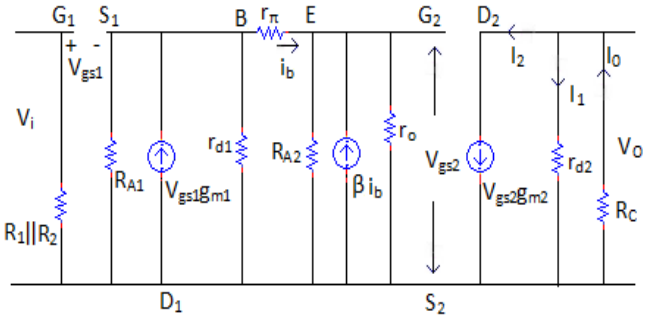

Fig. 5: Small-Signal AC Equivalent of Proposed Amplifier-2

Moreover, attempts are made to extend the small-signal AC equivalent circuit of Proposed amplifier-1 for the Proposed amplifier-2. The upshot is depicted in Fig.5. The approximated expression of the AC voltage gain for this amplifier comes out as following-

$$A_V = \frac{-g_{m2}}{\left(\frac{1}{R_c}+\frac{1}{r_{d2}}\right)\left[1+B.\{1+r_\pi.C\}+C.\left(r_\pi+\frac{1}{g_{m1}}\right)\right]}$$

Where

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$$B = \frac{1}{g_{m1}}\left(\frac{1}{R_{A1}} + \frac{1}{r_{d1}}\right) \quad \text{and} \quad C = \frac{1}{(1+\beta)}\left(\frac{1}{R_{A2}} + \frac{1}{r_o}\right)$$

Both the expressions for small-signal AC voltage gain use r_π as base-emitter resistance, r_o is the collector-emitter resistance and r_d as drain-source resistance. Negative sign in the expressions show phase reversal in output voltage waveform [1].

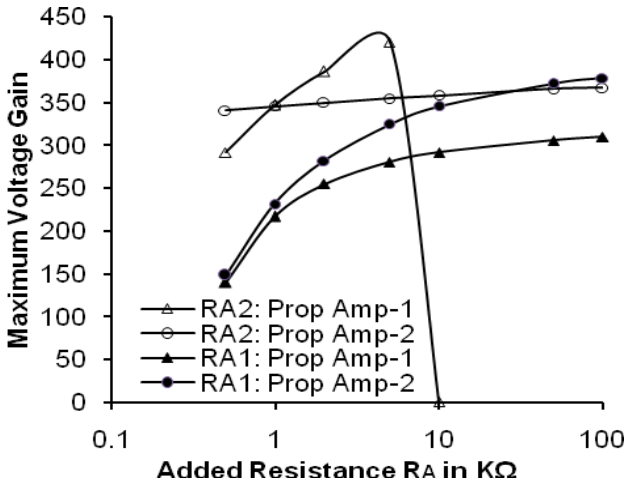

Fig. 6: Variation of Maximum Voltage Gain with RA

A_{VG} of both the proposed amplifiers significantly depends on additional biasing resistances R_{A1} and R_{A2}. Corresponding upshots are graphically depicted in Fig.6. For Proposed amplifier-1 (Fig.1), voltage gain found its maxim at R_{A2}=5KΩ, thereafter drops below unity at higher values of R_{A2}. However for increasing values of R_{A1} for Proposed amplifier-1, voltage gain initially increases but tends towards saturation beyond R_{A1}>50KΩ. Almost similar situation exists for Proposed amplifier-2 (Fig.2) for R_{A1} except it shows intense values of A_{VG} than Proposed amplifier-1 at every R_{A1}. However, situation is entirely different for R_{A2} with Proposed amplifier-2. Here, the A_{VG} is observed to hold almost saturation like track with increasing values of R_{A2}. This indicates that R_{A2} has more-or-less negligible effect on A_{VG} for Proposed amplifier-2.

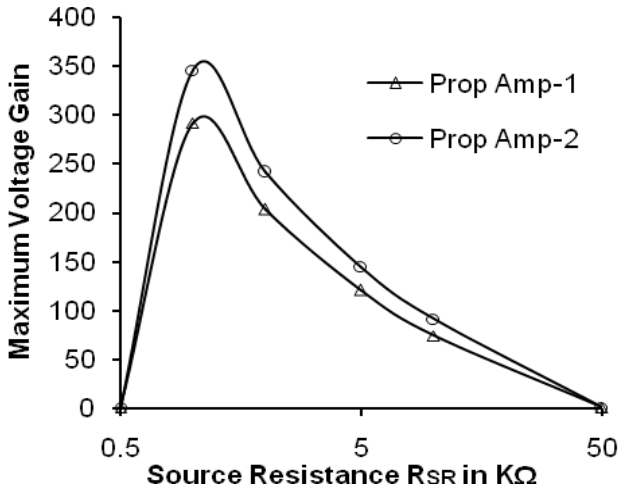

Fig.7: Variation of Maximum Voltage Gain with RSR

In addition, if additional biasing resistances R_{A1} and R_{A2} are simultaneously removed or R_{A2} is removed alone from the Proposed amplifier-1 (Fig.1), the corresponding circuit produces distorted output whereas if only R_{A1} is removed, the output signal shows clamping effect. However, if additional biasing resistance R_{A2} is removed from the Proposed amplifier-2 (Fig.2), A_{VG} falls below unity with in-phase output whereas if R_{A1} is removed, A_{VG} increases to 386.371(V_{OP}=391.906mV), current gain to 30.429K (I_{OP}=39.191μA), bandwidth reduces to 11.092KHz (f_L=125.717Hz and f_H=11.218KHz), AC input signal range reduces to 1-5mV and THD increases to 1.17%. If R_{A1} and R_{A2} are simultaneously removed from the Proposed amplifier-2 (Fig.2), respective circuit produces distorted output. This clearly indicates that the inclusion of R_{A1} and R_{A2} are essential to maintain the amplifying property of respective amplifiers. Variation of maximum voltage gain A_{VG} with Source resistance is shown in Fig.7. For proposed amplifier of Fig.1 and Fig.2, A_{VG} found its maximum at R_{SR}=1KΩ, thereafter, it decreases almost exponentially to reach below unity at 50KΩ. In fact, resistance R_{SR} in proposed amplifier circuits virtually behave as source resistance for the respective composite units. Therefore the source degeneration property of common source MOSFET in respective amplifiers forces voltage gain to fall almost exponentially with increasing values of R_{SR}.

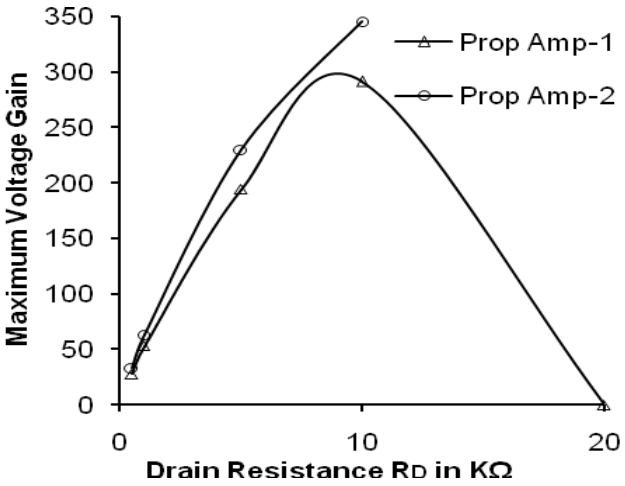

Fig. 8: Variation of Maximum Voltage Gain with RD

Variation of maximum voltage gain A_{VG} with drain resistance is shown in Fig.8. For both the proposed amplifier (Fig.1 and Fig.2) A_{VG} rises with rising values of R_C and finds its maxim at 10KΩ and falls below unity at 20KΩ for Proposed amplifier-1 whereas Proposed amplifier-2 produces distorted output beyond 10KΩ of R_C. Variation of maximum voltage gain A_{VG} with DC supply voltage V_{CC} is depicted in Fig.9. Voltage gain of both the proposed amplifiers increases non-linearly from 10V to 18V of V_{CC}, thereafter, drops to a lowest point at V_{CC}=20V [15]. The permissible range for reproduction of the amplified output at different V_{CC} for both the proposed amplifiers is 10-18V. This is perhaps due to the presence of CS MOSFET in Triple Darlington units of the proposed amplifiers at output position which bears a threshold voltage of 2.831V. The driving voltage at gate of the output CS MOSFET (node 7) increases with V_{CC}. This simply means that the MOSFET conducts well for 10-18 volts of V_{CC}. As V_{CC} increases beyond 18V, the MOSFET receives a better flow of electrons from source to drain.

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V_{CC} exerts a heavy attractive force on electrons entering the drain from the channel region [14]. So beyond V_{CC} >18V, the drain absorbs more electrons than the channel could supply. As a result, the channel completely pinches-off and thus subsequent increase in V_{CC}>18V has minor effect on output voltage [14]. This caused the voltage gain to be rolled-off.

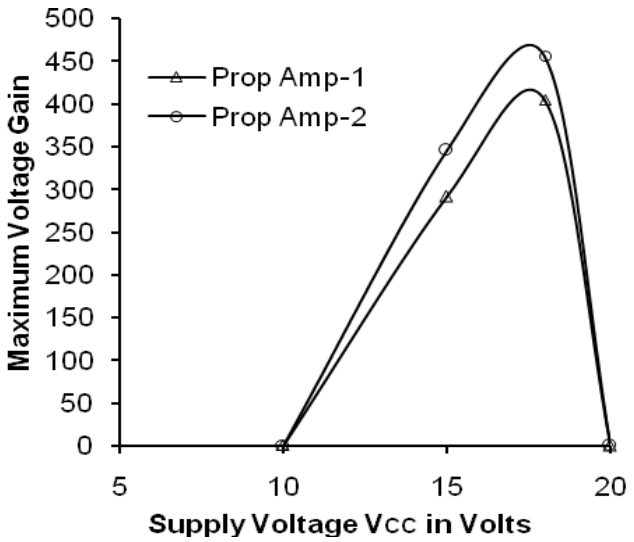

Fig. 9: Variation of Maximum Voltage Gain with VCC

Variation of maximum voltage gain with load resistance R_L is also studied for both the amplifiers under discussion (but not shown in form of graphs). It is observed that the voltage gain gradually rises up to 100KΩ value of R_L for amplifiers and then tends toward a saturation tendency at higher R_L. This rising and saturation of the voltage gain with R_L is found well in accordance of the usual behaviour of small signal amplifiers [2],[4],[5],[7],[12]. During the course of qualitative analysis, authors attempted to study the performance of proposed amplifiers (Fig.1 and Fig.2) by imposing some changes in the circuit configuration. Respective observations are listed below-

1. It is observed that when collector of the BJT of Proposed amplifier-1 (Fig.1) is detached from V_{CC} (node-4) and connected to node-5, the voltage gain falls to 263.773, bandwidth to 8.331 KHz and current gain to 553.905. However when drain of JFET is detached from node-4 and connected to node-5, the voltage gain falls below unity. Instead, if collector of BJT and drain of JFET are simultaneously detached from node-4 and connected to node-5, the voltage gain falls below unity. However when drain of the JFET or collector of BJT of Proposed amplifier-2 (Fig.2) is detached separately from V_{CC} (node-4) and connected to node-5, the voltage gain falls below unity. On the other hand if JFET and BJT of Proposed amplifier-2 (Fig.2) are simultaneously detached from V_{CC} and connected to node-5, the amplifier provides poor response.
2. Similarly, when biasing resistance R_1 is removed from the proposed amplifiers (Fig.1 and Fig.2), circuit doesn't perform well.

Variation of voltage gain, current gain and bandwidth with temperature is also measured and listed in Table-I. Table indicates that voltage gain, current gain and bandwidth of Proposed amplifier-1 (Fig.1) gradually decrease at rising temperature. However for Proposed amplifier-2 (Fig.2), both the gain gradually increases but at 80°C it starts decreasing whereas bandwidth decreases throughout the rising temperature.

Temp (°C)	Proposed Amplifier-1 (Fig.1)			Proposed Amplifier-2 (Fig.2)		
	A_{VG}	A_{IG}	B_W (KHz)	A_{VG}	A_{IG}	B_W (KHz)
-30	298.44	732.89	9.009	338.10	26.62K	14.678
-20	297.92	732.47	8.873	340.37	26.80K	14.416
-10	297.03	731.07	8.739	342.14	26.94K	14.147
0	295.84	728.85	8.616	343.49	27.05K	13.892
10	294.39	725.96	8.493	344.51	27.13K	13.618
27	291.49	719.78	8.286	345.56	27.21K	13.089
50	286.87	709.47	8.019	345.96	27.24K	12.388
80	280.01	693.66	7.687	345.21	27.18K	11.283

TABLE I: VARIATION OF A_{VG}, A_{IG} AND B_W WITH TEMPERATURE

Input and output noises for the proposed amplifier at 100Hz, 1KHz and 1MHz frequencies are observed and listed in TABLE II. Usually, resistors and semiconductor devices in electronic circuits are responsible to generate noises during amplification process. Table clearly indicates that levels of input and output noises are significantly low for proposed amplifier and within the permissible limit. Both varieties of noises reduce with elevation of operating frequency. Moreover, it also increases with temperature which is an obvious feature due to generation of more carriers and their higher collision rate at elevated temperature.

Temp (°C)	Total Output Noise(Volts/√Hz)		Total Input Noise (Volts/√Hz)	
	Fig.1 Amp. 1KHz ($x10^{-7}$)	Fig.2 Amp. 1KHz ($x10^{-7}$)	Fig.1 Amp. 1KHz ($x10^{-9}$)	Fig.2 Amp. 1KHz ($x10^{-9}$)
-30	8.211	9.892	2.751	2.929
-20	8.391	1.019	2.817	2.998
-10	8.561	1.049	2.882	3.067
0	8.722	1.077	2.948	3.138
10	8.875	1.104	3.015	3.208
27	9.119	1.150	3.128	3.330
50	9.423	1.209	3.285	3.497
80	9.781	1.285	3.493	3.722

TABLE II: VARIATION OF INPUT AND OUTPUT NOISE WITH TEMPERATURE

IV. CONCLUSIONS

As a novel approach, three dissimilar active devices namely MOSFET, JFET and BJT are used in Triple Darlington configuration to explore two small-signal amplifiers using RC coupling. These amplifiers can effectively process small-signals ranging below 10mV at 1KHz in the frequency band of 108.369Hz to 8.286 KHz and 155.77Hz to 13.245 KHz respectively. The proposed small-signal audio amplifiers (Fig.1 and 2) with Triple Darlington topology are free from the problem of poor response of conventional small-signal Darlington pair or Triple Darlington amplifiers at higher frequencies. With a narrow range bandwidth, proposed amplifiers generates only 1.17% and 1.13% harmonic distortions respectively and simultaneously produce high voltage and current gains. Status of voltage and current gains logically set power gain of these amplifiers greater than unity.

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These features make respective amplifiers fabulously unique in the class of RC coupled small-signal Darlington's amplifiers. The proposed amplifiers show considerable response in 0.5KΩ - 5KΩ range of additional biasing resistances R_{A1} and R_{A2} . Its optimum performance is received for 10-18V DC supply voltage and voltage gain is observed maximum for 1KΩ value of source resistance R_{SR}.

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