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Analysis of Advanced PWM Algorithms Based on Simplified Sequence for Reduced CMV in Induction Motor Drive

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Abstract*— This paper presents a simplified advanced Pulse width Modulation algorithms for reduced common mode voltage variations. These algorithms have been developed by using the concept of imaginary switching times and hence did not use angle and sector information. Thus, the proposed algorithms reduce the complexity involved in the existing PWM algorithms. In the conventional SVPWM method, two adjacent states with two zero voltage vectors are utilized to program the output voltage. Every 60^0 degrees the active voltage vectors change, but the zero state locations are retained. In the AZSPWM methods, the choice and the sequence of active voltage vectors are the same as in conventional SVPWM. However, instead of the real zero voltage vectors (V_0 and V_7), two active opposite voltage vectors with equal duration are utilized. In the NSPWM algorithm, in each sector any one of the phases is clamped to either positive or negative DC bus for a total of 120^o over a fundamental cycle. Hence, it reduces the switching losses of the inverter and switching frequency of the inverter by 33.33%. Among the proposed algorithms, the NSPWM algorithm gives superior performance with reduced switching losses of the inverter.

***Index Terms*—Common mode voltage, induction motor drive, SVPWM, AZSPWM and NSPWM**

I. INTRODUCTION

Recently, the voltage source inverters are becoming popular to feed variable voltage, variable frequency voltages to the three-phase induction motor drives. A detailed survey on the various PWM algorithms for voltage source inverters is given in [1]. Among the various PWM algorithms, SVPWM algorithm offers many advantages and hence it is becoming popular [2]. The SVPWM algorithm divides the zero voltage vector time equally among the two zero voltage vectors. To reduce the harmonic distortion, the zero voltage space vectors are used in SVPWM algorithm, which results in large common-mode voltage (CMV) variations. The poor CMV characteristics lead to prohibitive amount of common-mode current (CMC) in induction motors. In induction motor drive applications, this may lead to motor bearing failures, electromagnetic interference (EMI) noise, or interference with other electronic equipment in the vicinity [3]-[5]. Such problems have increased recently due to increasing PWM frequencies and faster switching times. The passive [5]-[6] or active filters [7] can be utilized to suppress the effect of the CMV from the source. However, these methods involve additional hardware, and thus, they significantly increase the drive cost and complexity. An alternative approach is to modify the pulse pattern of the standard PWM algorithm such that the CMV is substantially reduced from its source and its effects are mitigated at no cost [8]-[12]. Hence, researchers concentrated on improving the original three phase inverter by modifying the PWM techniques used for inverter control. These PWM algorithms are known as reduced common mode voltage PWM (RCMVPWM) methods. These include the recently reported active zero state PWM (AZSPWM) algorithms, remote state PWM (RSPWM) algorithm and near state PWM (NSPWM) algorithm as the most successful representatives. Depending on the choice of the voltage vectors, various RCMVPWM algorithms exist. In the AZSPWM methods, the classical active (adjacent) voltage vector s are complemented with either two near opposing active vectors or one of the adjacent states and its opposite vector with equal time to effectively create a zero-voltage vector [8]-[9]. In the AZSPWM methods, the choice of active voltage vectors is the same as in standard SVPWM algorithm. However, instead of the real zero voltage vectors (V0 and V7), two active opposite voltage vectors with equal duration are utilized. The RSPWM methods synthesize the output voltage from three inverter voltage vectors that are 120^o apart from each other (most remote vectors) as explained in [10]. The NSPWM method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds as explained in [11]-[12]. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized. NSPWM employs only three neighbor voltage vectors and sequences them in the order that the minimum switching count is obtained. In this algorithm, one of the phases is not switched within each sampling time period. Hence, this algorithm reduces the switching losses of the inverters also when compared with the AZSPWM and RSPWM algorithms. But, the existing NSPWM algorithm uses the conventional space vector approach, which requires angle and sector information and hence, increases the complexity.

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To reduce the complexity in the conventional space vector approach, an offset time based approach for SVPWM and various bus-clamping PWM algorithms has been given in [13]. This paper presents simplified advanced PWM algorithms by using the concept of imaginary switching times for reduced switching frequency and for reduced CMV in VSI fed induction motor drives.

II. COMMON MODE VOLTAGE

The common mode voltage is the potential of the star point of the load with respect to the center of the dc bus of the VSI. Fig. 1 shows a VSI fed induction motor. A set of phase voltage equations can be written as given in (1).

$$V_{an} = V_{so} - V_{ao}$$
$$V_{bn} = V_{so} - V_{bo} \qquad (1)$$
$$V_{cn} = V_{so} - V_{co}$$

where V_{ao}, V_{bo}, V_{co} are inverter pole voltages and V_{so} is common mode voltage. The voltage across of each capacitor is $\frac{V_{dc}}{2}$ and '*0*' is the common point of two capacitors and capacitors are connected across the input side of an inverter.

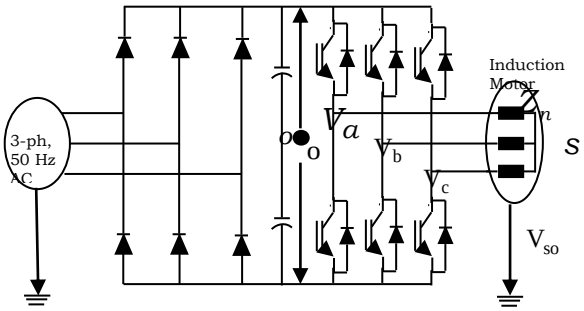

Fig.1 Three-phase VSI fed induction motor

Adding the set of equations and since $V_{an} + V_{bn} + V_{cn} = 0$, the common mode voltage in the motor is given by

$$V_{com} = V_{so} = \frac{V_{ao} + V_{bo} + V_{co}}{3} \qquad (2)$$

Hence, if the drive is fed by balanced three phase supply, the common mode voltage is zero. But, the common mode voltage exists inevitably when the drive is fed from an inverter employing PWM technique because the VSI cannot produce pure sinusoidal voltages and has discrete output voltages. It can be shown that the switching state and dc bus voltage decides the common mode voltage. There are eight available output voltage vectors in accordance with the eight different switching states of the inverter as depicted in Fig.2 According to the switching states of the inverter the common mode voltage can be expressed as given in (3).

$$V_{com} = V_{so} = \frac{V_{dc}}{3}(S_a + S_b + S_c) - \frac{V_{dc}}{2} \qquad (3)$$

where S_a, S_b and S_c denotes the switching states of each phase.

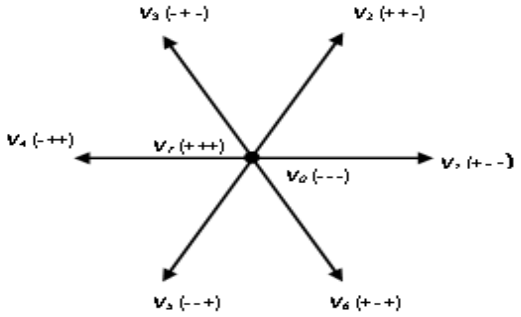

Fig. 2 Voltage space vectors of a three-phase VSI

The common mode voltage for each inverter shows that, if only even or only odd voltage vectors are used, no common mode voltage variation is generated. If a transition occurs from an even voltage vector to an odd one (or vice versa), a common mode variation of amplitude $V_{dc}/3$ is generated. If a transition from an odd (even) voltage vector to the zero (seventh) voltage vector occurs, a common variation $V_{dc}/3$ is generated. If a transition from an odd (even) voltage vector to the seventh (zero) voltage occurs, a common-mode variation of amplitude $2V_{dc}/3$ is generated. Finally, if a transition occurs from zero to seventh or vice versa, a common mode variation of amplitude V_{dc} is generated.

III. ADVANCED PWM ALGORITHMS

In the application field the problems related to common mode voltage are increasing due to increased PWM switching frequencies aimed at higher efficiency, increased bandwidth, etc. Hence, common mode voltage reduction techniques have been gaining importance. The effect of common mode voltage can be reduced actively or passively. The active common mode voltage reduction method that involves controlling the PWM pulse patterns is the most economical method as it requires no extra components. Recently, several PWM pulse patterns that yield reduced common mode voltage termed as reduced common mode voltage PWM (RCMVPWM) methods have been reported [8-9]. In all these methods, the zero states of the inverter are avoided and results in a common mode voltage of $\pm V_{dc}/6$. All these methods are described using space vector approach. Based on the choice of the voltage vectors, the RCMVPWM methods will be sub grouped in three types, these include active zero state PWM (AZSPWM) algorithms, remote state PWM (RSPWM) algorithms and near state PWM (NSPWM) algorithm [10-12]. In the AZSPWM algorithms, the conventional active (adjacent) voltage vectors are complemented with either two near opposing active vectors or one of the adjacent states and its opposite vector with equal time to effectively create a zero-voltage vector. The RSPWM methods synthesize the output voltage from three inverter voltage vectors that are 120° apart from each other (most remote vectors). The NSPWM method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized. But, this thesis mainly deals with only AZSPWM and NSPWM algorithms.

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In the AZSPWM algorithms, the vector transformation yields six active and two zero vectors for the inverter, and as shown in Fig. 3, the vectors divide the space into six segments as in SVPWM algorithm. These regions are utilized in programming the PWM pulses. But, in the NSPWM algorithm 30º phase-shifted regions are utilized as shown in Fig. 4. In the space vector approach, the duty cycles of the voltage vectors are calculated according to the volt-seconds balance rule. The voltage vectors and their sequences are selected based on a specified performance criterion such as the minimum output voltage ripple and switching count and the vectors are programmed accordingly. The formation of AZPWM and NSPWM algorithms is illustrated in Fig.3 – Fig.4.

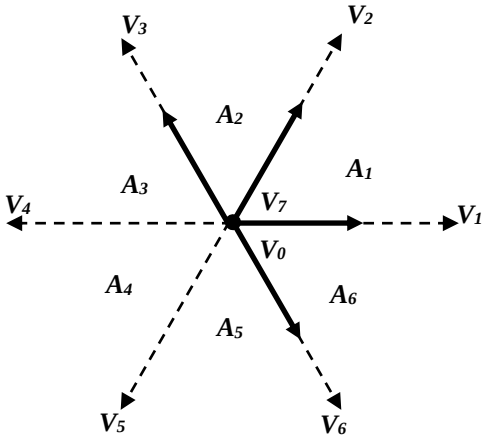

Fig. 3 Voltage space vectors and formation of AZSPWM algorithms

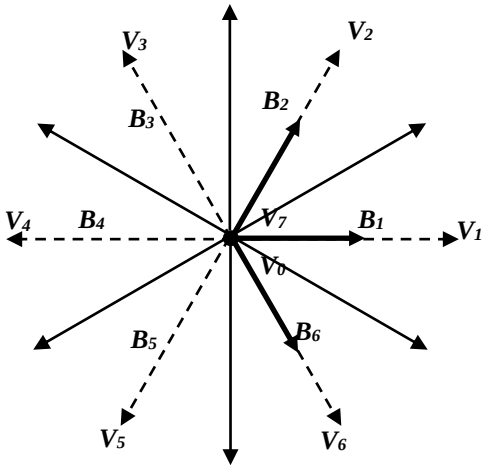

Fig. 4 Voltage space vectors and formation of NSPWM algorithm

In the conventional SVPWM method, two adjacent states with two zero voltage vectors are utilized to program the output voltage. Every 60^0 degrees the active voltage vectors change, but the zero state locations are retained. In the AZSPWM methods, the choice and the sequence of active voltage vectors are the same as in conventional SVPWM. However, instead of the real zero voltage vectors (V_0 and V_7), two active opposite voltage vectors with equal duration are utilized. Here, three choices exist. For AZSPWM algorithms, any of the pairs V_1-V_4, V_2-V_5, or V_3-V_6 can be utilized. The NSPWM employs only three neighbor voltage vectors and sequences them in the order that the minimum switching count is obtained. Thus, one of the phases is not switched within each PWM cycle. For example, for the region between -30º and +30º (sector B_1), the applied voltage vectors are V_1, V_2, and V_6 with the sequence V_6-V_2-V_1-V_1-V_2-V_6. In the NSPWM algorithm, in each sector any one of the phases is clamped to either positive or negative DC bus for a total of 120º over a fundamental cycle. Hence, it reduces the switching losses of the inverter and switching frequency of the inverter by 33.33%.

IV. ADVANCED PWM ALGORITHMS USING SIMPLIFIED SEQUENCE

Calculation of Switching Times - AZSPWM Algorithms:

To reduce the complexity involved in the existing AZSPWM algorithms, in this chapter, the proposed AZSPWM have been developed by using the notion of imaginary switching times. In this approach, the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages are calculated as given in (4)

$$T_{an} \equiv \left(\frac{T_s}{V_{dc}}\right) V_{an}\ ; \quad T_{bn} \equiv \left(\frac{T_s}{V_{dc}}\right) V_{bn}\ ; \quad T_{cn} \equiv \left(\frac{T_s}{V_{dc}}\right) V_{cn} \qquad (4)$$

To calculate the active vector switching times, the maximum, middle and minimum values of imaginary switching times are calculated in every sampling time as given in (5) – (9).

$$T_{max} = Max(T_{an}, T_{bn}, T_{cn}) \qquad (5)$$

$$T_{mid} = Mid(T_{an}, T_{bn}, T_{cn}) \qquad (6)$$

$$T_{min} = Min(T_{an}, T_{bn}, T_{cn}) \qquad (7)$$

Then the active vector switching times T_1 and T_2 may be expressed as

$$T_1 = T_{max} - T_{mid}\ ; T_2 = T_{mid} - T_{min} \qquad (8)$$

The zero voltage vectors switching time is calculated as

$$T_z = T_s - T_1 - T_2 \qquad (9)$$

Then, the zero voltage vector time is shared equally among the two opposite active voltage vectors to create effectively a zero voltage vector. Then, by utilizing the space vector approach, the possible switching sequences, can be derived.

Calculation of Switching Times - NSPWM Algorithms:

As the existing NSPWM algorithm uses conventional space vector approach, the complexity involved in the algorithm is more. To simplify the algorithm, proposed NSPWM algorithm is developed by using the notion of imaginary switching times. The modulating waveform of NSPWM algorithm is similar to the discontinuous PWM 1 (DPWM1) algorithm as explained in [11]. The modulating waveform can be generated by using the concept of imaginary switching times as given below:

The imaginary switching time periods, which are proportional to the instantaneous values of the reference phase voltages, are calculated. Then the maximum and minimum values can be calculated by using (8) and (9). Then, the effective time during which the induction motor is effectively connected to the source (that is the power will be transferred to the motor from source) can be calculated as given in (10).

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$$T_{eff} = T_{max} - T_{min} \quad (10)$$

When the actual gating signals for power devices are generated in the PWM algorithm, there is one degree of freedom by which the effective time can be relocated anywhere within the sampling time period. Therefore, the actual switching times for each inverter leg can be obtained by the time shifting operation as follows:

$$T_{ga} = T_{an} + T_{offset} \quad (11)$$

$$T_{gb} = T_{bn} + T_{offset} \quad (12)$$

$$T_{gc} = T_{cn} + T_{offset} \quad (13)$$

To guarantee the full utilization of dc-link voltage of the inverter, the actual switching times should be restricted to a value from 0 to T_s. To generate the modulating waveforms of NSPWM algorithm, the procedure is as follows:

If the A –phase reference voltage is positive (or negative) and has maximum magnitude, the A-phase switch should be fixed to the ON (or OFF) state. That is to say ,

$$\text{if } T_{max} + T_{min,} < 0 \Rightarrow T_{max} + T_{offset} = T_s$$
$$\text{if } T_{max} + T_{min} \geq 0 \Rightarrow T_{min} + T_{offset} = 0 \quad (14)$$

Therefore, the time shifting value T_{offset} is

$$\text{if } T_{max} + T_{min,} < 0 \Rightarrow T_{offset} = T_s - T_{max}$$
$$\text{if } T_{max} + T_{min} \geq 0 \Rightarrow T_{offset} = -T_{min} \quad (15)$$

Then, the modulating waveforms of NSPWM algorithm can be synthesized using the calculated gating times by using (16) .

$$V_{in}^{*} = \frac{V_{dc}}{2}\left(\frac{2*T_{gi}}{T_s} - 1\right) \qquad i = a, b, c \quad (16)$$

The total number of commutations in SVPWM algorithm is three in a sampling time interval, where as the number of commutations in NSPWM algorithm is two. Moreover, from the modulating waveform of NSPWM algorithm, it can be observed that any one of the phases is clamped to the either positive or negative DC bus for utmost a total of 120^0 over a fundamental cycle. Hence, the switching losses of the associated inverter leg are eliminated. Hence, the switching frequency of the NSPWM algorithms is reduced by 33% compared with SVPWM algorithm. This implies that if one wants to keep the average switching frequency constant, whenever NSPWM algorithm is used, sampling frequency must be increased by $\left(\frac{3}{2}\right)$ times. However, in NSPWM algorithm instead of one carrier wave, two carrier waves (V_{tri} and $-V_{tri}$) must be utilized. The choice of the triangle to be compared with the modulation signals is region dependent. If slope of the reference phase voltage is positive then the modulating waveform is compared with V_{tri} and if slope of the reference phase voltage is negative then the modulating waveform is compared with $-V_{tri}$. General switching rule is that if the modulating waveform is larger than the carrier signal (triangular wave), the upper switch associated with the specific phase is set “on”.

V. SIMULATION RESULTS AND DISCUSSION

To validate the proposed advanced PWM algorithms, numerical simulation studies have been carried out on v/f controlled induction motor drive by using Matlab/Simulink. For the simulation studies, the switching frequency of the inverter is taken as 5 kHz and dc link voltage is taken as 540V. Any well-designed PWM strategy must ensure that the line-line voltages do not have negative pulses in the positive half-cycle and vice versa for reduced harmonic distortion. That is, a line-line voltage must be either $+V_{dc}$ or 0 and must not be $-V_{dc}$ at any instant during its positive half cycle. Similarly, it must be either $-V_{dc}$ or 0 and must not be $+V_{dc}$ at any instant during its negative half cycle. The line voltages of v/f controlled induction motor drive are shown from which it can be observed that the proposed algorithms have pulses of opposite polarity and hence give more harmonic distortion when compared with the SVPWM algorithm.

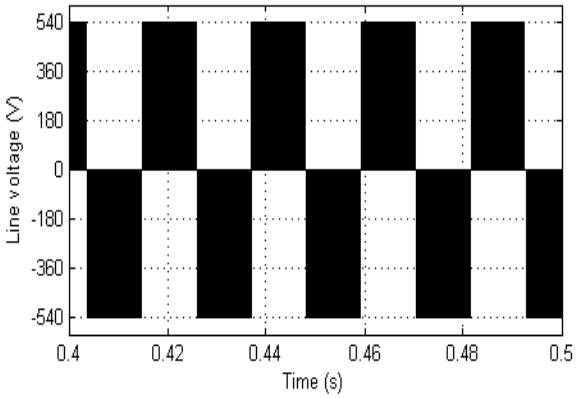

Fig 5 Line voltage for SVPWM algorithm

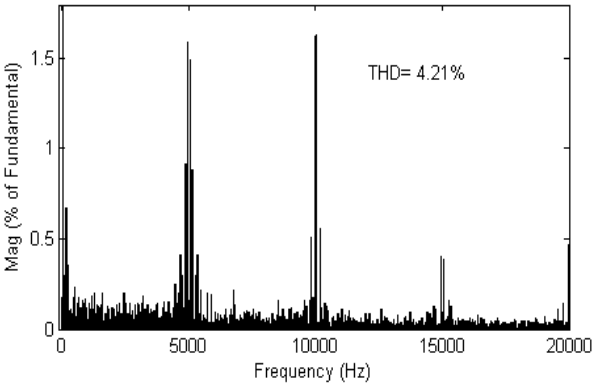

Fig 6 harmonic spectrum of line current of SVPWM based v/f controlled induction motor drive

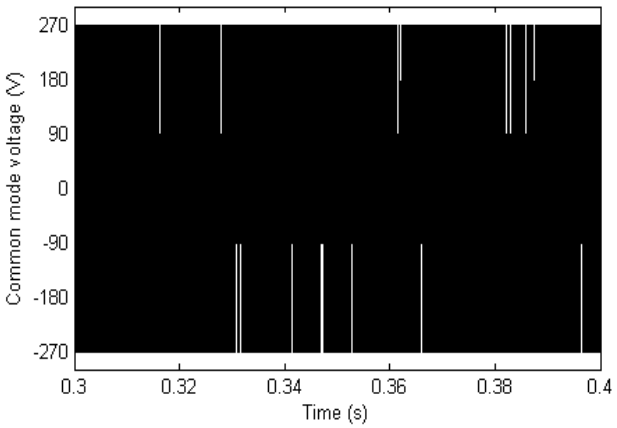

Fig 7 Common mode voltage variations of SVPWM based v/f controlled induction motor drive

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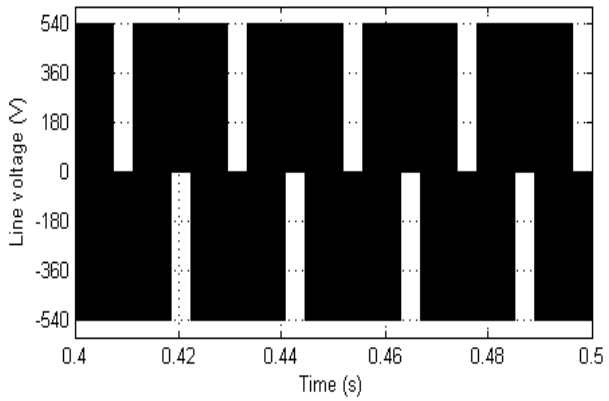

Fig 8 Line voltage for proposed AZSPWM algorithm

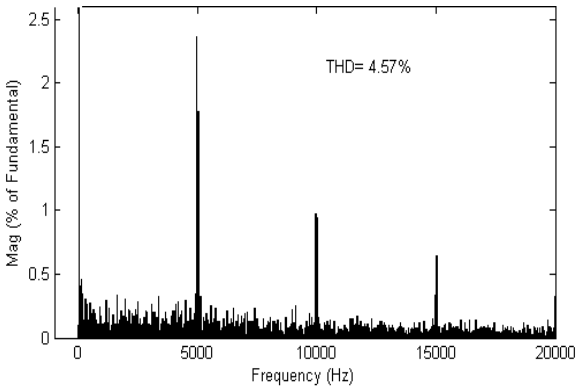

Fig 9 Harmonic spectra of line current of AZSPWM algorithm based v/f controlled induction motor drive

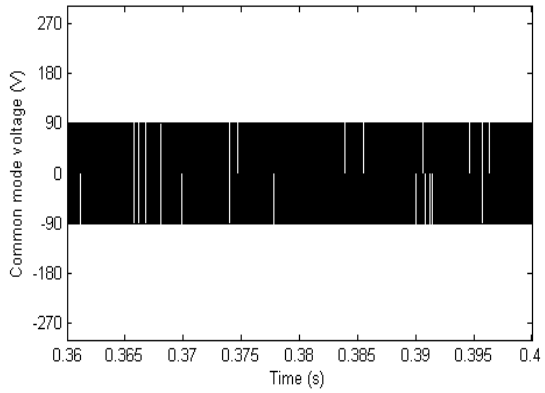

Fig 10 Harmonic spectra of line current of AZSPWM algorithm based v/f controlled induction motor drive

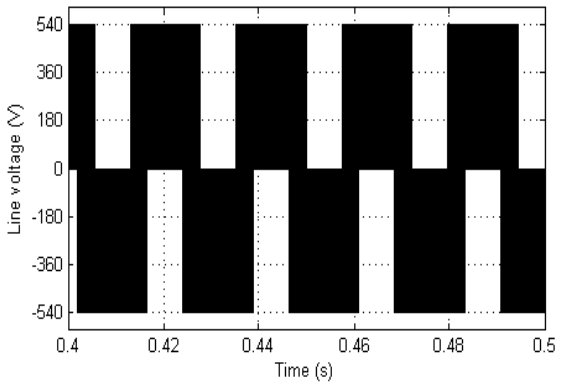

Fig 11 Line voltage for proposed NSPWM algorithm

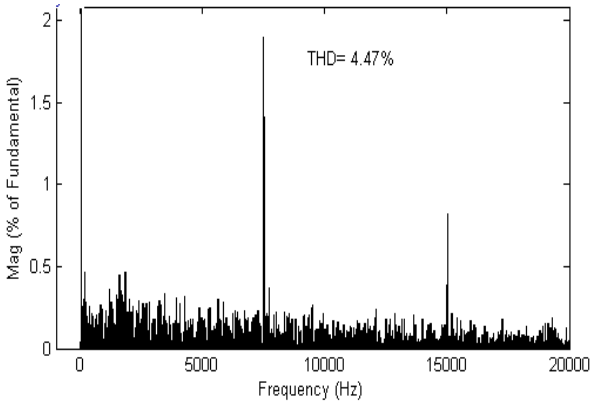

Fig 12 Harmonic spectra of line current of NSPWM algorithm based v/f controlled induction motor drive

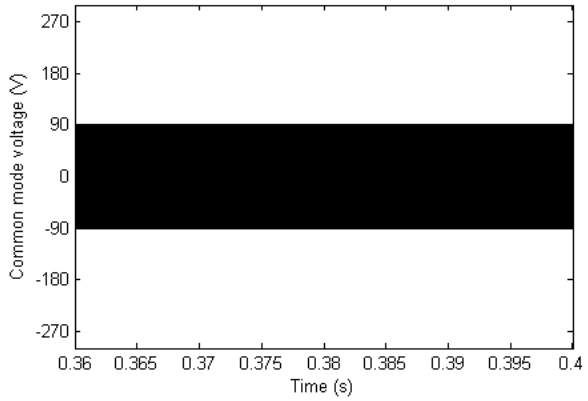

Fig 13 common mode voltage variations in NSPWM algorithm based v/f controlled induction motor drive

VI. CONCLUSION

In this paper, a simplified AZSPWM and NSPWM algorithms have been proposed to reduce the common mode voltage variations. Though the SVPWM algorithm gives less harmonic distortion and fixed frequency operation, it gives more common mode voltage variations. From the simulation results, it can be observed that the proposed algorithm gives reduced common mode voltage variations when compared with the SVPWM algorithm. But, the harmonic distortion is slightly high when compared with the SVPWM algorithm. Among the proposed algorithms, the NSPWM algorithm gives superior performance with reduced switching losses of the inverter.

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