

Performance Analysis of Twenty Seven Level Asymmetrical Cascaded H-Bridge Multi Level Inverter Fed Three Phase Induction Motor Drive

P. Roseline, B. Ramesh, Ch. V. V. Manga Lakshmi

Abstract—Multilevel inverters are suitable of high power handling capacity, associated with lower output harmonics and lower commutation losses. But the main disadvantages of multi level inverters are complexity, requiring a more number of power devices and passive components, and complex control circuitry. Hence a Twenty Seven Level Cascaded H-Bridge multi level inverter (CHBMLI) topology is proposed which requires only twelve switches and those switches are controlled by using of New PWM technique i.e., POD (Phase Opposition Disposition) modulation method whereas Twenty switches are required in the cascaded H- bridge multi level inverter (CHBMLI) for Eleven Level by using of Repeating sequence method. The proposed cascaded H- bridge multi level inverter topology offers strong advantages such as improved output waveforms, smaller filter size, and lower electromagnetic interference. Here an asymmetrical configuration of Twenty Seven-level inverter (TSLI) based Cascaded H-Bridge Multi Level topology fed Three Phase Induction Motor Drive performance is analyzed and compared with CHBMLI with Repeating sequence as switching technique. The performance factors are obtained at both transient and steady state operating conditions with usage of minimum number of switches so that switching losses can be reduced effectively with cascaded H- bridge multi level approach.

Index Terms—Cascaded H-Bridge Multi Level Inverter, Phase opposition disposition, Twenty seven level inverter, Total harmonic distortion.

I. INTRODUCTION

Since past decade, multilevel inverters have drawn increasing attention because of their promising applications in power systems and industrial drives. They can be efficiently used in the distributed energy systems in which, output ac voltage is obtained by connecting dc sources such as batteries, fuel cells, solar cells, rectified wind turbines etc at input side of the inverters mentioned in [1]. The ac output voltage obtained from the inverters can be fed to a load directly or interconnect to the ac grid without voltage balancing problems. The multilevel inverters offer several advantages as compared to the hard-switched two-level pulse width modulation inverters, such as their capabilities to operate at high voltage with lower dv/dt per switching, high efficiency, low electromagnetic interference etc.

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High magnitude sinusoidal voltage with extremely low distortion at fundamental frequency can be produced at output with the help of multilevel inverters by connecting sufficient number of dc levels at input side. There are mainly three types of multilevel inverters; these are a) diode-clamped, b) flying capacitor and c) cascade multilevel inverter (CHBMLI). Among these three, CHBMLI has a modular structure and requires least number of components as compared to other two topologies, and as a result, it is widely used for many applications in electrical engineering mentioned in [5]. To produce multilevel output ac voltage using different levels of dc inputs, the semiconductor devices must be switched ON and OFF in such a way that the fundamental voltage is obtained as desired along with the elimination of certain number of higher order harmonics in order to have least harmonic distortion in the ac output voltage. For switching the semiconductor devices, proper selection of switching angles is must. The switching angles at fundamental frequency, in general, are obtained from the solution of non linear transcendental equations characterizing harmonics contents in the output ac voltage; these equations are known as selective harmonic elimination (SHE) equations mentioned in [10]. A single-phase multi string five-level inverter integrated with an auxiliary circuit was recently proposed for dc/ac power conversion described in [12]. This topology used in the power stage offers an important improvement in terms of lower component count and reduced output harmonics. Unfortunately, high switching losses in the additional auxiliary circuit caused the efficiency of the multi string five-level inverter to be approximately 4% less than that of the conventional multi string three-level inverter in [13]. A novel isolated single-phase inverter with generalized zero vectors (GZV) modulation scheme was first presented to simplify the configuration. However, this circuit can still only operate in a limited voltage range for practical applications and suffer degradation in the overall efficiency as the duty cycle of the dc-side switch of the front-end conventional boost converter approaches unity in [14]. Furthermore, the use of isolated transformer with multi windings of the GZV based inverter results in the larger size, weight, and additional expense. The newly constructed inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and total harmonics distortion (THD). The performance of three phase induction motor is observed with the three phase Multi string multi level inverter up to Nine level developed in [15]. In this paper, an asymmetrical configuration of eleven-level inverter (ELI) based Multi String Multi Level topology fed Three Phase Induction Motor Drive performance is analyzed

and compared with conventional cascaded H- bridge multi level inverter and the performance factors are obtained at both transient and steady state operating conditions with usage of minimum number of switches so that switching losses can be reduced effectively with multi string multi level approach. Performance Analysis of Eleven Level Asymmetrical Multi String Multi Level Inverter fed Three Phase Induction Motor Drive [16].

II. MULTI LEVEL INVERTER TOPOLOGIES

1. Basic Five level Cascaded H-Bridge Multi level inverter(CHBMLI):

The Basic circuit of five level Cascaded H-bridge multi level inverter (CHBMLI) with eight switches as shown in Fig.1 and corresponding output voltage waveforms are shown in Fig.1. In this approach, all the eight switches are operated with a switching frequency of 50 Hz and the input voltage of Vdc=100V. The symmetrical multilevel approach of the Cascaded H-bridge inverter is operated with equal voltage values at the input side of the inverter. In a symmetrical Cascaded H-bridge multi level inverter, the Seven, Nine, Eleven and Thirteen levels are generated by using 12,16,20,24 switches respectively with repeating sequence as gating signal. The corresponding Switching states and terminal output voltages of five-level Cascaded H-bridge Multi level inverter is shown in Table .1

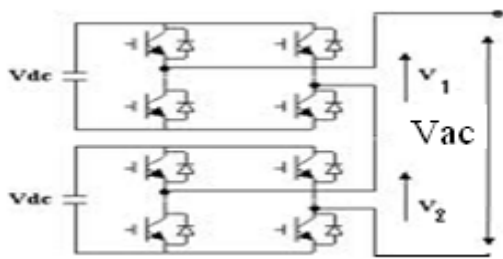


Fig. 1: Five Level Cascaded H-Bridge Inverter

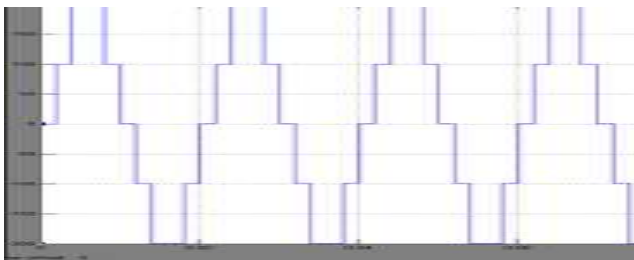


Fig. 2: Output Voltages of Five Level CHBMLI

Table. 1: Switching States and Terminal Voltage of Five-Level CHBMLI

Vo	Swiches in cascaded H-bridge Five level Multi level Inverter							
	S1	S2	S3	S4	S5	S6	S7	S8
+2Vs	1	1	0	0	1	1	0	0
+Vs	1	1	0	0	1	0	1	0
+Vs	1	0	1	0	1	1	0	0
0	1	0	1	0	1	0	1	0
-Vs	0	0	1	1	1	0	1	0
-Vs	1	0	1	0	0	0	1	1
-2Vs	0	0	1	1	0	0	1	1

2 Eleven Level Cascaded H-Bridge Multi level inverter(CHBMLI):

The Eleven Level Cascaded Multi level inverter circuit is shown in Fig.3 in a symmetrical approach with an input voltage of 100 V and corresponding output voltage waveforms are shown in Fig.6. It requires 20 switches to get eleven level of output voltage. The Table.2 shows the operation of switches at different levels of voltages.

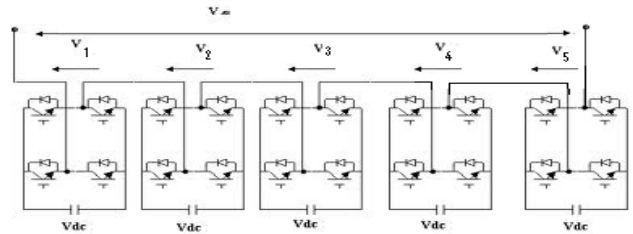


Fig. 3: Eleven Level Cascaded H-Bridge MLI

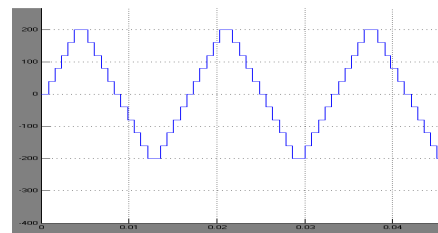


Fig. 4. Output Voltages of Eleven Level CHBMLI

Table 2: Switching States and Terminal Voltage of Eleven Level Cascaded H-Bridge Multi Level Inverter

V o	Swiches in Cascaded H-Bridge Eleven level Multi level inverter																			
	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9	S 1	S 1	S 1	S 1	S 1	S 1	S 1	S 1	S 1	S 1	S 1
+ 5 V s	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
+ 4 V s	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1
+ 3 V s	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1
+ 2 V s	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1
+ V s	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
- V s	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
- 2 V s	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1
- 3 V s	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
- 4 V s	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
- 5 V s	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1

Table.2 consists of switching combinations that generate the required eleven level output signals. The corresponding

mode of operations of the cascaded H bridge multilevel inverter stages are described as follows.

- a) Maximum positive output voltage (+5Vs): Active switches S1,S2,S5,S6,S9,S10,S13,S14,S17 and S18 are kept in ON and inverter output voltage is 5Vs.
- b) positive output voltage (+4Vs): Active switches S1,S2,S5,S6,S9,S10,S13,S14,S18, and S20 are kept ON and inverter output voltage is 4Vs.
- c) positive output voltage (+3Vs): Active switches S1,S2,S5,S6,S9,S10,S14,S16,S18, and S20 are kept ON and inverter output voltage is 3Vs.
- d) positive output voltage (+2Vs): Active switches S1,S2,S5,S6,S10,S12,S14,S16,S18, and S20 are kept ON and inverter output voltage is 2Vs.
- e) positive output voltage (+Vs): Active switches S1,S2,S6,S8,S10,S12,S14,S16,S18, and S20 are kept ON and inverter output voltage is Vs.
- f) Zero Output, (0): Active switches S2,S4,S6,S8,S10,S12,S14,S16,S18 and S20 are kept ON and inverter output voltage is 0.
- g) negative output voltage (-Vs): Active switches S3,S4,S6,S8,S10,S12,S14,S16,S18, and S20 are kept ON and inverter output voltage is -Vs.
- h) negative output voltage (-2Vs): Active switches S3,S4,S7,S8,S10,S12,S14,S16,S18, and S20 are kept ON and inverter output voltage is -2Vs
- i) negative output voltage (-3Vs): Active switches S3,S4,S7,S8,S11,S12,S14,S16,S18, and S20 are kept ON and inverter output voltage is -3Vs.
- j) negative output voltage (-4Vs): Active switches S3,S4,S7,S8,S11,S12,S15,S16,S18, and S20 are kept ON and inverter output voltage is -4Vs.
- k) Maximum negative output voltage (-5Vs): Active switches S3,S4,S7,S8,S11,S12,S15,S16,S19, and S20 are kept ON and inverter output voltage is -5Vs.

III. PROPOSED TWENTY SEVEN LEVEL CASCADED H-BRIDGE MULTI LEVEL INVERTER (CHBMLI)

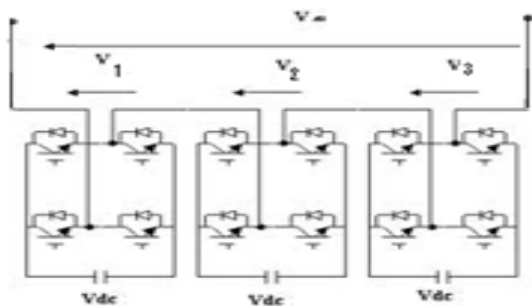


Fig. 5: Twenty Seven Level Cascaded H-Bridge MLI

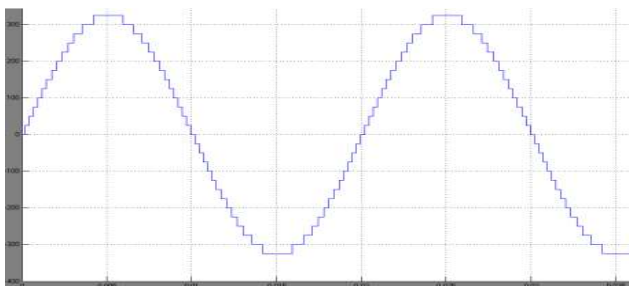


Fig. 6: Output Voltages of Twenty Seven Level CHBMLI

Table 3: Switching States and Terminal Voltage of Twenty Seven Level Cascaded H-Bridge Multi Level Inverter

Vo	Switches in Cascaded H-Bridge Twenty Seven level Multi level inverter											
	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9	S 10	S 11	S 12
+13 Vs	1	1	0	0	1	1	0	0	1	1	0	0
+12 Vs	1	0	1	0	1	1	0	0	1	1	0	0
+11 Vs	0	0	1	1	1	1	0	0	1	1	0	0
+10 Vs	1	1	0	0	1	0	1	0	1	1	0	0
+9 Vs	1	0	1	0	1	0	1	0	1	1	0	0
+8 Vs	0	0	1	1	1	0	1	0	1	1	0	0
+7 Vs	1	1	0	0	0	0	1	1	1	1	0	0
+6 Vs	1	0	1	0	0	0	1	1	1	1	0	0
+5 Vs	0	0	1	1	0	0	1	1	1	1	0	0
+4 Vs	1	1	0	0	1	1	0	0	1	0	1	0
+3 Vs	1	0	1	0	1	1	0	0	1	0	1	0
+2 Vs	0	0	1	1	1	1	0	0	1	0	1	0
+Vs	1	1	0	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0	1	0
-Vs	1	1	0	0	1	0	1	0	1	0	1	0
-2Vs	0	0	1	1	1	1	0	0	1	0	1	0
-3Vs	1	0	1	0	1	1	0	0	1	0	1	0
-4Vs	1	1	0	0	1	1	0	0	1	0	1	0
-5Vs	0	0	1	1	0	0	1	1	1	1	0	0
-6Vs	1	0	1	0	0	0	1	1	1	1	0	0
-7Vs	1	1	0	0	0	0	1	1	1	1	0	0
-8Vs	0	0	1	1	1	0	1	0	1	1	0	0
-9Vs	1	0	1	0	1	0	1	0	1	1	0	0
-10 Vs	1	1	0	0	1	0	1	0	1	1	0	0
-11 Vs	0	0	1	1	1	1	0	0	1	1	0	0
-12 Vs	1	0	1	0	1	1	0	0	1	1	0	0
-13 Vs	1	1	0	0	1	1	0	0	1	1	0	0

Table.3 consists of switching combinations that generate the required Twenty Seven level output signals.

The corresponding mode of operations of the cascaded H bridge multilevel inverter stages are described as follows.

- a) Maximum output voltage (+13Vs & -13Vs): Active switches S1,S2,S5,S6,S9 and S10 kept in ON and inverter output voltage is 13Vs.
- b) output voltage (+12Vs and -12Vs): Active switches S1,S3,S5,S6,S9 and S10 are kept ON and inverter output voltage is 12Vs.
- c) output voltage (+11Vs and -11Vs): Active switches S3,S4,S5,S6,S9 and S10 are kept ON and inverter output voltage is 11 Vs.
- d) output voltage (+10Vs and -10Vs): Active switches S1,S2,S5,S7,S9 and S10 are kept ON and inverter output voltage is 10Vs.
- e) output voltage (+9Vs and -9Vs): Active switches S1,S3,S5,S7,S9 and S10 are kept ON and inverter output voltage is 9Vs.
- f) output voltage (+8Vs and -8Vs): Active switches S3,S4,S5,S7,S9 and S10 are kept ON and inverter output voltage is 8.
- g) output voltage (+7Vs and -7Vs): Active switches S1,S2,S7,S8,S9 and S10 are kept ON and inverter output voltage is 7Vs.
- h) output voltage (+6Vs and -6Vs): Active switches S1,S3,S6,S7,S8,S9 and S10 are kept ON and inverter output voltage is 6Vs
- i) output voltage (+5Vs and -5Vs): Active switches S3,S4,S7,S8,S9 and S10 are kept ON and inverter output voltage is 5Vs.
- j) output voltage (+4Vs and -4Vs): Active switches S1,S2,S5,S6,S9 and S11 are kept ON and inverter output voltage is 4Vs.
- k) output voltage (+3Vs and -3Vs): Active switches S1,S3,S5,S6,S9 and S11 are kept ON and inverter output voltage is -5Vs.
- l) output voltage (+2Vs and -2Vs): Active switches S3,S4,S5,S6,S9 and S11 are kept ON and inverter output voltage is -5Vs.
- m) output voltage (+Vs and -Vs): Active switches S1,S2,S5,S7,S9 and S11 are kept ON and inverter output voltage is Vs.
- n) Zero output voltage: Active switches S1,S3,S5,S7,S9 and S11 are kept ON and inverter output voltage is Zero.

IV. SIMULATION RESULTS AND DISCUSSIONS

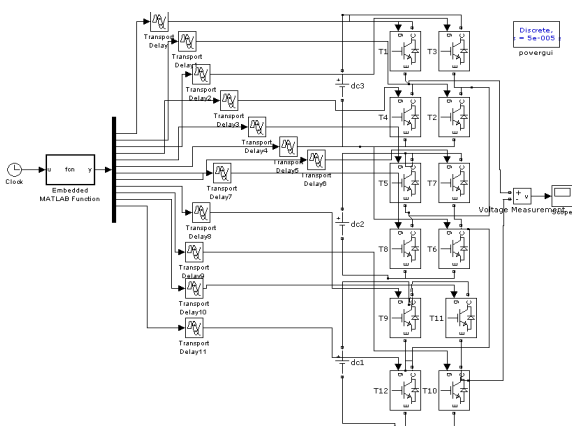


Fig. 7: Single Phase Twenty Seven Level Cascaded H-Bridge MLI

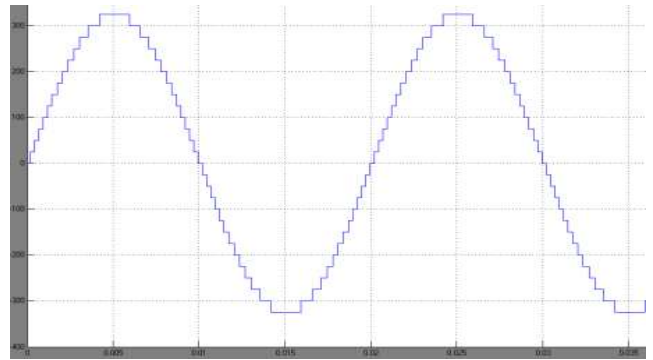


Fig. 8: Output Voltage of Twenty Seven Level CHBMLI

To validate the proposed topologies, numerical simulation studies have been carried out by using Matlab-Simulink. For the simulation studies the dc link voltage is taken as 400V. The parameters of the induction motor used in this paper are $R_s = 1.57\text{ohm}$, $R_r = 1.21\text{ohm}$, $L_m = 0.165\text{H}$, $L_s = 0.17\text{H}$, $L_r = 0.17\text{H}$ and $J = 0.089\text{Kg-m}^2$. The simulation results of proposed topologies are shown from Fig.9 – Fig.19.

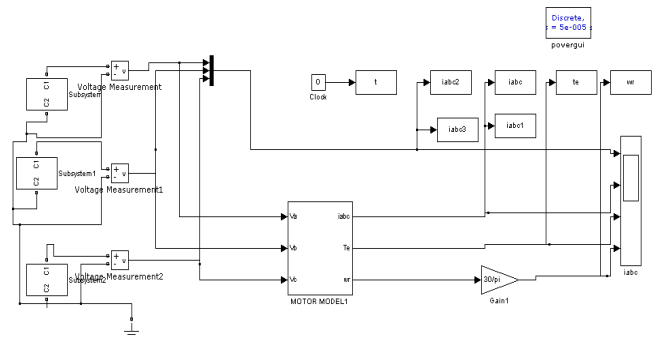


Fig. 9: Twenty Seven Level Asymmetrical Cascaded H-Bridge Multi Level inverter Fed Three Phase Induction Motor Drive

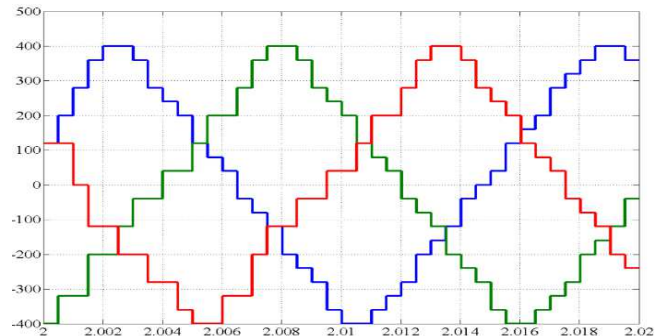


Fig. 10: Three Phase Eleven Level Output Voltage Waveforms of Cascaded H-Bridge

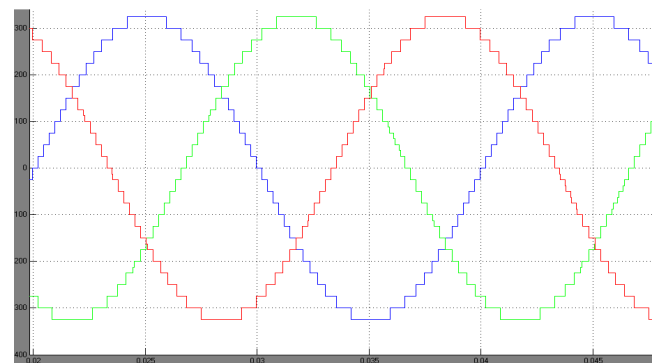


Fig. 11: Three Phase Twenty Seven Level Output Voltage Waveforms of Cascaded H-Bridge

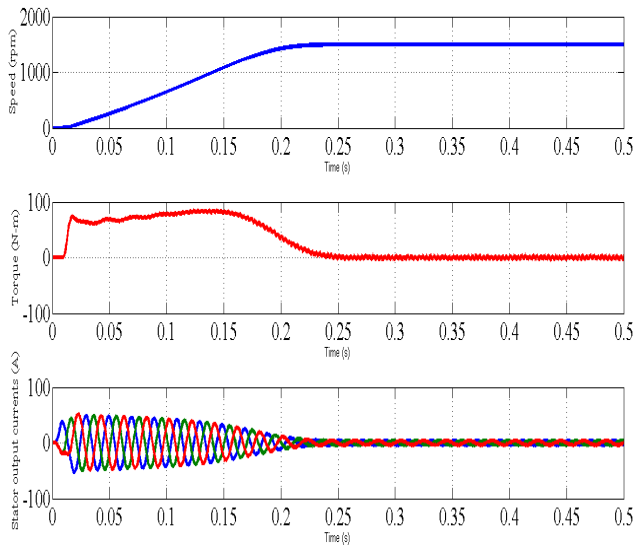


Fig. 12: Starting Transients of Eleven Level Cascaded H-Bridge Inverter Fed Three Phase Induction Motor Drive Respectively

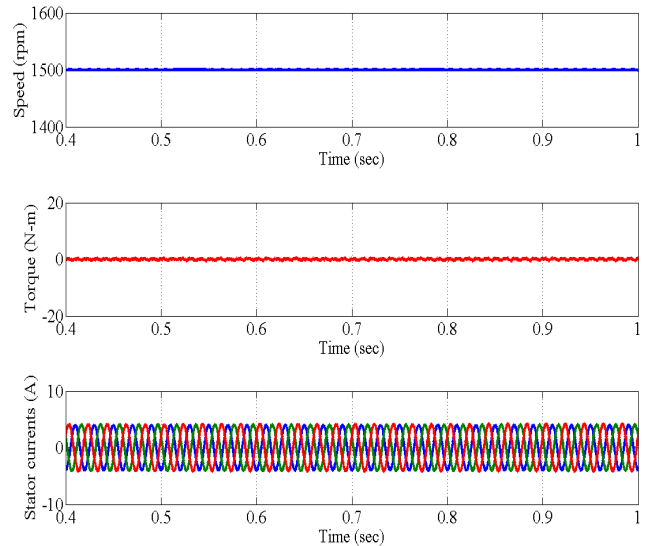


Fig. 15: Steady State Performance of Twenty Seven Level Cascaded H-Bridge Inverter Fed Three Phase Induction Motor Drive Respectively

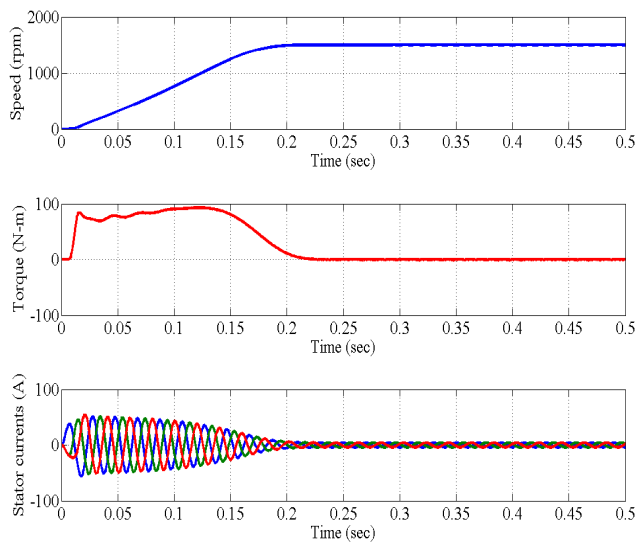


Fig. 13: Starting Transients of Twenty Seven Level Cascaded H-Bridge Inverter Fed Three Phase Induction Motor Drive Respectively

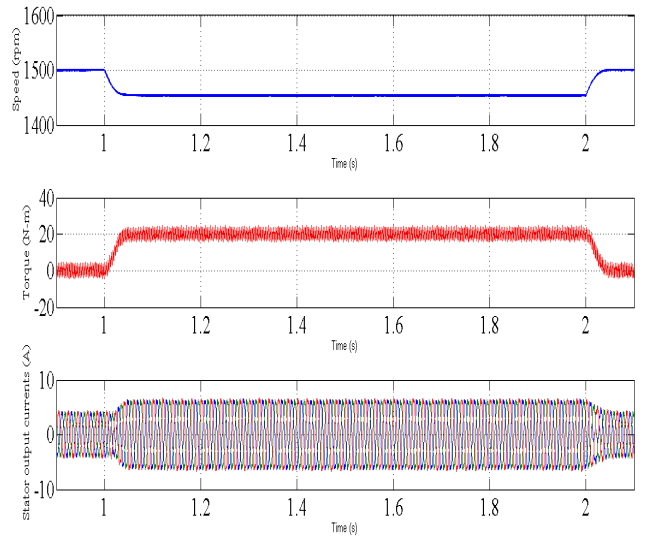


Fig. 16: Performance during Sudden Change in Load Torque of Eleven Level Cascaded H-Bridge Inverter Fed Three Phase Induction Motor Drive Respectively

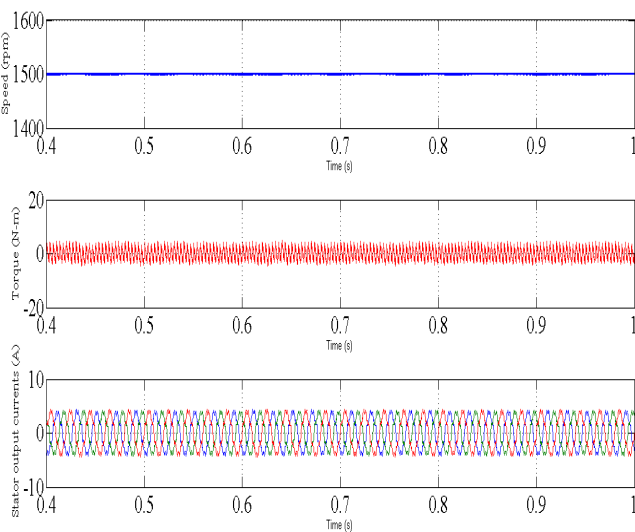


Fig. 14: Steady State Performance of Eleven Level Cascaded H-Bridge Inverter Fed Three Phase Induction Motor Drive Respectively

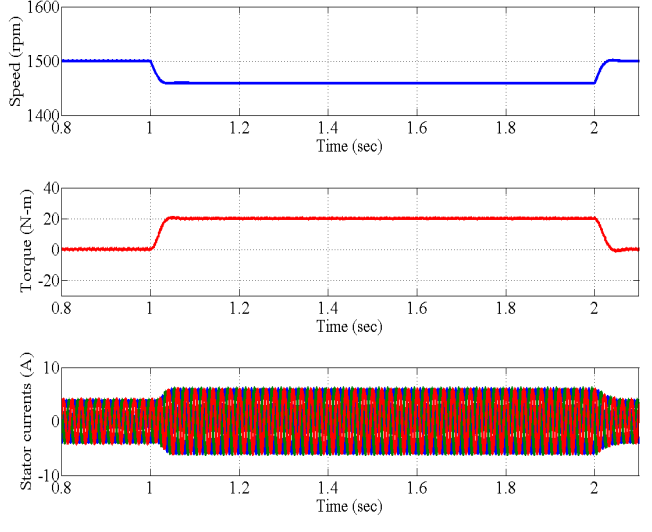


Fig. 17: Performance during Sudden Change in Load Torque of Twenty Seven Level Cascaded H-Bridge Inverter Fed Three Phase Induction Motor Drive Respectively

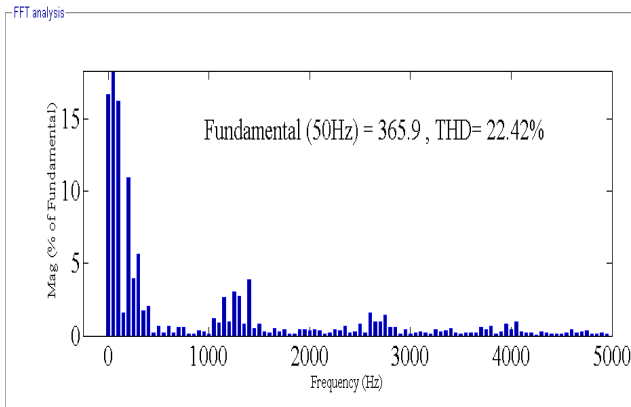


Fig. 18: Total Harmonic Distortion of Output Voltage Waveforms with Eleven Level Cascaded H-Bridge Inverters Respectively

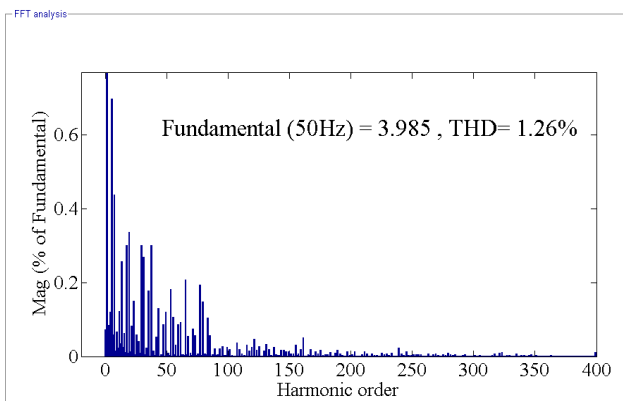


Fig. 19: Total Harmonic Distortion of Output Voltage Waveforms with Twenty Seven Level Cascaded H-Bridge Inverters Respectively

V. CONCLUSION

In this paper, a Cascaded H-bridge multi level inverter topology is proposed to offer strong advantages like an improved output waveforms, smaller filter size, and lower electromagnetic interference. Here an asymmetrical configuration with Twenty Seven level Cascaded H-bridge Multi Level inverter fed Three Phase Induction Motor Drive performance is analyzed and compared with conventional cascaded H- bridge multi level inverter. The analysis of performance factors at both transient and steady state operating conditions are satisfactory. Hence the switching losses can be reduced effectively with new switching technique of Cascaded H-bridge multi level Inverter approach by using of minimum number of switches when compared to Repeating Sequence switching topology of cascaded H- bridge multi level inverter.

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